1.6 Ω On Resistance, ± 5 V, +12 V, and +3 V Quad SPST Switches

DESCRIPTION

The DG9424E, DG9425E, DG9426E are monolithic quad single-pole-single-throw analog switches. The G9424E and DG9425E differ only in that they respond to opposite logic levels. The DG9426E has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, and one DPDT.

Using BiCMOS wafer fabrication technology allows the DG9424E, DG9425E, and DG9426E to operate on single and dual supplies. Single supply voltage ranges from 3 V to 16 V while dual supply operation is recommended with ± 3 V to ± 8 V. Each switch conducts equally well in both direction when on, and blocks input voltages up to the supply levels when off.

The low and flat on resistance over the full input signal voltage rang bring excellent linearity, reduce insertion loss and signal distortion, make them ideal for data acquisition and programmable gain control applications. These switch characters also make them ideal fit for audio signal switch and reed relay replacement.

The DG9424E, DG9425E, DG9426E feature low power dissipation, fast switching speed, and low voltage logic control threshold. Proprietary design enables the low charge injection that minimize the switching transient.

Operation temperature is specified from -40 °C to +85 °C. The DG9424E, DG9425E, DG9426E are available in 16 lead TSSOP packages.

FEATURES

- 3 V to 16 V single supply or ± 3 V thru ± 8 V dual supply operation
- 1.6 Ω typical on resistance
- 3 V logic compatible for control
- Bidirectional rail to rail signal switching
- Fast switching speed
- < 0.2 nA switch on leakage
- Break-before-make switching - DG9426

BENEFITS

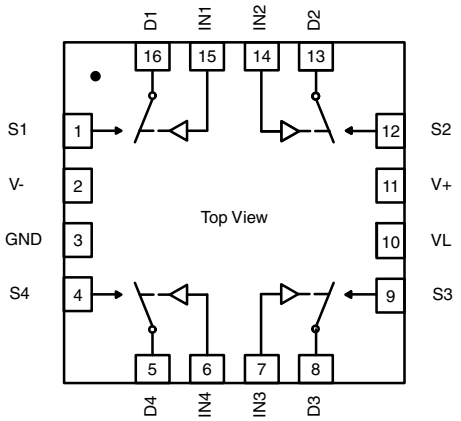
- Wide operation voltage range
- Low signal errors and distortion
- Fast switching time
- Simple interfacing

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems
- Computer peripherals
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

QFN-16 (4 mm x 4 mm)



Note

- QFN exposed pad can either be tied to V- or left floating

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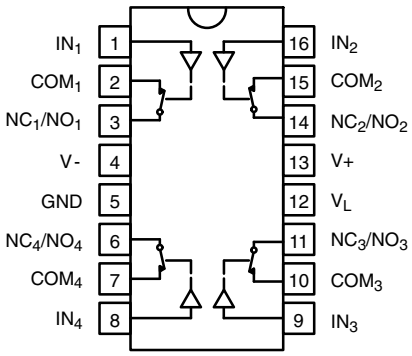
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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG9424E / DG9425E

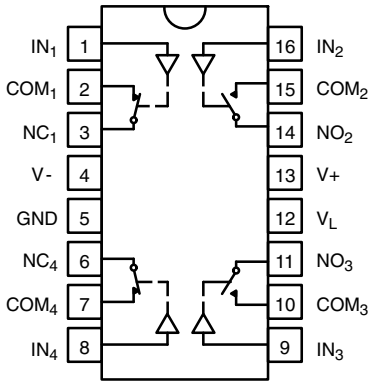
TSSOP



Top View

DG9426E

TSSOP



Top View

TRUTH TABLE		
LOGIC	**DG9424E**	**DG9425E**
0	Off	On
1	On	Off

TRUTH TABLE		
LOGIC	**SW_1, SW_4**	**SW_2, SW_3**
0	On	Off
1	Off	On

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER	PART MARKING	STD PACK QUANTITY
-40 °C to +85 °C	16-pin TSSOP	DG9424EDQ-T1-GE3	9424E	Tape and reel 3000 units
		DG9425EDQ-T1-GE3	9425E	Tape and reel 3000 units
		DG9426EDQ-T1-GE3	9426E	Tape and reel 3000 units
	QFN (4 mm x 4 mm) 16L (variation 2)	DG9424EDN-T1-GE4	9424E	Tape and reel 2500 units
		DG9425EDN-T1-GE4	9425E	Tape and reel 2500 units
		DG9426EDN-T1-GE4	9426E	Tape and reel 2500 units

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
V+ to V-		-0.3 to +18	V
GND to V-		18	
V_L		(GND - 0.3) to (V+) + 0.3	
IN, COM, NC, NO [a]		(V-) - 0.3 to (V+) + 0.3	
Continuous current (NO, NC, COM pins)		100	mA
Peak current, S or D (pulsed 1 ms, 10 % duty cycle)		200	
Storage temperature		-65 to +150	°C
Power dissipation (package) [b]	16-pin TSSOP [c]	450	mW
Thermal resistance [b]		178	°C/W
ESD human body model (HBM); per ANSI / ESDA / JEDEC® JS-001		>1500	V
Latch up current, per JESD78D		400	mA

Notes

a. Signals on NC, NO, COM or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings

b. All leads welded or soldered to PC board

c. Derate 7 mW/°C above 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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SPECIFICATIONS [a] Single Supply 12 V							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [f]**	**TEMP. [b]**	**LIMITS -40 °C to +85 °C**			**UNIT**
				MIN. [d]	**TYP. [c]**	**MAX. [d]**	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	0	-	12	V
On-resistance	R_{ON}	V+ = 10.8 V, V- = 0 V, I_{NO}, I_{NC} = 50 mA, V_{COM} = 2/9 V	Room	-	1.6	3	Ω
			Full	-	-	4	
Digital Control							
Input current	I_{INL} or I_{INH}		Full	-1	0.01	1	µA
Dynamic Characteristics							
Turn-on time [e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_{NO}, V_{NC} = 5 V, see Fig. 2	Room	-	36	51	ns
			Full	-	-	65	
Turn-off time [e]	t_{OFF}		Room	-	20	35	
			Full	-	-	44	
Break-before-make time delay [e]	t_D	DG9426E only, V_{NO}, V_{NC} = 5 V, R_L = 300 Ω, C_L = 35 pF	Room	2	-	-	
Charge injection [e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	-	38	-	pC
Off-isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-56	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-	-77	-	
NO, NC off capacitance [e]	$C_{NO(off)}$	f = 1 MHz	Room	-	49	-	pF
	$C_{NC(off)}$						
COM off capacitance [e]	$C_{COM(off)}$		Room	-	37	-	
Channel on capacitance [e]	$C_{COM(on)}$		Room	-	89	-	
Power Supplies							
Positive supply current	I+	V_{IN} = 0 or V_L	Room	-	0.02	1	µA
			Full	-	-	5	
Negative supply current	I-		Room	-1	-0.002	-	
			Full	-5	-	-	
Logic supply current	I_L		Room	-	0.002	1	
			Full	-	-	5	
Ground current	I_{GND}		Room	-1	-0.002	-	
			Full	-5	-	-	

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SPECIFICATIONS [a] Dual Supply ± 5 V							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** $V+ = 5\ V$, $V- = 5\ V$ $V_L = 5\ V$, $V_{IN} = 2.4\ V, 0.8\ V$ [f]	**TEMP.**[b]	**LIMITS -40 °C to +85 °C**			**UNIT**
				MIN. [d]	**TYP.** [c]	**MAX.** [d]	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	-5		5	V
On-resistance	R_{ON}	$V+ = 4.5\ V$, $V- = -4.5\ V$, I_{NO}, $I_{NC} = 50\ mA$	Room	-	1.9	3.3	Ω
			Full	-	-	4.3	
Switch off leakage current	$I_{NO(off)}$ $I_{NC(off)}$	$V+ = 5.5\ V$, $V- = -5.5\ V$, $V_{COM} = \pm 4.5\ V$, V_{NO}, $V_{NC} = \pm 4.5\ V$	Room	-1	-	1	nA
			Full	-10	-	10	
	$I_{COM(off)}$		Room	-1	-	1	
			Full	-10	-	10	
Channel on leakage current	$I_{COM(on)}$	$V+ = 5.5\ V$, $V- = -5.5\ V$, V_{NO}, $V_{NC} = V_{COM} = \pm 4.5\ V$	Room	-1	-	1	
			Full	-10	-	10	
Digital Control							
Input current [a]	I_{INL} or I_{INH}		Full	-1	0.05	1	µA
Dynamic Characteristics							
Turn-on time [e]	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35\ pF$, V_{NO}, $V_{NC} = \pm 3.5\ V$, see Fig. 2	Room	-	48	67	ns
			Full	-	-	81	
Turn-off time [e]	t_{OFF}		Room	-	34	57	
			Full	-	-	67	
Break-before-make time delay [e]	t_D	DG9426E only, V_{NO}, $V_{NC} = 3.5\ V$, $R_L = 300\ \Omega$, $C_L = 35\ pF$	Room	2	-	-	
Charge injection [e]	Q_{INJ}	$V_g = 0\ V$, $R_g = 0\ \Omega$, $C_L = 1\ nF$	Room	-	112	-	pC
Off isolation [e]	OIRR	$R_L = 50\ \Omega$, $C_L = 5\ pF$, $f = 1\ MHz$	Room	-	-56	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-	-82	-	
Source off capacitance [e]	$C_{NO(off)}$ $C_{NC(off)}$	$f = 1\ MHz$	Room	-	38	-	pF
Drain off capacitance [e]	$C_{COM(off)}$		Room	-	38	-	
Channel on capacitance [e]	$C_{COM(on)}$		Room	-	89	-	
Power Supplies							
Positive supply current [e]	I+	$V_{IN} = 0$ or V_L	Room	-	0.03	1	µA
			Full	-	-	5	
Negative supply current [e]	I-		Room	-1	-0.002	-	
			Full	-5	-	-	
Logic supply current [e]	I_L		Room	-	0.002	1	
			Full	-	-	5	
Ground current [e]	I_{GND}		Room	-1	-0.002	-	
			Full	-5	-	-	

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SPECIFICATIONS [a] Single Supply 5 V							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V [f]**	**TEMP.[b]**	**LIMITS -40 °C to +85 °C**			**UNIT**
				MIN.[d]	**TYP.[c]**	**MAX.[d]**	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	-	-	5	V
On-resistance [e]	R_{ON}	V+ = 4.5 V, I_{NO}, I_{NC} = 50 mA	Room	-	3.1	4.8	Ω
			Full	-	-	5.8	
Dynamic Characteristics							
Turn-on time [e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_{NO}, V_{NC} = 3.5 V, see Fig. 2	Room	-	62	78	ns
			Hot	-	-	106	
Turn-off time [e]	t_{OFF}		Room	-	29	44	
			Hot	-	-	56	
Break-before-make time delay [e]	t_D	DG9426E only, V_{NO}, V_{NC} = 3.5 V, R_L = 300 Ω, C_L = 35 pF	Room	5	-	-	
Charge injection [e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	-	10	-	pC
Power Supplies							
Positive supply current [e]	I+	V_{IN} = 0 or V_L	Room	-	0.02	1	µA
			Hot	-	-	5	
Negative supply current [e]	I-		Room	-1	-0.002	-	
			Hot	-5	-	-	
Logic supply current [e]	I_L		Room	-	0.002	1	
			Hot	-	-	5	
Ground current [e]	I_{GND}		Room	-1	-0.002	-	
			Hot	-5	-	-	

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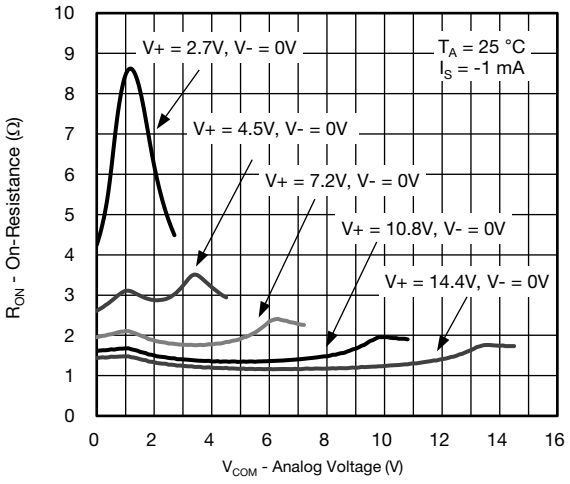
SPECIFICATIONS [a] Single Supply 3 V							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V- = 0 V V_L = 3 V, V_{IN} = 2.4 V, 0.4 V [f]**	**TEMP.[b]**	**LIMITS -40 °C to +85 °C**			**UNIT**
				MIN. [d]	**TYP. [c]**	**MAX. [d]**	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	0	-	3	V
On-resistance	R_{ON}	V+ = 2.7 V, V- = 0 V. I_{NO}, I_{NC} = 5 mA, V_{COM} = 0.5, 2.2 V	Room	-	6	-	Ω
			Full	-	-	-	
Switch off leakage current [a]	$I_{NO(off)}$	V+ = 3.3 V, V- = 0 V. V_{COM} = 0.3, 3 V, V_{NO}, V_{NC} = 3, 0.3 V	Room	-1	-	1	nA
	$I_{NC(off)}$		Full	-10	-	10	
	$I_{COM(off)}$		Room	-1	-	1	
			Full	-10	-	10	
Channel on leakage current [a]	$I_{COM(on)}$	V+ = 3.3 V, V- = 0 V, V_{NO}, V_{NC} = V_{COM} = 0.3, 3 V	Room	-1	-	1	
			Full	-10	-	10	
Digital Control [e]							
Input current	I_{INL} or I_{INH}		Full	-1	0.005	1	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	R_L = 300 Ω, C_L = 35 pF. V_{NO}, V_{NC} = 1.5 V, see Fig. 2	Room	-	170	-	ns
			Full	-	-	230	
Turn-off time	t_{OFF}		Room	-	65	-	
			Full	-	-	89	
Break-before-make time delay	t_D	DG9426E only, V_{NO}, V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF	Room	5			
Charge injection [e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	-	15	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-56	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-	-80	-	
Source off capacitance [e]	$C_{NO(off)}$	f = 1 MHz	Room	-	53	-	pF
	$C_{NC(off)}$						
Drain off capacitance [e]	$C_{COM(off)}$		Room	-	42	-	
Channel on capacitance [e]	$C_{COM(on)}$		Room	-	92	-	

Notes

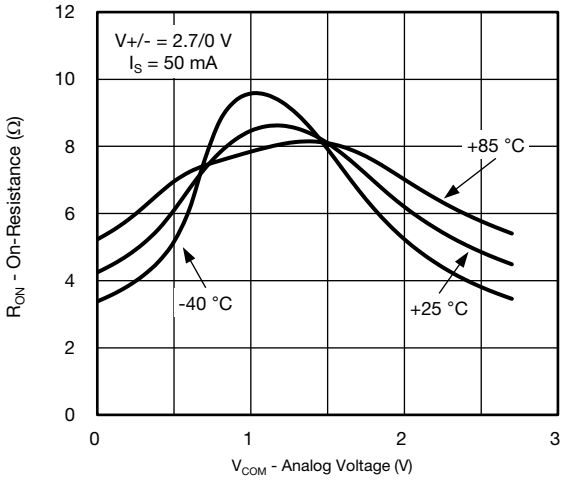
a. Leakage parameters are guaranteed by worst case test conditions and not subject to production test
b. Room = 25 °C, Full = As determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = Input voltage to perform proper function

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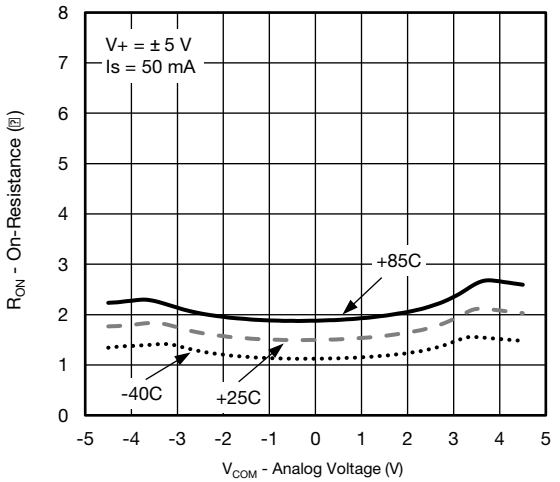
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



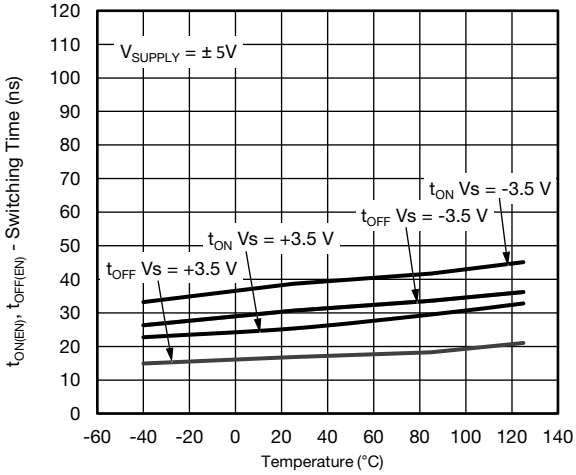
R_{ON} vs. V_{COM} and Supply Voltage



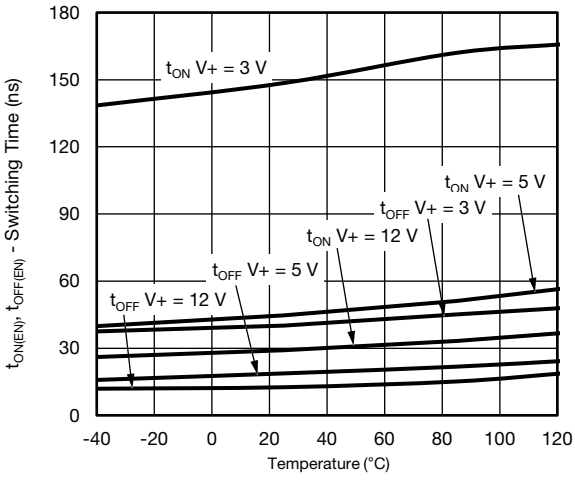
R_{ON} vs. Analog Voltage and Temperature



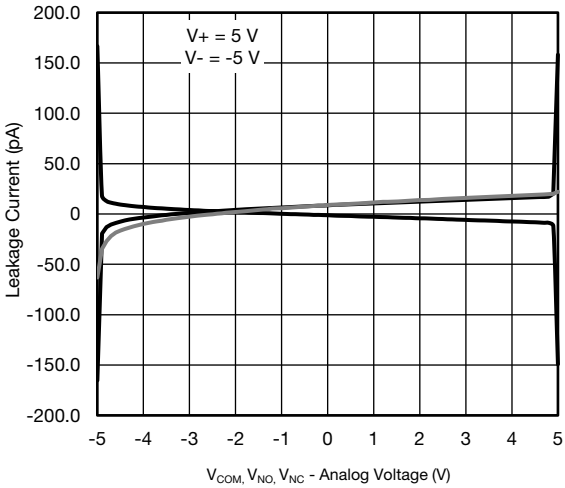
R_{ON} vs. Analog Voltage and Temperature



Switching Time vs. Temperature and Dual Supply Voltage



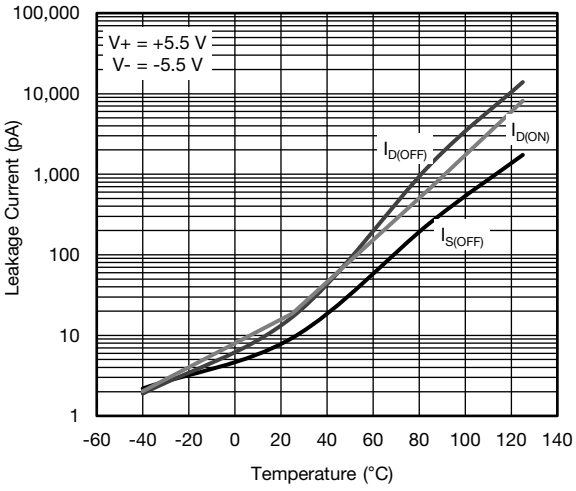
Switching Time vs. Temperature and Single Supply Voltage



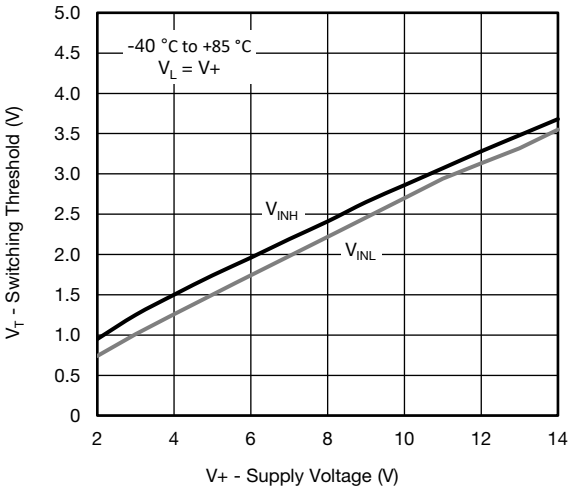
Leakage Current vs. Analog Voltage

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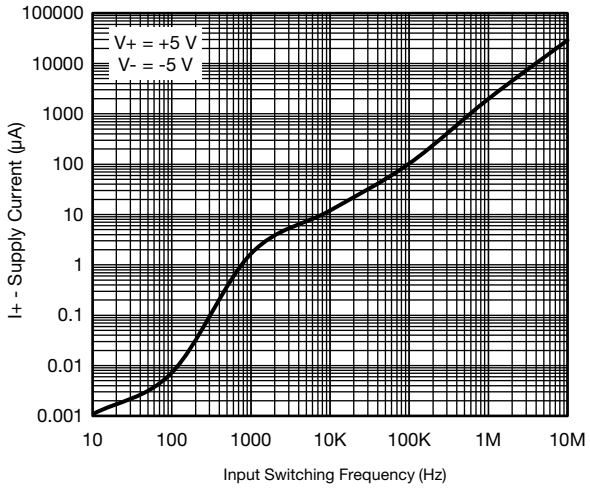
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



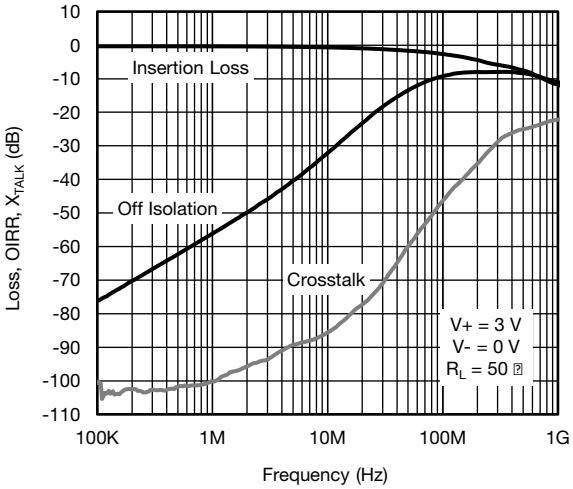
Leakage Current vs. Temperature



Switching Threshold vs. Supply Voltage



Switching Current vs. Input Switching Frequency



Insertion Loss, Off Isolation and Crosstalk vs. Frequency

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SCHEMATIC DIAGRAM (typical channel)

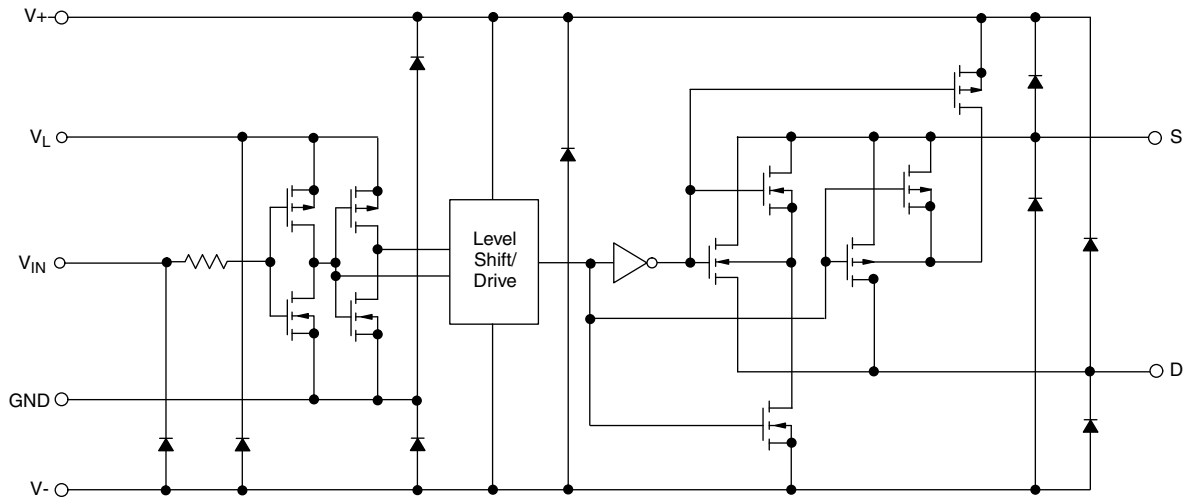
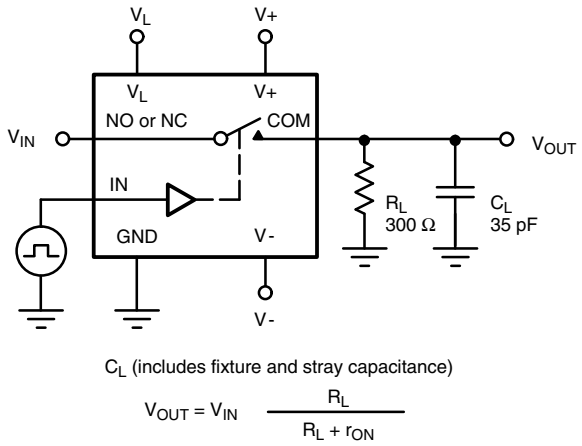


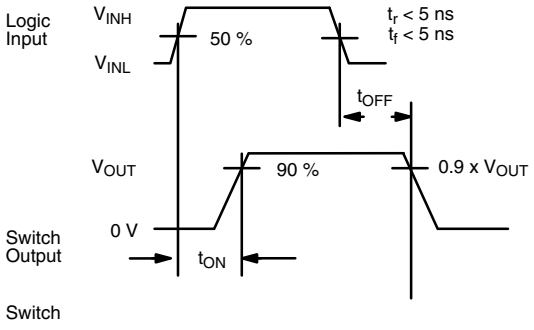
Fig. 1

TEST CIRCUITS



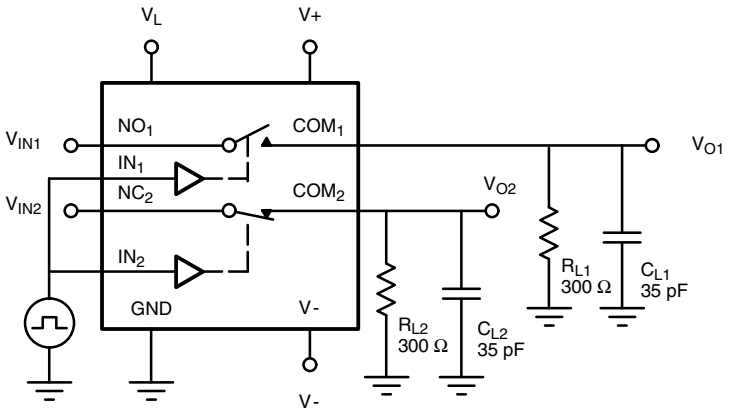
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time



C_L (includes fixture and stray capacitance)

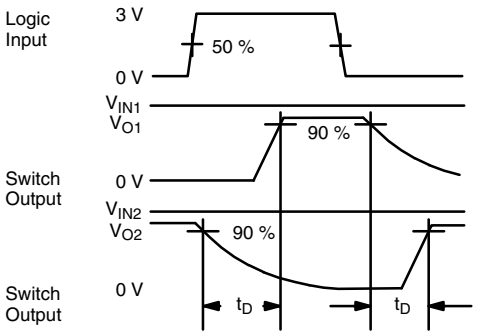
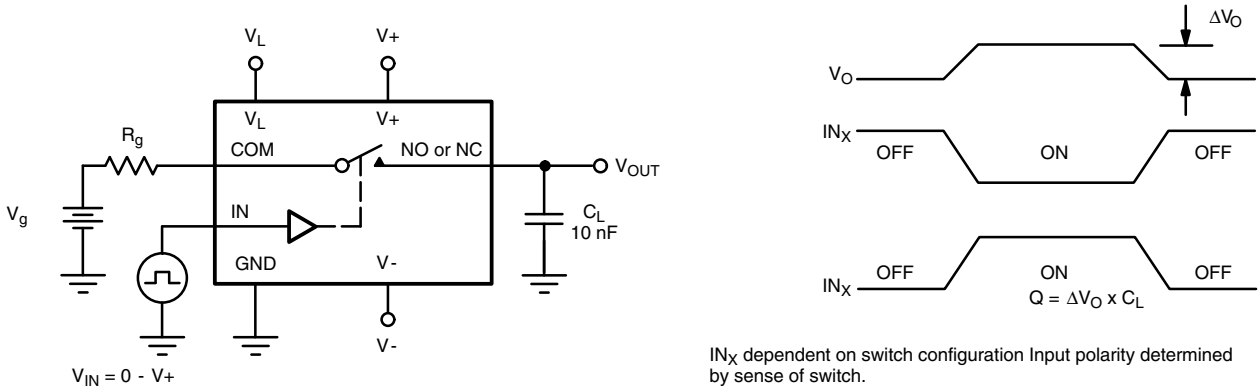


Fig. 3 - Break-Before-Make (DG9426E)

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TEST CIRCUITS



IN_X dependent on switch configuration Input polarity determined by sense of switch.

Fig. 4 - Charge Injection

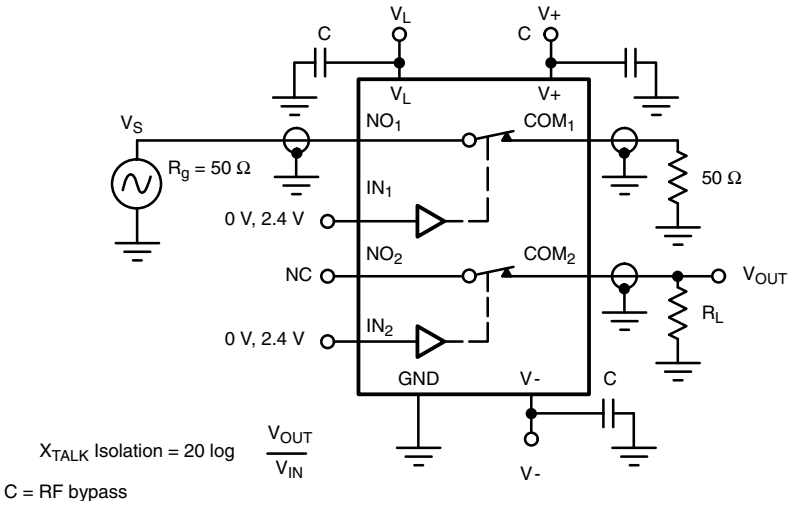


Fig. 5 - Crosstalk

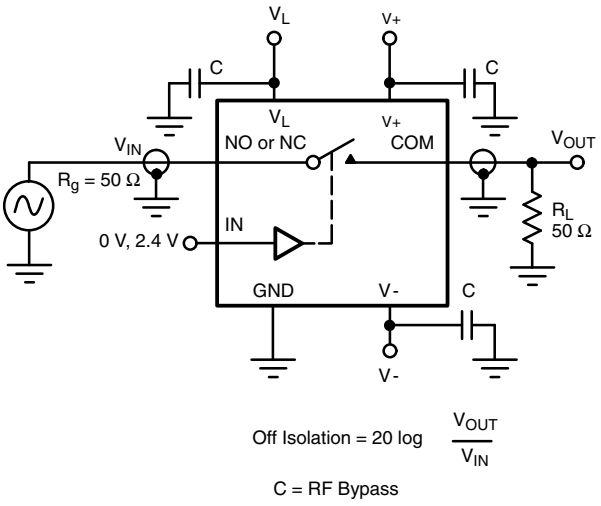


Fig. 6 - Off-Isolation

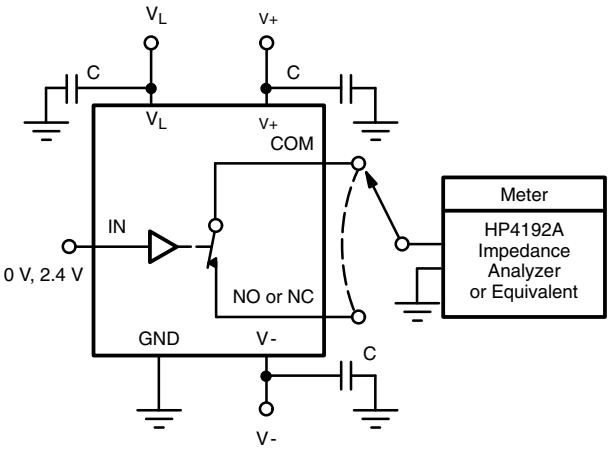


Fig. 7 - Source/Drain Capacitances

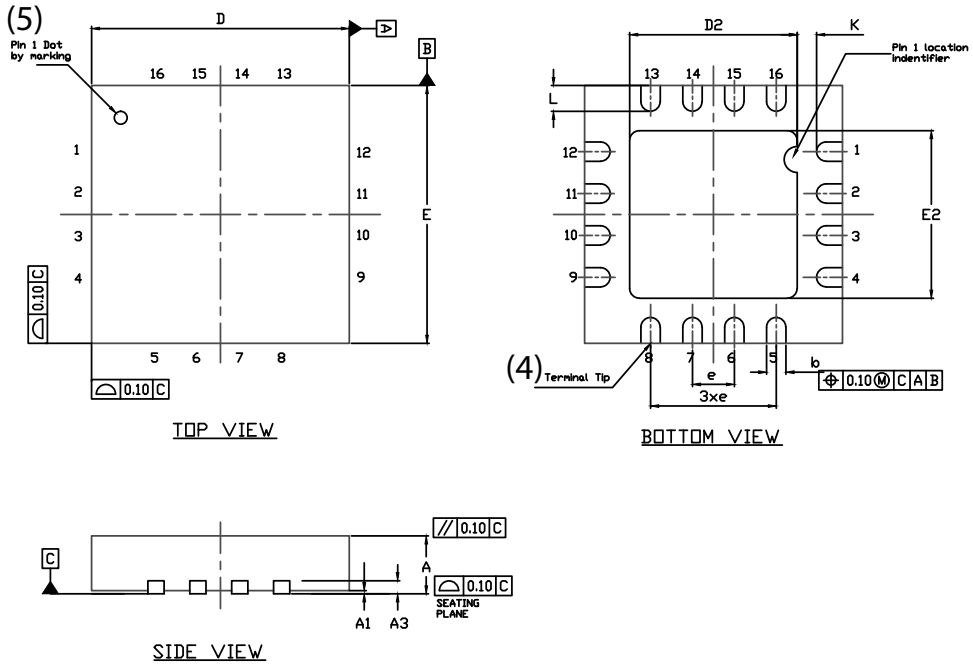
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PRODUCT SUMMARY						
Part number	DG9424E	DG9424E	DG9425E	DG9425E	DG9426E	DG9426E
Status code	2	2	2	2	2	2
Configuration	SPST x 4, NO	SPST x 4, NO	SPST x 4, NC	SPST x 4, NC	SPST x 4, comp	SPST x 4, comp
Single supply min. (V)	3	3	3	3	3	3
Single supply max. (V)	16	16	16	16	16	16
Dual supply min. (V)	3	3	3	3	3	3
Dual supply max. (V)	8	8	8	8	8	8
On-resistance (Ω)	1.6	1.6	1.6	1.6	1.6	1.6
Charge injection (pC)	38	38	38	38	38	38
Source on capacitance (pF)	89	89	89	89	89	89
Source off capacitance (pF)	37	37	37	37	37	37
Leakage switch on typ. (nA)	-	-	-	-	-	-
Leakage switch off max. (nA)	1	1	1	1	1	1
-3 dB bandwidth (MHz)	-	-	-	-	-	-
Package	TSSOP-16	QFN-16 4 x 4	TSSOP-16	QFN-16 4 x 4	TSSOP-16	QFN-16 4 x 4
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare, portable	Multi purpose, instrumentation, medical and healthcare, portable	Multi purpose, instrumentation, medical and healthcare, portable	Multi purpose, instrumentation, medical and healthcare, portable	Multi purpose, instrumentation, medical and healthcare, portable	Multi purpose, instrumentation, medical and healthcare, portable
Interface	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Turn on time max. (ns)	51	51	51	51	51	51
Crosstalk and off isolation	-56	-56	-56	-56	-56	-56

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QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS[1]			INCHES			MILLIMETERS[1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N[3]	16			16			16			16		
Nd[3]	4			4			4			4		
Ne[3]	4			4			4			4		

Notes

(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

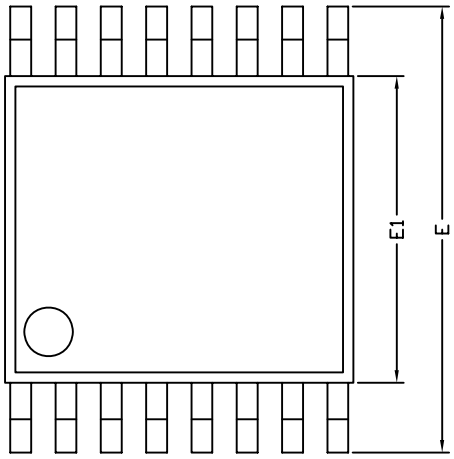
ECN: S13-0893-Rev. B, 22-Apr-13
DWG: 5890

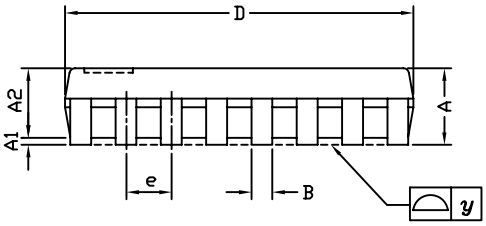
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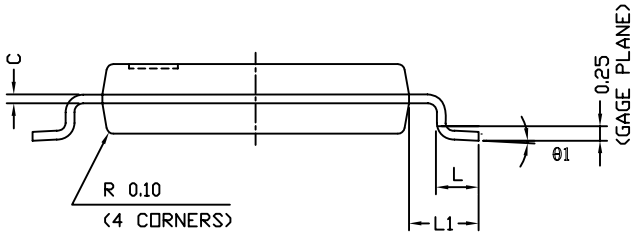
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TSSOP: 16-LEAD



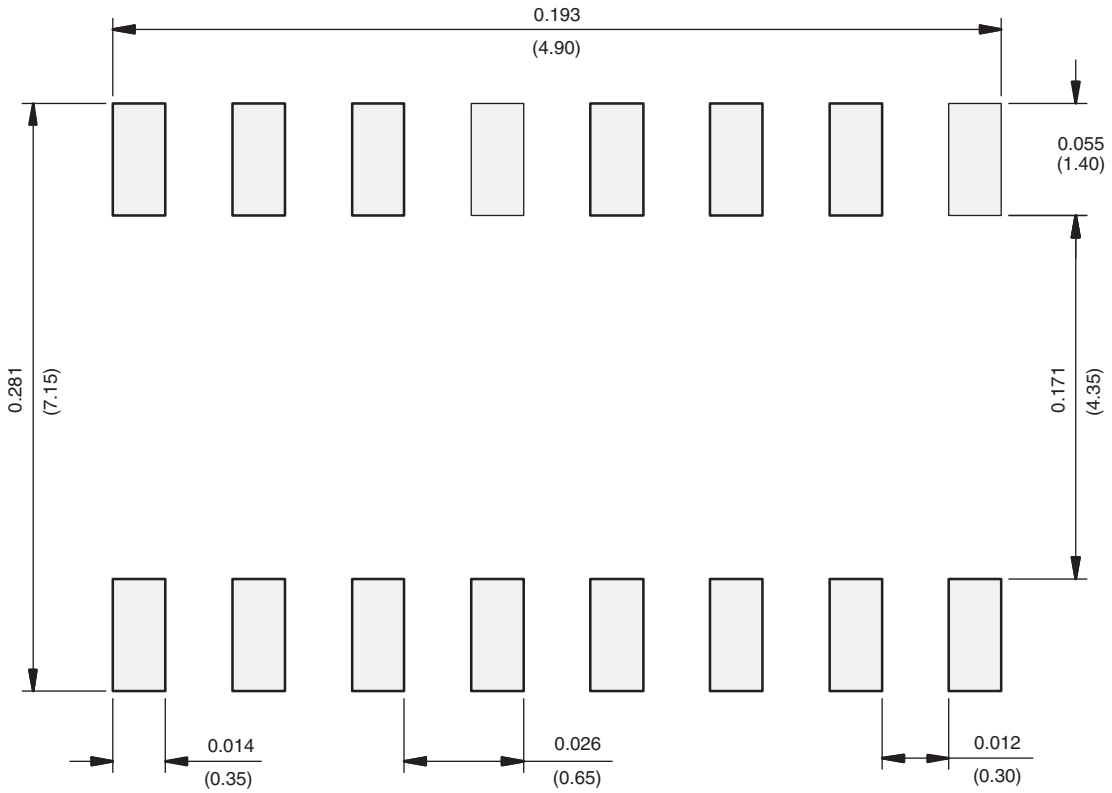




Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

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RECOMMENDED MINIMUM PAD FOR TSSOP-16

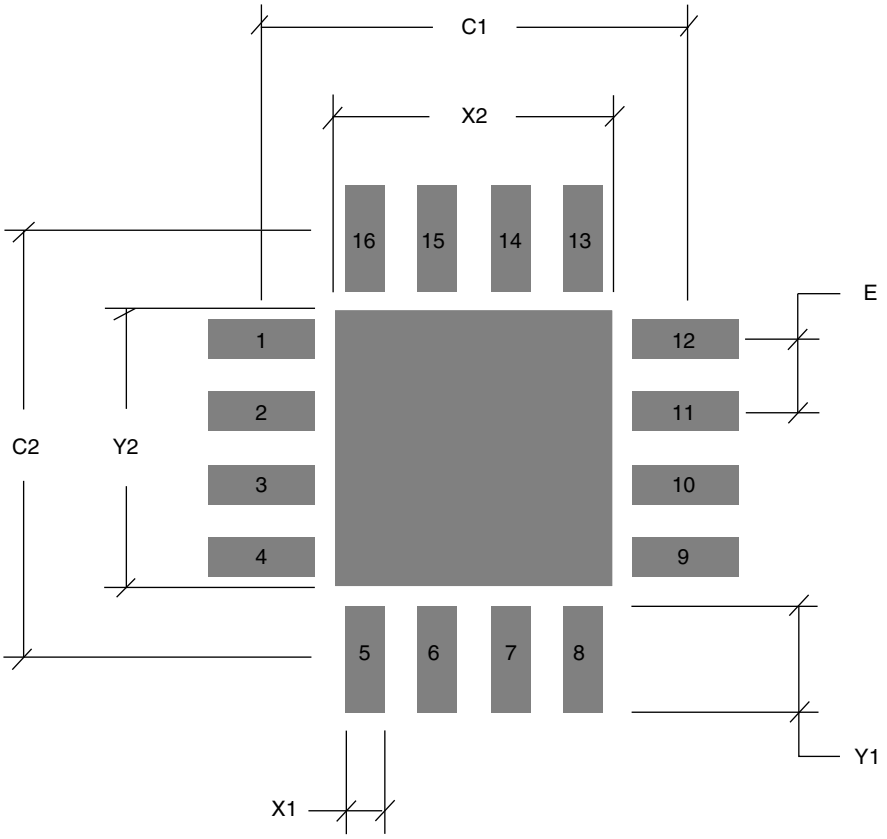


Recommended Minimum Pads
Dimensions in inches (mm)

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RECOMMENDED MINIMUM PADS FOR QFN-16
(4 mm x 4 mm BODY, Variation 2)



	INCHES	MILLIMETERS
C1	0.149	3.785
C2	0.149	3.785
E	0.026	0.65
X1	0.012	0.305
X2	0.104	2.642
Y1	0.032	0.813
Y2	0.104	2.642

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