Qualcomm SiRFstar IV 4e

Qualcomm® SiRFstar™ IV GSD4e B03 WLCSP is a comprehensive navigation processor built on a low-power RF CMOS single-die, incorporating the baseband, integrated navigation solution, software, ARM®7 processor, and RF functions that are designed to form a complete internal ROM-based standalone or Aided-GPS engine. GSD4e WLCSP is based on the new SiRFstar IV architecture. GSD4e WLCSP aims to lower BoM costs and risk while delivering automotive industry-leading GPS performance in a compact solution. GSD4e WLCSP serves the traditional GPS engine space because it is engineered to generate a PVT solution without relying upon host device processing power or other resources.

SiRFstar IV 4e Specs

Location

Satellite Systems Support

- GPS

Jammer Remover/Tracking

- Up to 8 CW Jammers
- Up to 80 dB-Hz

Verification Channels

- 48 Channels

CPU

CPU Cores

- ARM7 CPU

Interface

Supported Interfaces

- UART
- SPI
- I²C

Package

Package Type

- WLCSP
- 3.5 x 3.2 x 0.6mm 0.5mm pitch WLCSP

Package Size

- 0.5mm Pitch

Product Details | Benefits | Key Features

GPS RF

- Integrated LNA
- Single-SAW filter design
- Fractional-N synthesiser
- SPI control interface
- TCXO input (crystal oscillator input/output supported)
- TCXO power control with pre-warm-up capability
- ADC block with selectable 2 and 4-bit quantisation
- Automatic RF circuit tuning with digital read-out and restore by software via SPI messages

GPS Signal Processing

- Enhanced DSP core has more than twice the clock speed and more than double the RAM capacity relative to previous DSP core
- Scanning, detection and tracking of CW tones in IF bandwidth
- CW filtering and excision
- Matched filter acquisition and tracking processing based on DSP core
- Tracking hardware based on DSP core
- Automated internal hardware blanking capability

ARM7TDMI Microprocessor System

- Industry-standard ARM 7TDMI CPU core
- Uses internal ROM as code storage for PVT applications
- Separate power domains for E-fuse, DSP core, patch RAM and ARM 7TDMI subsystem

Package Option

- 42-ball WLCSP, 3.5 x 3.2 x 0.6mm, 0.5mm pitch
- Integrated Power Management Unit (PMU)
- Primary input is 1.8V:
- All I/O is 1.8V
- Integrated regulators run from 1.8V
- KA LDO provides 1.2V non-volatile core voltage supply
- Main switch-mode regulator provides 1.2V baseband and RF core voltage supply
- Low-overhead LDO for 0.96V main core standby voltage supply
- Integrated finite state machine for power sequencing and low-power modes
- Use integrated LDO mode in place of switch-mode regulator for reduced BOM size
- Internal power control allows unswitched external bypass source supply

I/O and Interfaces

- Host port options UART, SPI, I²C
- Additional I²C port for dead reckoning, sensor inputs and serial flash patch source
- Aiding inputs for time and frequency
- Arbitration I/O for multi-function radio coordination
- Tiny footprint as functions are multiplexed
- CMOS I/O runs from 1.8V, is 3.6V tolerant, and failsafe when not powered

The technology in the SiRFstar IV is designed to balance maximum performance with minimal power consumption. It is engineered to break the old GPS performance vs power trade off through the fusion of a new high performance GPS engine, advanced power management, and a smart sensor interface to achieve high sensitivity hot start conditions for fast location fixes while drawing only 50-400 µA.

Premium on-chip software is designed to provide a new level of continuous location awareness by employing the following advanced technology:

- Opportunistic ephemeris decode and advanced power management to allow the GPS receiver to stay in a hot start condition nearly continuously while consuming very little power
- Local ephemeris prediction, capturing ephemerides, and predicting them three days to one week in advance boosts sensitivity and performance
- Dynamic contextual awareness, temperature monitoring, and MEMS sensors to work in concert to conserve power and boost performance

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