3-Axis, ±16 *g*, I²S Digital Accelerometer

Data Sheet ADXL317

FEATURES

48 kHz I²S/TDM digital output
High resolution: 14 bits
Directly compatible with the AD2425W, AD2428W, and AD2429W A²B transceivers
User selectable bandwidth: 500 Hz to 4 kHz
Low latency: 90 µs typical at 4 kHz bandwidth
Low noise
- **55 µ*g*/√Hz typical for x- and y-axes**
- **120 µ*g*/√Hz typical for z-axis**

Operating temperature range: −40°C to +125°C
Small, thin package: 5 mm × 5 mm × 1.45 mm LFCSP
AEC-Q100 qualified for automotive applications

APPLICATIONS

Wideband ANC
Adaptive suspension control

GENERAL DESCRIPTION

The ADXL317 is a small, thin, low latency, 3-axis accelerometer with high resolution (14-bit) measurement up to ±16 *g*. Digital output data is formatted as an I²S/time-division multiplexing (TDM) signal. Additionally, an I²C digital interface is provided for user configuration.

The ADXL317 is well suited for wideband active noise control (ANC) applications. Featuring very low latency from the moment of acceleration to the transmission of digital output data, the ADXL317 is uniquely capable of responding quickly enough to allow wideband ANC systems sufficient time to respond to noise scenarios. The low noise of the ADXL317 enhances the ability of the device to accurately discriminate various external noise sources.

Due to the wide operating temperature range and high performance, the ADXL317 is ideal for other wheel well applications, such as adaptive suspension control.

The Automotive Audio Bus (A²B®) developed by Analog Devices, Inc., introduces system wide savings in cabling costs. The ADXL317 is designed to interface directly with the A²B product portfolio, such as the AD2425W, AD2428W, and AD2429W A²B transceivers.

The ADXL317 is supplied in a small, thin, 5 mm × 5 mm × 1.45 mm, 32-pin LFCSP package. The device is qualified for use in automotive applications over the entire operating temperature range of −40°C to +125°C.

Note that throughout this data sheet, multifunction pins, such as DTX1/TPC, are referred to either by the entire pin name or by a single function of the pin, for example, DTX1, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM

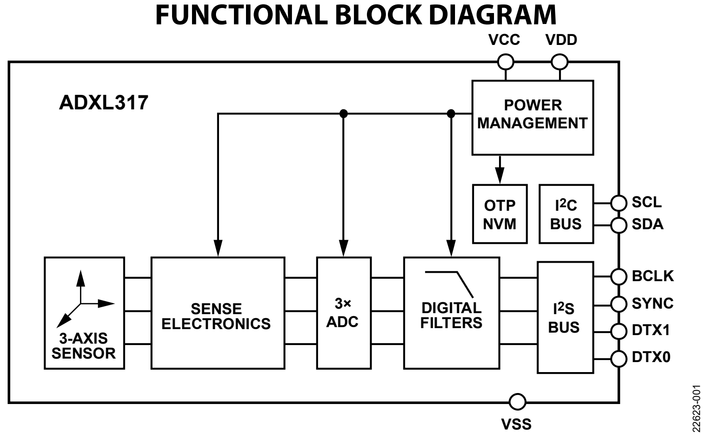


Figure 1.

Rev. 0
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

12/2019—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25 °C, V_{CC} = 3.3 V, acceleration = 0 *g*, nominal clock set to 3.072 MHz or 6.144 MHz, unless otherwise specified. For complete definitions and conditions of all specifications, refer to the Terminology section.

Table 1. Accelerometer Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR		Each axis				
Full-Scale Range	FSR		±16			*g*
Nonlinearity		Percentage of full-scale range		±1#		%
Cross Axis Sensitivity				±1		%
Resonant Frequency	f_0					
X- and Y-Axes				5.10		kHz
Z-Axis				3.15		kHz
Quality Factor	Q					
X- and Y-Axes				3.3		
Z-Axis				1.75		
SENSITIVITY		Each axis				
Sensitivity[1]		DC response				
500 Hz Cascaded Filter			454.5	500	555.6	LSB/*g*
1 kHz Cascaded Filter			461.5	507.6	564.0	LSB/*g*
2 kHz Cascaded Filter			468.6	515.5	572.7	LSB/*g*
4 kHz Cascaded Filter			519.5	571.4	634.9	LSB/*g*
Sensitivity Change Due to Temperature		−40°C ≤ T_A ≤ +25°C and +25°C ≤ T_A ≤ +125°C				
X- and Y-Axes		1σ		±2.5		%
Z-Axis		1σ		±4.5		%
RESOLUTION						
Measurement Resolution		All axes		14		Bits
ZERO *g* BIAS LEVEL		Each axis				
0 *g* Bias Error		Over full operating temperature range	−1.5		+1.5	*g*
Initial 0 *g* Output Deviation						
X- and Y-Axes				±200		m*g*
Z-Axis				±500		m*g*
FREQUENCY RESPONSE		User selectable				
Cutoff (−3 dB) Frequency		Filters only				
500 Hz Cascaded Filter				506		Hz
1 kHz Cascaded Filter				1012		Hz
2 kHz Cascaded Filter				2025		Hz
4 kHz Cascaded Filter				4051		Hz
NOISE						
Noise Density[2]						
X- and Y-Axes				55		μ*g*/√Hz
Z-Axis				120		μ*g*/√Hz
Output Noise, X- and Y-Axes						
500 Hz Cascaded Filter				2.5	4	m*g* rms
1 kHz Cascaded Filter				5.5	10	m*g* rms
2 kHz Cascaded Filter				22.5	35	m*g* rms
4 kHz Cascaded Filter				85	110	m*g* rms
Output Noise Z-Axis						
500 Hz Cascaded Filter				4	9	m*g* rms
1 kHz Cascaded Filter				7	12	m*g* rms
2 kHz Cascaded Filter				30	40	m*g* rms
4 kHz Cascaded Filter				120	135	m*g* rms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SELF TEST						
Positive Self Test Output Change	+STΔ	DC self test magnitude				
X- and Y-Axes			2.16	3.6	5.04	*g*
Z-Axis			4.08	6.8	9.52	*g*
Negative Self Test Output Change	−STΔ	DC self test magnitude				
X- and Y-Axes			−5.04	−3.6	−2.16	*g*
Z-Axis			−9.52	−6.8	−4.08	*g*
SUPPLY						
Operating Voltage	V_{CC}		3.0	3.3	3.6	V
Regulated Input/Output (I/O) Voltage	V_{DD}			1.8		V
Quiescent Supply Current					5	mA
Turn On Time				200		µs
I^2S/TDM INTERFACE						
Frame Rate				48		kHz
Word Size						
I^2S/TDM2				32		Bits
TDM4				16, 32		Bits
TDM8				16		Bits
Input Clock Frequency		BCLK from master device				
I^2S/TDM2		32-bit word size		3.072		MHz
TDM4		16-bit word size		3.072		MHz
		32-bit word size		6.144		MHz
TDM8		16-bit word size		6.144		MHz
LATENCY						
Filter delay		Filters only; does not include sense electronics or analog-to-digital converter (ADC)				
500 Hz Bandwidth				585		µs
1 kHz Bandwidth				291		µs
2 kHz Bandwidth				144		µs
4 kHz Bandwidth				70.9		µs
Additional Latency		Sense electronics and ADC				
X- and Y-Axes				13.8		µs
Z-Axis				20.4		µs
ENVIRONMENTAL						
Operating Temperature Range			−40		+125	°C

[1] Sensitivity varies with filter setting and deviation from nominal clock frequency. This specification assumes a nominal clock of 3.072 MHz or 6.144 MHz.
[2] Noise density at 100 Hz with high-pass filter disabled (x_HPF_EN = 0). Noise density may vary across frequency.

TIMING SPECIFICATIONS

Table 2. I^2C Digital Input/Output Characteristics

Parameter	Test Conditions/Comments	Limit[1] Min	Max	Unit
Digital Input				
Input Voltage Level				
Low (V_{IL})			$0.3 \times V_{DD}$	V
High (V_{IH})		$0.7 \times V_{DD}$		V
Input Current Level				
Low (I_{IL})	$V_{IN} = V_{DD}$		0.1	µA
High (I_{IH})	$V_{IN} = 0$ V	−0.1		µA
Digital Output				
Output Voltage Level				
Low (V_{OL})	$V_{DD} = 1.8$ V, $I_{OL} = 3$ mA		400	mV
Output Current Level				
Low (I_{OL})	$V_{OL} = V_{OL, MAX}$	3		mA
Pin Capacitance	$f_{IN} = 1$ MHz, $V_{IN} = 2.5$ V		8	pF
Input Frequency			100	kHz

[1] Limits are based on characterization results and are not production tested.

Table 3. I^2C Timing ($T_A = 25°C$, $V_{CC} = 3.3$ V)

Parameter	Limit[1, 2] Min	Max	Unit	Description
f_{SCL}		100	kHz	SCL clock frequency
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	SCL high time
t_3	1.3		µs	SCL low time
t_4	0.6		µs	Start/repeated start condition hold time
t_5	100		ns	Data setup time
t_6[3, 4, 5, 6]	0	0.9	µs	Data hold time
t_7	0.6		µs	Repeated start condition setup time
t_8	0.6		µs	Stop condition setup time
t_9	1.3		µs	Bus-free time between a stop condition and a start condition
t_{10}		300	ns	Rise time of both SCL and SDA when receiving
	0		ns	Rise time of both SCL and SDA when receiving or transmitting
t_{11}		250	ns	Fall time of SDA when receiving
		300	ns	Fall time of both SCL and SDA when transmitting
	$20 + 0.1\ C_b$[7]		ns	Fall time of both SCL and SDA when receiving or transmitting
C_b		400	pF	Capacitive load for each bus line

[1] Limits are based on characterization results, with $f_{SCL} = 100$ kHz, and are not production tested.
[2] All values are in reference to the V_{IH} and V_{IL} levels shown in Table 2.
[3] t_6 is the data hold time measured from the falling edge of SCL. t_6 applies to data transmission and acknowledge.
[4] A transmitting device must internally provide an output hold time of at least 300 ns for the SDA signal (with respect to $V_{IH, MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[5] The maximum t_6 value must be met only if the device does not stretch the low period (t_3) of the SCL signal.
[6] The maximum value for t_6 is a function of the clock low time (t_3), the clock rise time (t_{10}), and the minimum data setup time ($t_{5, MIN}$). This value, t_6, is calculated as $t_{6, MAX} = t_3 - t_{10} - t_{5, MIN}$.
[7] C_b is the total capacitance of one bus line in picofarads.

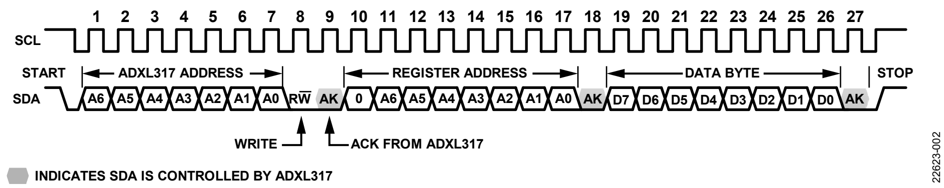


Figure 2. I²C Single-Byte Register Write

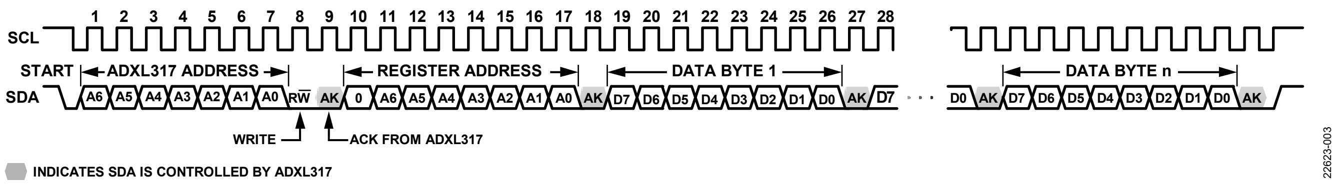


Figure 3. I²C Multibyte Register Write

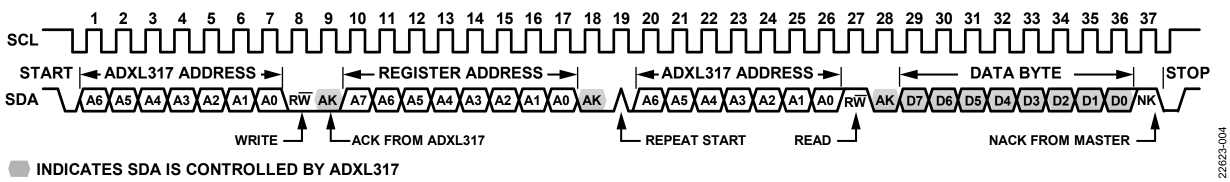


Figure 4. I²C Single-Byte Register Read

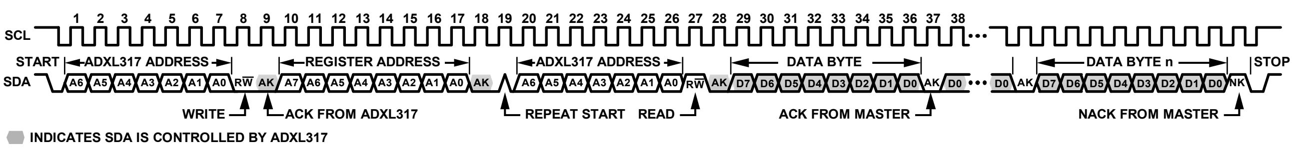


Figure 5. I²C Multibyte Register Read

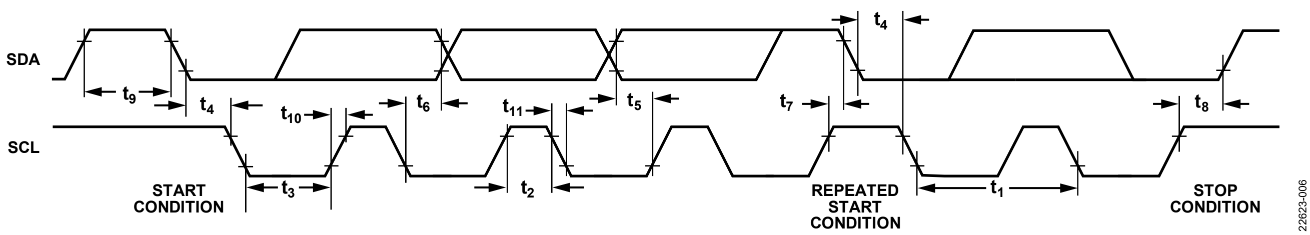


Figure 6. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Mechanical Shock	
Any Axis, Unpowered	±4000 *g* (0.5 ms half sine)
Any Axis, Powered	±2000 *g* (0.5 ms half sine)
Voltage	
Supply Voltage	−0.3 V to +4.0 V
Any Pin to Ground	−0.3 V to V_{DD} + 0.3 V
Electrostatic Discharge (ESD)	
Human Body Model (HBM), All Pins	2 kV
Latch-Up Current	100 mA
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

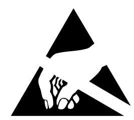
θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CS-32-4[1]	48.3	20.4	°C/W

[1] Test Condition 1: simulated thermal impedance values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

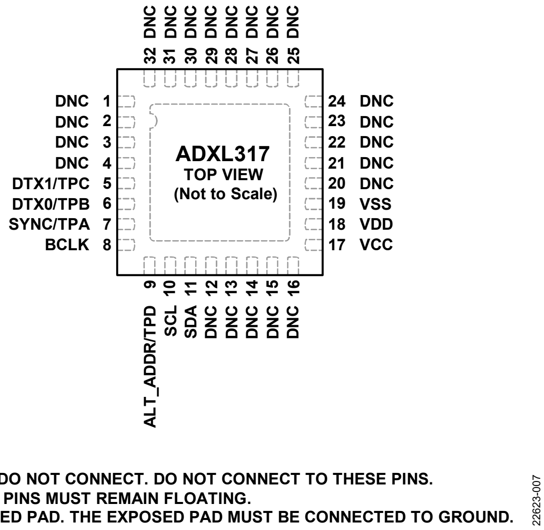


Figure 7. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DNC	Do Not Connect. Do not connect these pins. These pins must remain floating.
5	DTX1/TPC	I²S Data Channel 1/Test Pad C.
6	DTX0/TPB	I²S Data Channel 0/Test Pad B.
7	SYNC/TPA	I²S Sync/Test Pad A.
8	BCLK	I²S Clock.
9	ALT_ADDR/TPD	I²C Address Select/Test Pad D. Connect this pin to ground to set the ADXL317 I²C address to 0x53. Connect this pin to VDD to set the address to 0x1D.
10	SCL	I²C Serial Clock.
11	SDA	I²C Serial Data.
12 to 16	DNC	Do Not Connect. Do not connect these pins. These pins must remain floating.
17	VCC	Supply Voltage.
18	VDD	Internal Regulator Output Voltage. Use this pin for the I²C high reference.
19	VSS	Reference Voltage. Connect this pin to ground.
20 to 32	DNC	Do Not Connect. Do not connect these pins. These pins must remain floating.
	EP	Exposed Pad. The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

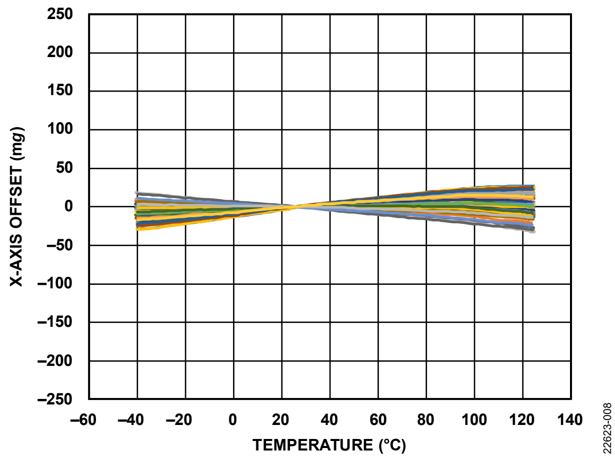


Figure 8. X-Axis Offset vs. Temperature

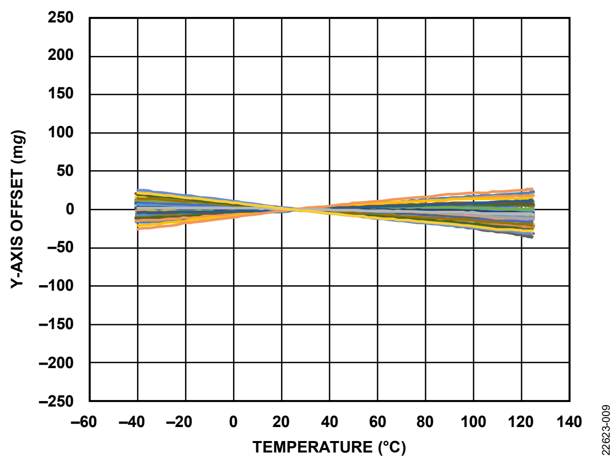


Figure 9. Y-Axis Offset vs. Temperature

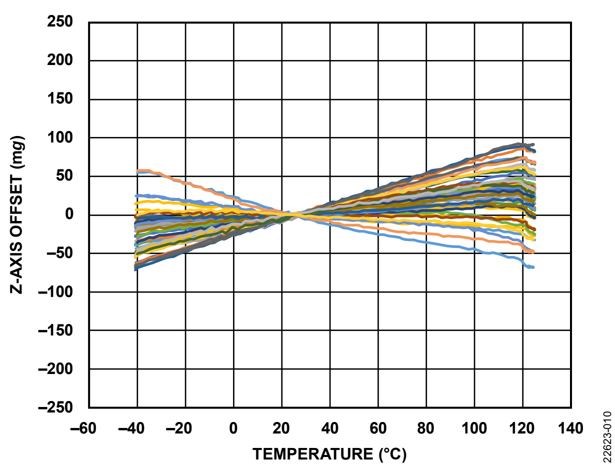


Figure 10. Z-Axis Offset vs. Temperature

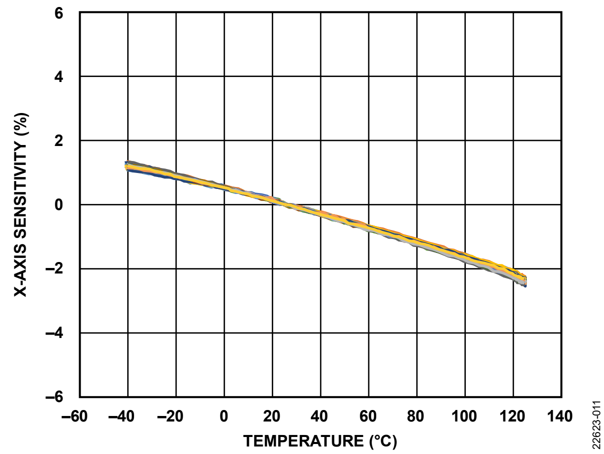


Figure 11. X-Axis Sensitivity vs. Temperature (500 Hz Cascaded Filter)

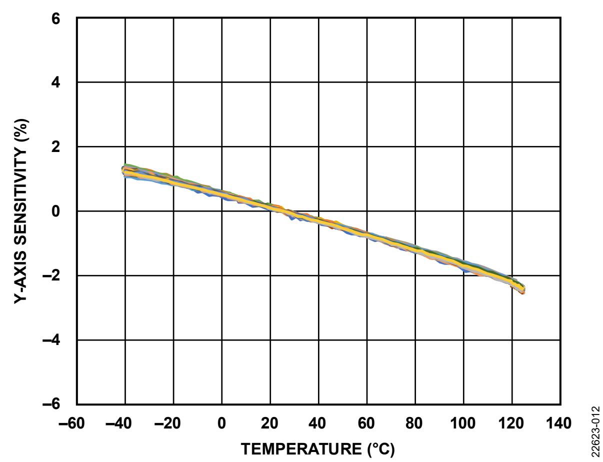


Figure 12. Y-Axis Sensitivity vs. Temperature (500 Hz Cascaded Filter)

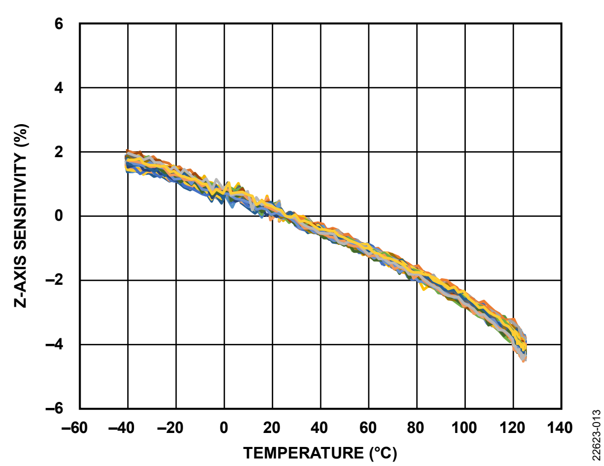


Figure 13. Z-Axis Sensitivity vs. Temperature (500 Hz Cascaded Filter)

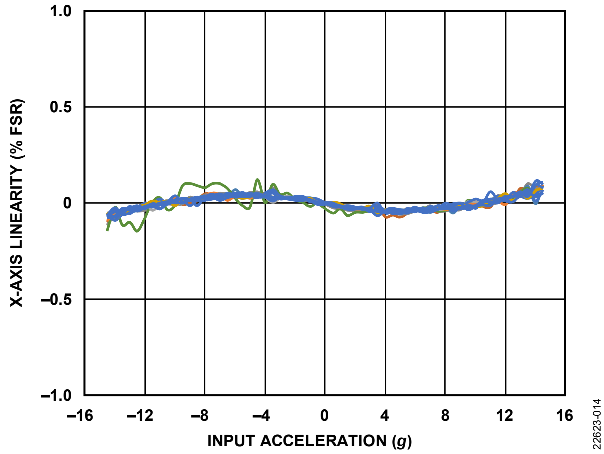


Figure 14. X-Axis Linearity

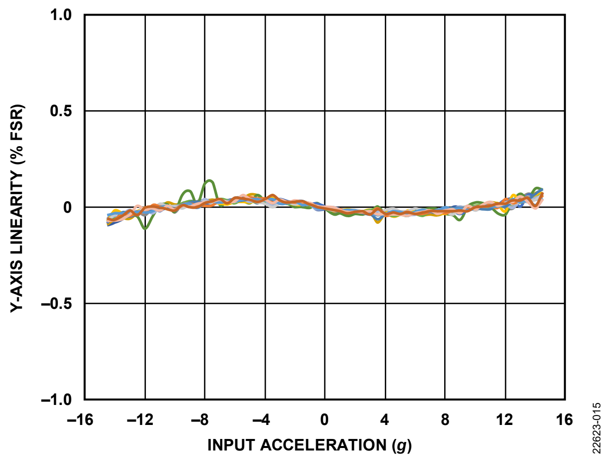


Figure 15. Y-Axis Linearity

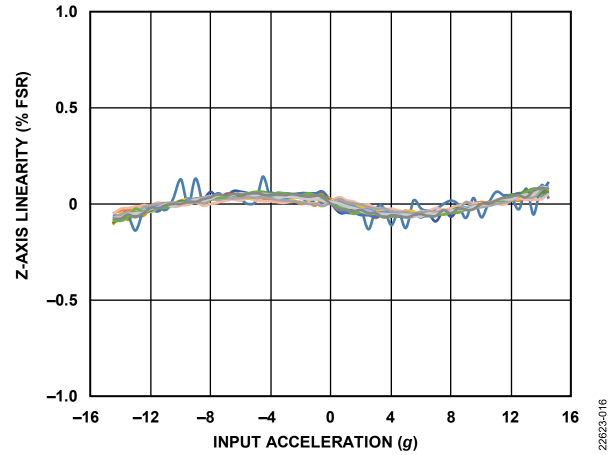


Figure 16. Z-Axis Linearity

TERMINOLOGY

Full-Scale Range (FSR)

The FSR of the ADXL317 is the guaranteed dynamic range at the output of the signal chain. FSR is specified as a minimum value and is guaranteed across all conditions. Acceleration measurement may be possible beyond this minimum value. However, performance characteristics are not guaranteed.

Nonlinearity

Device nonlinearity is the maximum deviation of any sensor data point from the least squares linear fit of the acceleration data set at an equivalent input acceleration level. The acceleration data set can encompass any range of applied acceleration, up to the complete FSR of the ADXL317. Nonlinearity is defined mathematically as

$$\left|\frac{ACC_{MEAS}(g_n) - ACC_{FIT}(g_n)}{FSR}\right| \times 100\%$$

where:

ACC_{MEAS} is the measured acceleration at a defined g_n.
ACC_{FIT} is the predicted acceleration at a defined g_n.
g_n is the input acceleration level.

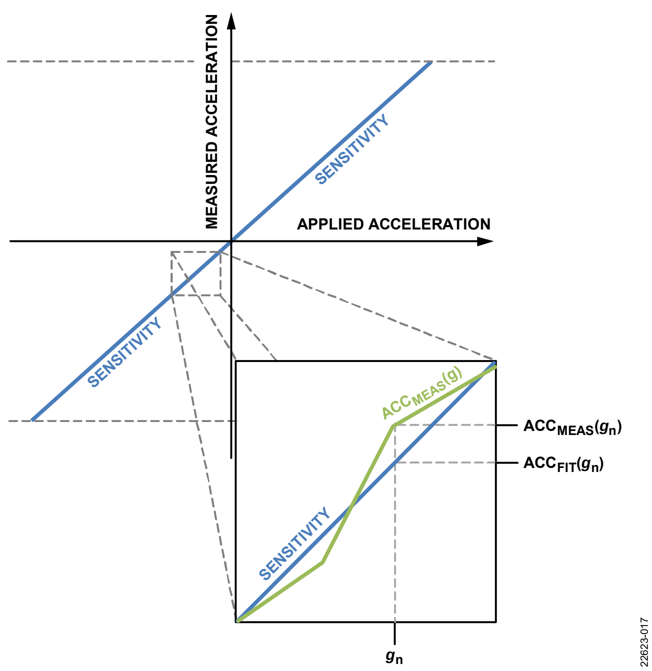


Figure 17. Accelerometer Linearity Error (Not to Scale)

Cross Axis Sensitivity

Cross axis sensitivity is the measured output of the device in response to input stimuli orthogonal to the intended sense axis. It is measured as a percentage of the applied acceleration, as follows:

$$\left[\frac{ACC_{MEAS}(g_x)}{g_y\ (or\ g_z)}\right] \times 100\%$$

where:

$ACC_{MEAS}(g_x)$ is the measured x-axis acceleration.
g_y is the applied y-axis acceleration.
g_z is the applied z-axis acceleration.

The cross axis sensitivity specification accounts for device level cross axis components only. These components include variations in sensor fabrication and the alignment of the sensor to the orthogonal axes of the package (also known as package alignment error). The cross axis specification does not account for system level sources of misalignment (for example, on the PCB or module).

Resonant Frequency (f_o)

f_o is the natural frequency at which the MEMS element has a higher gain when subjected to acceleration events. Input acceleration at this resonant frequency causes the sensor to displace by an amount equal to the applied acceleration multiplied by the quality factor (Q).

The ADXL317 uses different sensor types for the horizontal (x- and y-axes) and the vertical (z-axis) sensing axes. Therefore, the resonant frequency responses of these sensors are not the same.

Quality Factor

The quality factor is a scalar factor that governs the increase or decrease in amplitude of an acceleration signal applied at the resonant frequency of a MEMS element.

Sensitivity

Sensitivity is the slope of the line of best fit for the acceleration transfer function, as measured across the output FSR of the ADXL317. The sensitivity defines the change in output (LSB) per unit change of input (*g*). The inverse, scale factor, is in units of *g*/LSB.

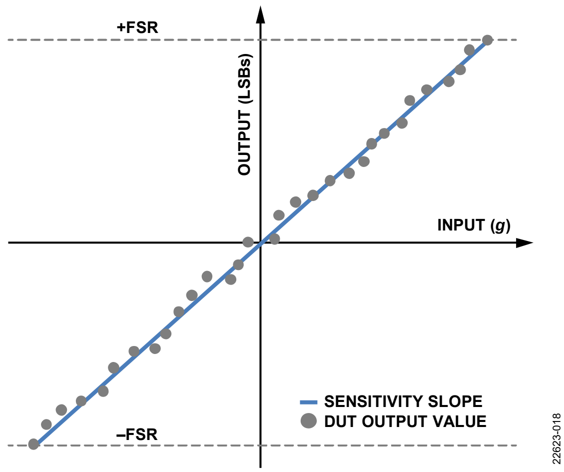


Figure 18. Nominal Sensitivity Slope

Measurement Resolution

Measurement resolution specifies the number of data bits in each acceleration data-word. For example, the 14-bit measurement of the ADXL317 has 16,384 bits of resolution. For an FSR of ±16 *g* (32 *g* total), this resolution yields a sensitivity of 500 LSB/*g* and a scale factor of 2.0 m*g*/LSB.

Zero *g* Bias Error

The zero *g* bias error (also called offset) is any static error term on the output of the ADXL317. Zero *g* bias error is measured as the deviation from 0 *g* with no externally applied acceleration (including gravity).

To more accurately measure offset, take measurements at orientations of +1 *g* and −1 *g* and average the results. Each measurement must be taken over a sufficiently long time window to reduce the influence of external physical stimuli that may exist in the measurement system.

$$Offset = \frac{ACC_{MEAS}(g_{Input} = 1\,g) + ACC_{MEAS}(g_{Input} = -1\,g)}{2}$$

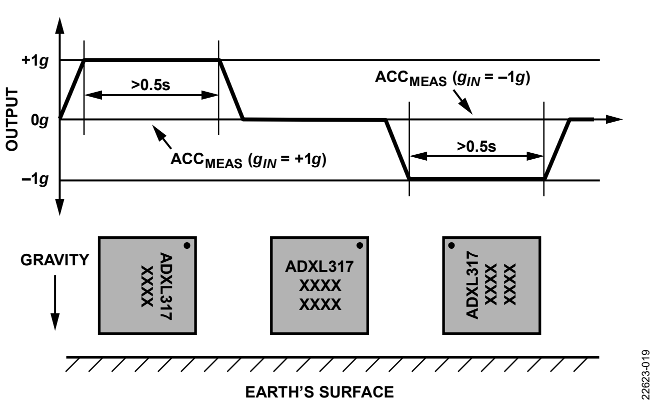


Figure 19. Zero g Bias Error Measurement (X-Axis Example)

Initial Zero *g* Output Deviation

Initial zero *g* output deviation is the error level at ambient conditions, measured immediately after completion of device manufacture. The initial zero *g* output deviation value denotes the standard deviation of the measured offset values across a large population of devices.

Cutoff (−3 dB) Frequency

For applied ac acceleration, the cutoff (−3 dB) frequency (also referred to as bandwidth) is the frequency at which the input stimulus is attenuated in amplitude by 29.3% (1 – √2/2) at the output of the signal chain. The −3 dB corner is set according to the low-pass cascaded integrated comb (CIC) filter and the low-pass infinite impulse response (IIR) filter setting as selected by the user. A high-pass filter can also be turned on by the user but is disabled by default. All other signal chain elements have an appreciably high bandwidth and are not significant contributors to the cutoff frequency.

Noise Density

Noise density is a measure of the inherent noise in the ADXL317 and is a combination of all internal noise sources. This density is fixed by the architecture of the device and is independent of bandwidth. See the Filtering: Noise and Latency Considerations section for more information on noise density.

Output Noise

Output noise is the realized noise in reported measurements. Whereas noise density expresses the inherent noise in the device, output noise is the union of density and bandwidth. Filters with lower bandwidths provide more aggressive filtering and, therefore, greater noise reduction than filters with higher bandwidths.

Self Test Output Change

The sensor self test is a diagnostic test. In this test, the sensor proof mass is deflected by an electrostatic force, thereby creating a measurable output change. For a self test routine to be evaluated properly, the change in output must be measured before and after applying the self test force. If this change is within the specified values shown in Table 1, it is considered successful.

The ADXL317 features positive, negative, and ac self test routines. AC self test toggles between positive and negative self test at a rate of 100 Hz. See the Using Self Test section for more information.

Operating Voltage (V_{CC})

Operating voltage is the necessary voltage on the VCC pin for proper operation. Any voltages on the VCC pin outside the specified minimum and maximum values may cause the device to malfunction.

Regulated I/O Voltage (V_{DD})

Regulated I/O voltage is the voltage reference for both on-chip digital communication interfaces: I^2S and I^2C. Operating these interfaces at other values from the regulated 1.8 V may result in miscommunication between the ADXL317 and master device.

Quiescent Supply Current

Quiescent supply current is the current draw of the device when no data is being transmitted and the device is operating within the minimum/maximum supply voltage (VCC).

Turn On Time

Turn on time specifies the necessary time needed for the regulated I/O voltage (VDD) to settle to the final value. This settling indicates that the nonvolatile memory (NVM) contents have been loaded and have taken effect. Following a hardware reset, the user must wait for the specified turn on time before performing reads from or writes to the ADXL317.

Inter-IC Sound (I^2S) Protocol

The I^2S protocol is a set of specifications for the transmission of digital audio signals along a bus. This bus consists of four signals: serial clock (BCLK), synchronization signal (SYNC), and two serial data channels (DTX[1:0]). The ADXL317 acts as a slave transmitter in this protocol.

Inter-IC (I^2C) Protocol

The I^2C protocol is a set of specifications for the transmission of data between multiple ICs along only two wires: serial data (SDA) and serial clock (SCL). These lines are shared between all devices on the bus. Each device on the bus is software addressable via a unique address.

Latency

Latency is the time between an acceleration event hitting the ADXL317 and the measurement being available on the output channel. There are two components that define the total latency of the signal chain:

- Fixed latency imposed by the sense electronics and ADCs.
- Latency created by the adjustable low-pass (CIC and IIR) and high-pass filters.

These two components must be added together to determine the total latency of the ADXL317. Filter latency is dependent on bandwidth, with higher bandwidths requiring less time for the input signal to appear on the output of the device.

THEORY OF OPERATION

OVERVIEW

The ADXL317 is a complete, 3-axis acceleration measurement system designed to interface directly with the Analog Devices line of A^2B transceivers, making the ADXL317 ideal for automotive noise cancellation applications. The wide range of selectable bandwidth settings, low output noise, and low latency make the ADXL317 appropriate for wideband noise sensing and adaptive suspension control.

The ADXL317 treats all three sensor channels independently. There are three analog channels in the ASIC die with separate analog signal processing for each accelerometer axis. Each analog channel is then sampled by separate digital signal processing blocks that process the samples for the common communications interface block. Therefore, if one sensor channel fails, transmission of acceleration data continues for the other axes.

MECHANICAL DEVICE OPERATION

The ADXL317 contains three independent sensors, one for each axis of sensitivity. Each acceleration sensor is a polysilicon, surface micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent, fixed plates and plates attached to the moving mass. Acceleration deflects the beam and unbalances the differential capacitor, resulting in a sensor output with amplitude proportional to acceleration. Phase sensitive demodulation determines the magnitude and polarity of the acceleration.

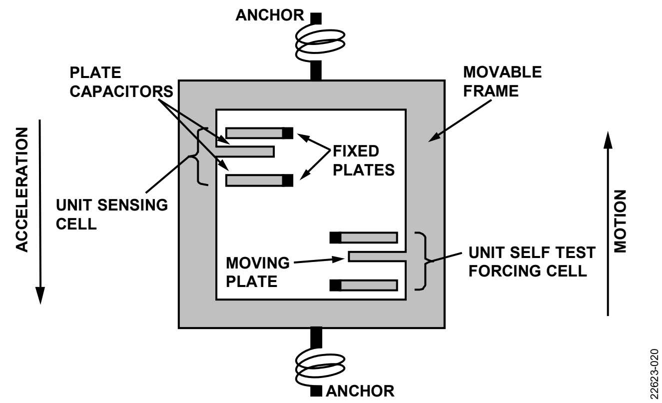


Figure 20. Simplified View of One Sensor During Acceleration

NOISE AND LATENCY TRADE-OFF

The ADXL317 offers several options for controlling the trade-off between output noise and latency (or delay) to accommodate a wide range of system requirements.

The ADXL317 features two cascaded, low-pass digital filters: a two-pole CIC filter and a single-pole IIR filter, which remove unwanted high frequency content from the signal. More aggressive filtering (that is, using a filter with a lower cutoff frequency) introduces more delay to the signal chain, but decreases output noise. Conversely, less aggressive filtering results in more output noise but less delay. The optimal compromise between these two parameters depends on system implementation.

The ADXL317 features four settings for each filter, for a total of 16 combinations. The noise and delay associated with a subset of these settings are shown in Table 7. For more information, see the Filtering: Noise and Latency Considerations section.

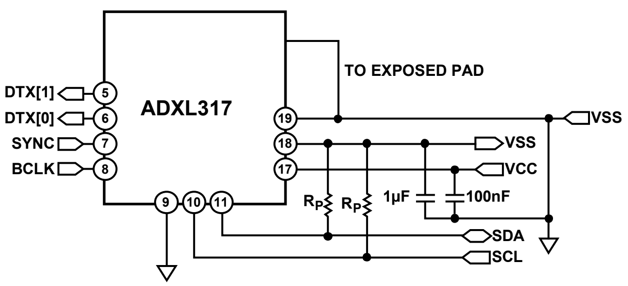
Table 7. Output Noise and Delay vs. Filter Cutoff Frequency (T_A = 25°C, V_{CC} = 3.3 V)

	Output Noise (m*g* rms)		
Cutoff Frequency (Hz)	X-/Y-Axes	Z-Axis	Delay (µs)
506	2.5	4	585
1012	5.5	7	291
2025	22.5	30	144
4051	85	120	70.9

APPLICATIONS INFORMATION

APPLICATION CIRCUIT

Figure 21 shows the recommended application circuit for the ADXL317. The operating power pin, VCC (Pin 17), requires a 100 nF bypass capacitor to ground (VSS, Pin 19) placed as close as possible to the pin. The voltage regulator output pin, VDD (Pin 18), requires a 1 µF capacitor. The two I^2C lines, SCL (Pin 10) and SDA (Pin 11), each require a pull-up resistor to VDD. The value of these resistors is dependent on bus capacitance. Refer to *UM10204 I^2C-bus specification and user manual*, Rev. 6—4 April 2014 (NXP Semiconductor) when selecting pull-up resistor values to ensure proper operation. The exposed pad on the bottom of the package must be connected to ground.



NOTES
1. ALT_ADDR MAY BE GROUNDED OR CONNECTED TO VDD. SEE THE I^2C INTERFACE SECTION FOR DETAILS.
2. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO GROUND.

22623-021

Figure 21. Recommended Application Circuit

POWER

The ADXL317 has a single power input pin, VCC, which operates at a nominal voltage of 3.3 V. An internal regulator steps this voltage down to 1.8 V. The VCC pin must be properly bypassed, as shown in Figure 21, to remove ac fluctuations from the power supply.

VDD is the output of the internal voltage regulator, which holds the pin at a constant 1.8 V. This pin must also be decoupled from ac noise for stability. VDD must be used as the pull-up voltage for the I^2C lines (SCL and SDA).

INTERFACING WITH A^2B TRANSCEIVERS

The ADXL317 is designed to interface directly with the AD2425W, or with an I^2S capable A^2B transceiver from Analog Devices. The connection between the ADXL317 and the AD2425W is shown in Figure 22. A generic A^2B transceiver can be used. Refer to the appropriate transceiver data sheet for additional details.

Power

The ADXL317 operates as a phantom powered slave device and, therefore, must derive power directly from the A^2B transceiver. Connect one of the VOUT pins (3.3 V) from the transceiver to VCC on the ADXL317, being sure to properly decouple the supply on both ends.

Communications

Directly connect the BCLK pin and the SYNC pin between the ADXL317 and the A^2B transceiver. The DTX1 and DTX0 pins on the ADXL317 are outputs (data transmit) and must be connected to the corresponding DRX0 and DRX1 (data receive) pins on the transceiver. Adding small (~100 Ω) series resistors to these four lines may improve electromagnetic interference (EMI) performance. The exact value of these resistors depends on the observed EMI characteristics of the system.

SCL and SDA must also be connected directly between the two devices, taking care to choose appropriate pull-up resistors. Use VDD as the pull-up voltage for I^2C.

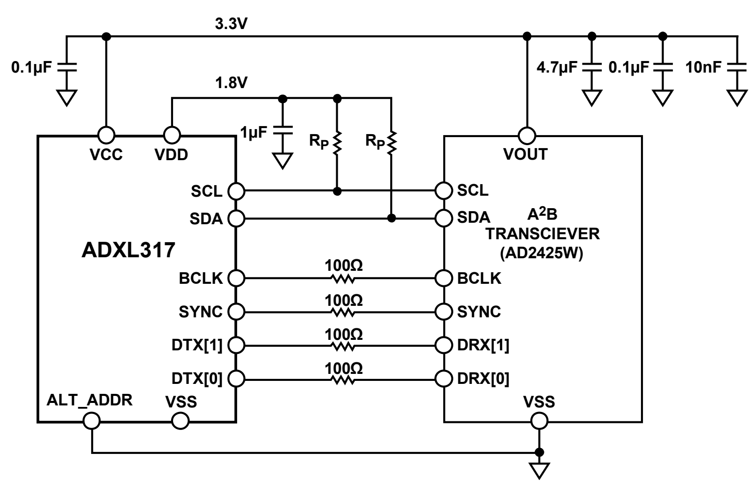


Figure 22. ADXL317 to A^2B Transceiver Connection Diagram

USING SELF TEST

The ADXL317 features a flexible self test routine to evaluate the condition of the sensors. Self test can be activated in one of the three following modes:

- Positive self test mode. In this mode, a positive dc excitation is applied to the sensor along the desired axis. This excitation is approximately 3.6 *g* for the x- and y-axes, and 6.6 *g* for the z-axis, plus any excitation from the environment.
- Negative self test mode. In this mode, a negative dc excitation is applied to the sensor along the desired axis. This excitation is approximately −3.6 *g* for the x- and y-axesm and −6.6 *g* for the z-axis, plus any excitation from the environment.
- AC self test mode. In this mode, a 100 Hz square wave is applied to the sensor along the desired axis. The upper and lower bounds of this square wave are equal to the values of the positive and negative self tests, respectively.

When first powering on the ADXL317, the user must use the positive and negative dc self test or the ac self test to achieve an accurate understanding of device health. Each axis is capable of controlling its self test independently of the other axes, resulting in many combinations of self test settings. These settings are configured in the X_ST, Y_ST, and Z_ST registers and the corresponding x_ST_AC, x_ST_POS, and x_ST_NEG bits. Although any number of these bits for a given axis can be asserted simultaneously, only one such force can be applied to each axis at a time. If multiple bits are asserted, self test is disabled. The mapping of all possible settings of these bits and the resultant self test force is shown in Table 8.

Table 8. Self Test Settings Combinations

x_ST_AC	x_ST_POS	x_ST_NEG	Self Test Force
0	0	0	Self test is disabled
0	0	1	Negative self test
0	1	0	Positive self test
0	1	1	Self test is disabled
1	0	0	AC self test
1	0	1	Self test is disabled
1	1	0	Self test is disabled
1	1	1	Self test is disabled

When a self test force is exerted along any axis, the value returned from the sensor is additive with any external force applied to the accelerometer, as shown in Figure 25. In this graphic, the accelerometer experiences a sine wave motion with an amplitude of 4 *g*. For simplicity, assume all axes receive the same input. The resultant measurement returned from the ADXL317 after applying self test is the sine wave added to the self test excitation.

Be sure to account for gravity in self test measurements. For example, applying positive self test to the z-axis with the accelerometer sitting flat on a table (that is, with the z-axis aligned with gravity) results in acceleration of 6.6 *g* from self test, plus 1 *g* from gravity, for a total of 7.6 *g*. Therefore, self test is best performed in the absence of any external acceleration, other than static, known sources like gravity that can be easily calibrated out.

Taking an accurate self test measurement involves a few steps. For the two dc self test modes, the following routine must be followed to accurately assess the results of self test:

1. Ensure all self test functionality is disabled. That is, set the X_ST, Y_ST, and Z_ST registers (Address 0x84, Address 0x86, and Address 0x88, respectively) to 0x00.
2. Read acceleration data for the x-axis. It is recommended to take an average of 25 ms to reduce the influence of noise in the measurement.
3. Activate self test by asserting the X_ST_POS bit and wait for the output to transition to the maximum value.
4. Read acceleration data again for 25 ms.
5. Subtract the data collected in Step 2 from the data collected in Step 4 to determine the magnitude of the self test delta (STΔ).
6. Deactivate the X_ST_POS bit, activate the X_ST_NEG bit, and wait for the output to transition to the minimum value.
7. Read acceleration data again for 25 ms.
8. Compare the positive and negative STΔ magnitudes to the limits in Table 1. If both magnitudes are within the minimum and maximum specifications, the device passed the self test. Otherwise, the device failed and must be flagged for further investigation.
9. Repeat Step 1 to Step 8 for the y-axis and z-axis, sequentially.

Self test must be activated one channel at a time, meaning that Step 1 to Step 9 must be repeated for the x-, y-, and z-axis channels, sequentially.

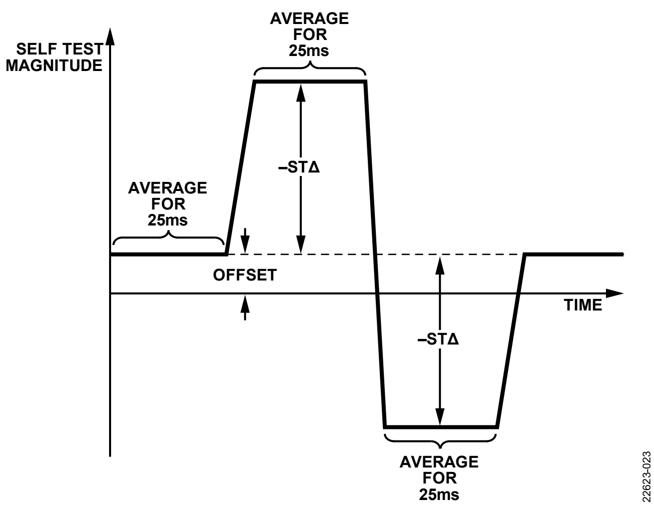


Figure 23. DC Self Test Measurement

The same steps can be followed when taking an ac self test measurement. However, greater care must be taken in the timing between measurements. Additionally, it may be helpful to examine the frequency domain of the signal to determine if the sensor and signal chain are behaving as desired. For the ac self test mode, the following routine must be followed to accurately assess the results of self test:

1. Ensure all self test functionality is disabled. That is, set the X_ST, Y_ST, and Z_ST registers (Address 0x84, Address 0x86, and Address 0x88, respectively) to 0x00.
2. Read acceleration data for the x-axis. It is recommended to take an average of 25 ms to reduce the influence of noise in the measurement.
3. Activate self test by asserting the X_ST_AC bit.
4. Read acceleration data for at least 40 ms with at least a 1 kHz data rate.
5. Determine the STΔ magnitudes using the procedure shown in Figure 24.
6. Compare the positive and negative STΔ magnitudes to the limits shown in Table 1. If both magnitudes are within the minimum and maximum specifications, the device passed the self test. Otherwise, the device failed and must be flagged for further investigation.
7. Repeat Step 1 to Step 6 for the y-axis and z-axis, sequentially.

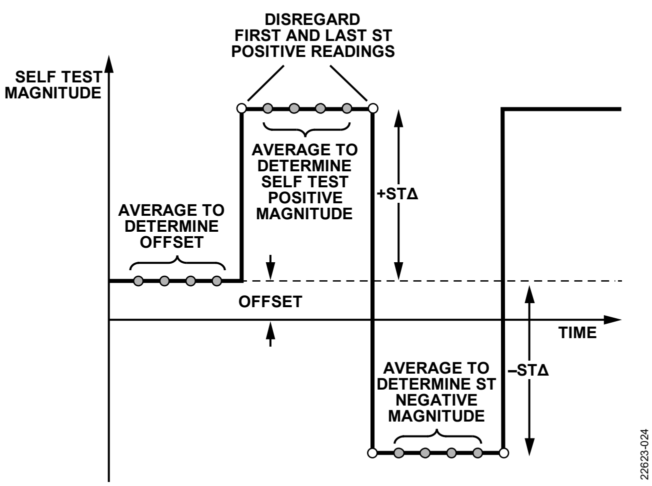


Figure 24. AC Self Test Measurement

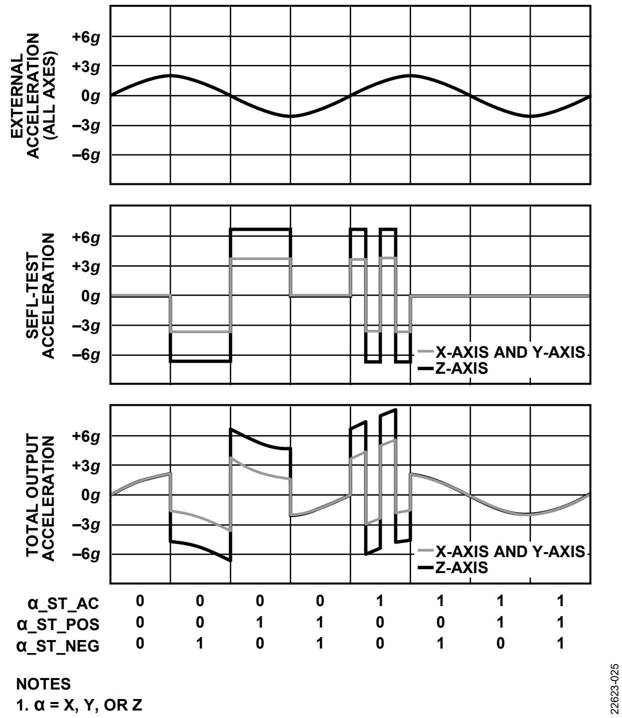


Figure 25. Self Test Settings and Resulting Output in Presence of 12.5 Hz Sinusoidal Input Acceleration

SERIAL COMMUNICATIONS

The ADXL317 communicates via both 4-wire I²S and 2-wire I²C digital communication interfaces. The I²S bus is the primary means of outputting data, and the I²C bus configures the register settings. In both cases, the ADXL317 operates as a slave device, receiving commands and responding with requested data. These two ports operate independently and use separate pins. Therefore, these ports can be used simultaneously.

I²S/TDM INTERFACE

The ADXL317 constantly streams data out of the I²S port. This protocol is suitable for obtaining high speed, synchronous accelerometer data. The ADXL317 operates at a clock speed of 3.072 MHz or 6.144 MHz (typical) with a frame frequency of 48 kHz. The device supports 16-bit TDM4 and TDM8, as well as 32-bit I²S/TDM2 and TDM4.

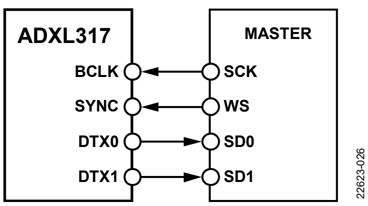


Figure 26. I²S/TDM Wiring Diagram

Signals

The ADXL317 uses a 4-wire I²S interface, comprising one continuous serial clock, one synchronization signal, and two serial data channels. There are numerous naming conventions for these channels. The ADXL317 uses the same terminology and symbols as the A²B family of transceivers from Analog Devices. See Table 9 for a comparison of the names used in the I²S specification against the names used in the ADXL317.

Table 9. I²S Signal Names

I²S Specification		ADXL317	
Full Name	**Symbol**	**Full Name**	**Symbol**
Continuous Serial Clock	SCK	Bit clock	BCLK
Word Select	WS	Sync	SYNC
Serial Data	SD	Data transmit	DTX

Bit Clock (BCLK)

The bit clock (BCLK) line controls the timing of transactions between the master (A²B transceiver or other controller) and slave (ADXL317). This clock must be supplied externally to the BCLK pin (Pin 8) at a rate of either 3.072 MHz or 6.144 MHz. The incoming clock frequency must be specified in the CLOCK_RATE register (Address 0x83).

The ADXL317 has no internal clock, and all timing is derived from BCLK. BCLK must be running at all times for the ADXL317 to operate, even when using I²C to read and/or write registers.

Sync (SYNC) Signal

The SYNC line selects the channel being transmitted. By default, with SYNC high (set to 1), the right channel is transmitting. With SYNC low (set to 0), the left channel is transmitting (in TDM2 mode). This behavior can be reversed by asserting the INV bit in the I2S_CFG0 register (Address 0x81). SYNC demarcates the boundary between the first and second halves of the frame.

The value of SYNC is latched on the rising edge of BCLK as long as INV (Address 0x81, Bit 7) = 0. After SYNC changes value, the timing of the transmission of the MSB of the data depends on the value of the early bit in the I2S_CFG0 register. If early = 0, the SYNC pin changes in the same cycle as the MSB of the first data channel. If early = 1, the SYNC pin changes one cycle before the MSB of the first data channel.

By default, the SYNC pin changes value on the rising edge of BCLK. This change can be altered to occur on the falling edge by asserting the TXBCLKINV bit in the I2S_CFG1 register.

Data Transmit (DTX) Signal

The data transmit (DTX) lines send data from the ADXL317 to the master device. Data is transmitted in twos complement format with the most significant bit (MSB) first. The position of the LSB in the transaction is dependent on the word length, as defined in the Packet Format section.

Data can be sent over one or both of the DTX pins, depending on the values of the TX0EN and TX1EN bits in the I2S_CFG1 register, as well as the operating mode.

Packet Format

The ADXL317 features four packet formats, depending on the input clock (BCLK) frequency and system requirements. At 3.072 MHz, 32-bit I²S/TDM2 and 16-bit TDM4 are supported. At 6.144 MHz, 32-bit TDM4 and 16-bit TDM8 are supported. Note that 32-bit I²S/TDM2 mode requires two data pins, whereas the other three modes require only one.

Table 10. Required BCLK Frequencies for All Supported Output Formats

Output Format	16-Bit Mode BCLK Frequency	32-Bit Mode BCLK Frequency	No. of Pins
I²S/TDM2	Not applicable	3.072 MHz	2
TDM4	3.072 MHz	6.144 MHz	1
TDM8	6.144 MHz	Not applicable	1

In I²S/TDM2 mode, the DTX0 pin transmits data from the x- and y-axes. The DTX1 pin transmits z-axis data followed by all zeros in the second half of the transmission. BCLK must be running at 3.072 MHz, and each axis comprises 32 bits.

In TDM4 mode, data from all three axes is sent over a single pin, whereas the other pin remains at zero during the entire transaction. Each axis comprises 16 bits with BCLK running at 3.072 MHz and 32 bits at 6.144 MHz.

In TDM8 mode, the frame is further divided in eight segments. The first three segments on one pin contain data from all three axes, and the remaining segments are held at zero. BCLK must be running at 6.144 MHz, and each axis comprises 16 bits.

The frame rate for all transactions is 48 kHz, which translates to 64 clock cycles at 3.072 MHz or 128 cycles at 6.144 MHz. The number of channels in each frame is always a power of two (two, four, or eight). The ADXL317 has three channels, one for each axis. Therefore, all channels beyond the third are set entirely to 0. Table 11 through Table 14 shows how these channels align within each frame, and Figure 27 through Figure 30 show how the various I^2S configuration settings affect the timing of each transaction. Note that these figures are not to scale, and clock rates differ.

For formats that only require one data pin, the TX0EN bit and the TX1EN bit in the I2S_CFG1 register control which pin is actively outputting data. The inactive pin is pulled low during the entirety of the transaction.

Table 11. Two-Pin I^2S/TDM2 Packet Format (3.072 MHz BCLK, 32-Bit Data, TX0EN = 1, TX1EN = 1)

DTX0	DTX1
X-axis data (32-bit)	Z-axis data (32-bit)
Y-axis data (32-bit)	0x00000000

Table 12. One-Pin TDM4 Packet Format (3.072 MHz BCLK, 16-Bit Data, TX0EN = 1, TX1EN = 0)

DTX0	DTX1
X-axis data (16-bit)	0x0000
Y-axis data (16-bit)	0x0000
Z-axis data (16-bit)	0x0000
0x0000	0x0000

Table 13. One-Pin TDM4 Packet Format (6.144 MHz BCLK, 32-Bit Data, TX0EN = 1, TX1EN = 0)

DTX0	DTX1
X-axis data (32-bit)	0x00000000
Y-axis data (32-bit)	0x00000000
Z-axis data (32-bit)	0x00000000
0x00000000	0x00000000

Table 14. One-Pin TDM8 Packet Format (6.144 MHz BCLK, 16-Bit Data, TX0EN = 1, TX1EN = 0)

DTX0	DTX1
X-axis data (16-bit)	0x0000
Y-axis data (16-bit)	0x0000
Z-axis data (16-bit)	0x0000
0x0000	0x0000
0x0000	0x0000
0x0000	0x0000
0x0000	0x0000
0x0000	0x0000

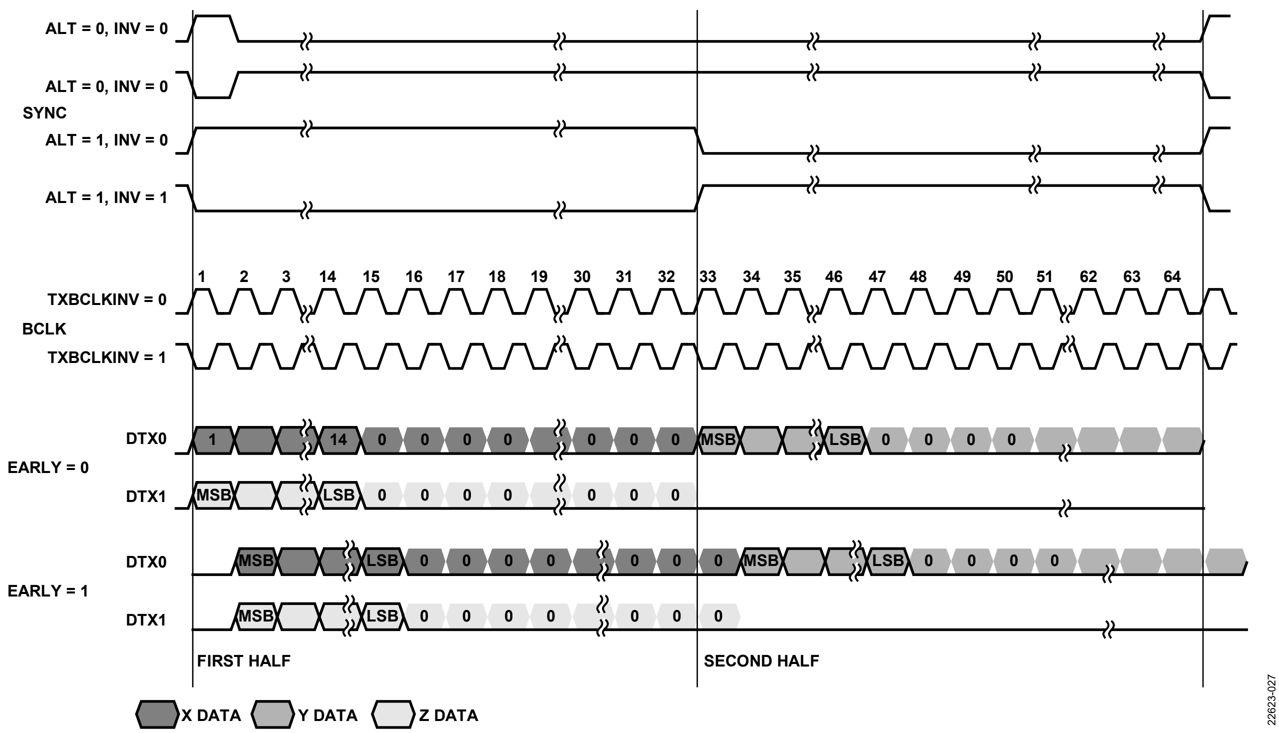


Figure 27. 3.072 MHz I²S/TDM2 Timing (32-Bit Data)

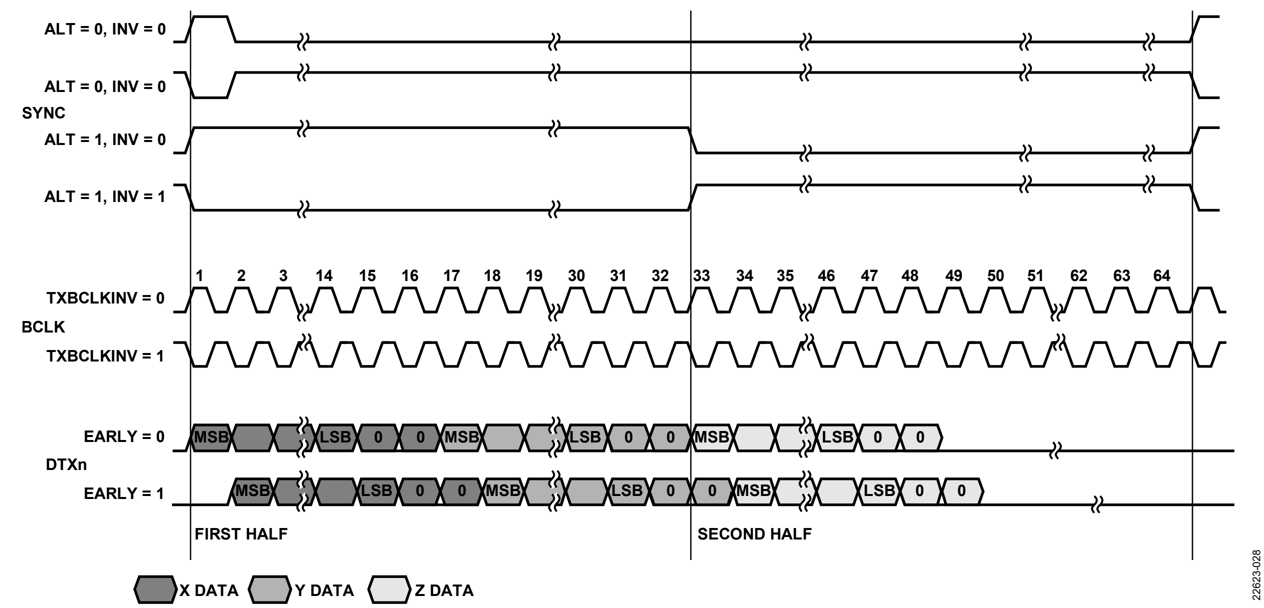


Figure 28. 3.072 MHz TDM4 Timing (16-Bit Data)

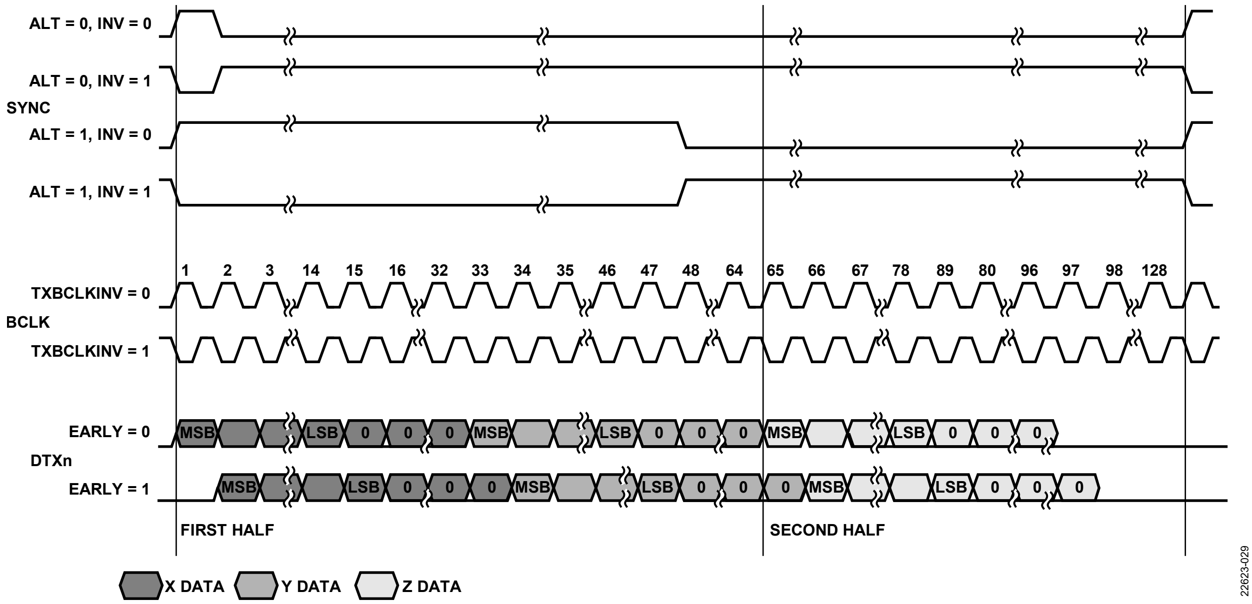


Figure 29. 6.144 MHz TDM4 Timing (32-Bit Data)

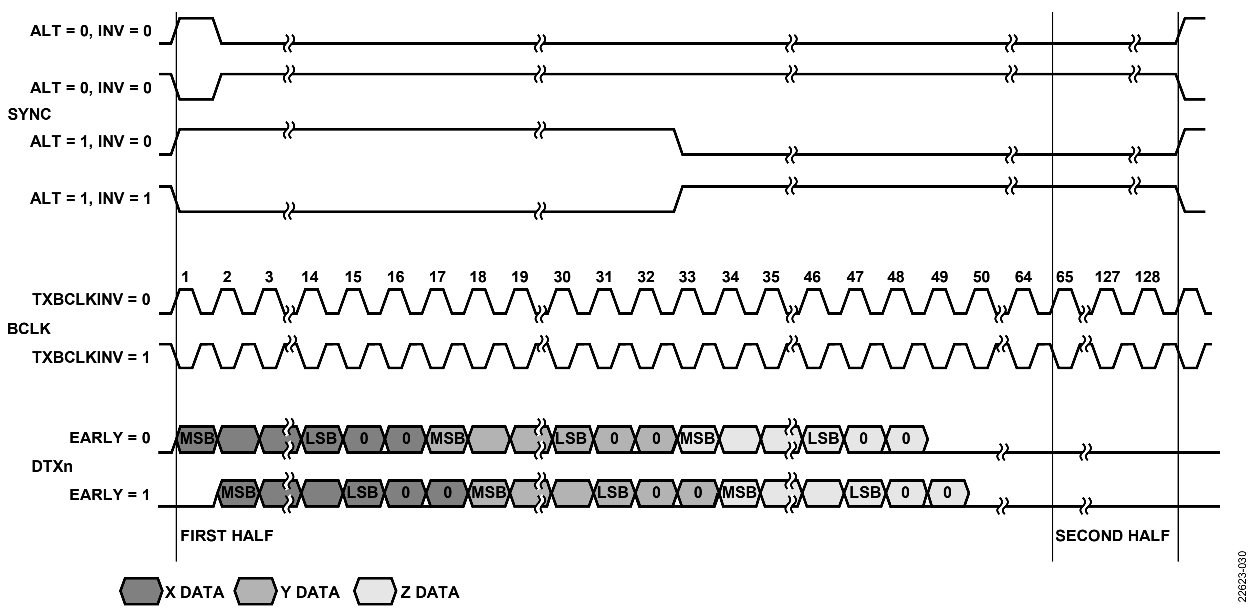


Figure 30. 6.144 MHz TDM8 Timing (16-Bit Data)

I²C INTERFACE

The ADXL317 features a 2-wire I²C interface through which the user performs register reads and writes. These reads and writes configure the various device settings. The I²C interface conforms to *UM10204 I²C-bus specification and user manual*, Rev. 6—4 April 2014, available from NXP Semiconductor, and supports standard data transfer mode at 100 kHz if the bus parameters shown in Table 2 and Table 3 are met. The SCL and SDA lines require pull-up resistors (R_P). Refer to *UM10204 I²C-bus specification and user manual*, Rev. 6—4 April 2014 (NXP Semiconductor) when selecting pull-up resistor values to ensure proper operation. Single- and multi-byte reads and writes are supported, as shown in Figure 32. When communicating with the ADXL317 via I²C, BCLK must be provided with a valid clock signal.

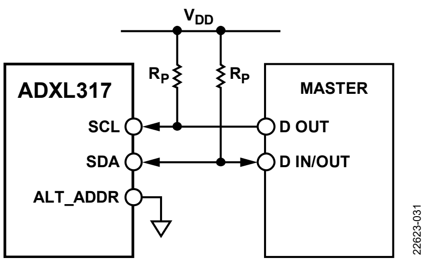


Figure 31. I²C Wiring Diagram

Signals

SCL

SCL is the serial clock input to the ADXL317. SCL is generated by the master device and requires a pull-up resistor.

SDA

SDA is the serial data line. SDA is bidirectional, with the ADXL317 and master device each controlling the line during different slices of each transaction. SDA also requires a pull-up resistor.

Definitions

A start condition is a transition of SDA from high to low while SCL is high.

A stop condition is a transition of SDA from low to high while SCL is high.

An acknowledge condition (ACK) occurs when the transmitter releases the SDA line during the acknowledge clock pulse (the ninth bit following and byte), and the receiver pulls SDA low during the entire high period of this clock pulse. This is denoted as A in the timing diagrams that follow.

A no acknowledge condition (NACK) is similar to an acknowledge, but the receiver pulls SDA high during the entire high period of the acknowledge clock pulse. This is denoted as NA in the timing diagrams that follow.

The ADXL317 device address depends on the wiring of the ALT_ADDR pin. With this pin grounded, the address is 0x53. With this pin pulled to VDD, the address is 0x1D. All bytes are transmitted MSB first.

Register Writes

All commands begin with the master transmitting a start condition followed by the ADXL317 device address and the R/W bit. Because both reads and writes require writing the desired register address to the device, the R/W bit is always low (denoting a write condition) in this first portion of the communication. The ADXL317 responds to this request with an acknowledge condition. Next, the master transmits the address of the register to be written. The ADXL317 again responds with an acknowledge. The master then transmits the data to be written to the specified register, and the ADXL317 responds one last time with an acknowledge. Finally, the transaction is terminated with the transmission of a stop condition from the master.

Multibyte writes are also supported. To write to multiple consecutive registers, the master continues to transmit data bytes between each acknowledge condition. The ADXL317 autoincrements the address and writes each byte to the subsequent register. Only after a stop condition is received does the ADXL317 stop writing.

See Figure 32 for a visual representation of the transactions described in this section. See Figure 2 and Figure 3 for waveforms.

Register Reads

Reading from a register involves the same first few steps as writing to a register. The master sends a start condition followed by the ADXL317 device address and the R/W bit low. After the ADXL317 responds with an acknowledge, the master transmits the address of the register to read, to which the ADXL317 again responds with an acknowledge.

To differentiate this command from a register write, the master next transmits a repeated start command, followed immediately by the ADXL317 device address, plus the R/W bit high to denote a read condition. The ADXL317 responds to this request with an acknowledge, followed by the contents of the desired register. The master responds to the receipt of this data with a no acknowledge to prevent the ADXL317 from responding further, followed by a stop condition to terminate the transaction.

Multibyte reads are also supported. To read from multiple consecutive registers, the master simply responds with an acknowledge instead of a no acknowledge following the receipt of data. The ADXL317 continues to auto-increment the register address and transmit the contents of each subsequent register until a no acknowledge and stop are received.

See Figure 32 for a visual representation of these transactions and Figure 4 and Figure 5 waveforms.

Invalid Registers

The user accessible registers are located at Address 0x00 to Address 0x01 and Address 0x80 to Address 0x8F. See the Register Map section for details regarding the functionality of these registers. Attempting to read a register outside of these ranges returns all zeros. However, the device responds to the request with an acknowledge condition, which applies to both single- and multi-byte transactions.

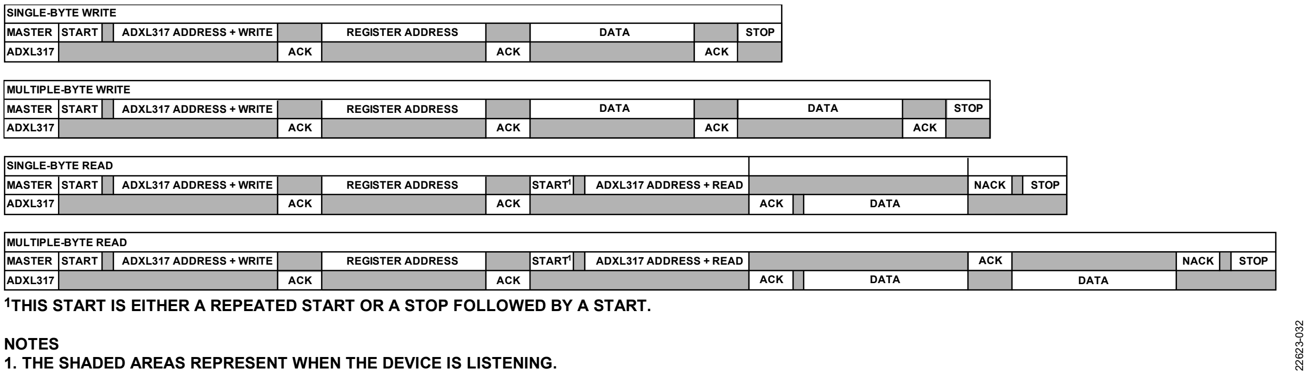


Figure 32. I²C Communication Format

FILTERING: NOISE AND LATENCY CONSIDERATIONS

There are several filters in the signal chain of the ADXL317 that can be independently controlled. These filters are as follows:

- Low-pass CIC filter. This filter is always enabled, and the corner frequency can be set to 7.66 kHz, 3.83 kHz, 1.91 kHz, or 957 Hz.
- Low-pass IIR filter. This filter can be turned on or off and is enabled by default. The corner frequency can be set to 5.00 kHz, 2.50 kHz, 1.25 kHz, or 625 Hz.
- High-pass filter. This filter can be turned on or off and is disabled by default. The corner frequency can be set to 29.8 Hz, 7.46 Hz, 1.85 Hz, or 0.46 Hz.

By combining these settings, a wide variety of filter characteristics can be achieved. In addition to the nominal 4 kHz, 2 kHz, 1 kHz, and 500 Hz settings, obtained by matching the values in the x_IIR_CORNER and x_CIC_CORNER_LPF fields, 12 other settings are possible (see Table 15).

In general, a higher cutoff (−3 dB) frequency results in less delay but more noise, whereas a lower cutoff frequency results in less noise but more delay. These trends are shown in Figure 33 through Figure 36. This phenomenon is not necessarily always the case. Therefore, take care when choosing filter settings to achieve the desired trade-off between noise and latency.

The resonant frequency of the sensor has an impact on the total signal chain response. Filter settings near resonance are shifted to higher frequencies, resulting in higher effective bandwidths. Also, the front-end electronics add a constant delay of approximately 14 μs for the x- and y-axes, and 20 μs for the z-axis.

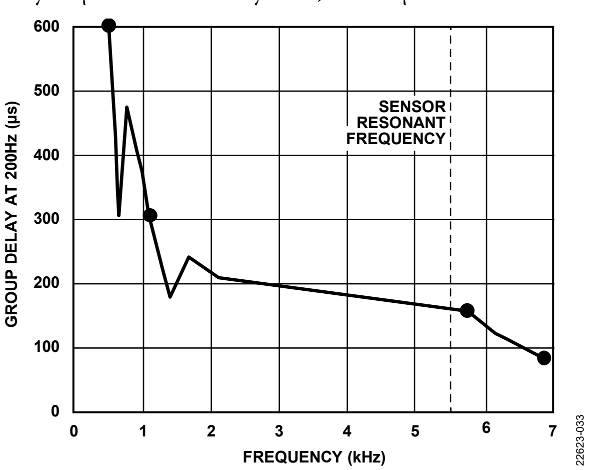


Figure 33. X- and Y-Axes Group Delay vs. Frequency for All Filter Settings (See Table 15 for Specific Items in This Figure Marked with Circles)

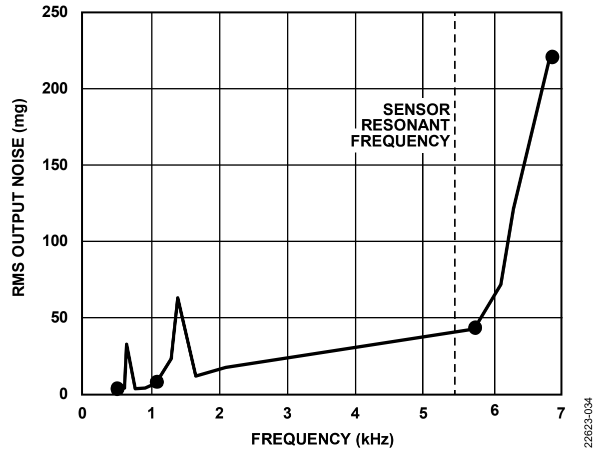


Figure 34. X- and Y-Axes Noise vs. Frequency for All Filter Settings (See Table 15 for Specific Items in This Figure Marked with Circles)

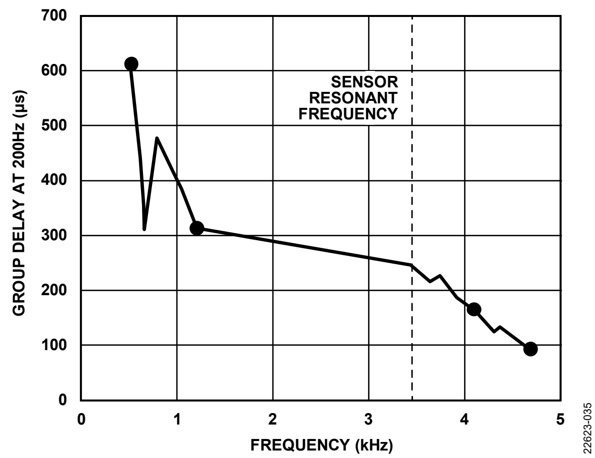


Figure 35. Z-Axis Group Delay vs. Frequency for All Filter Settings (See Table 15 for Specific Items in This Figure Marked with Circles)

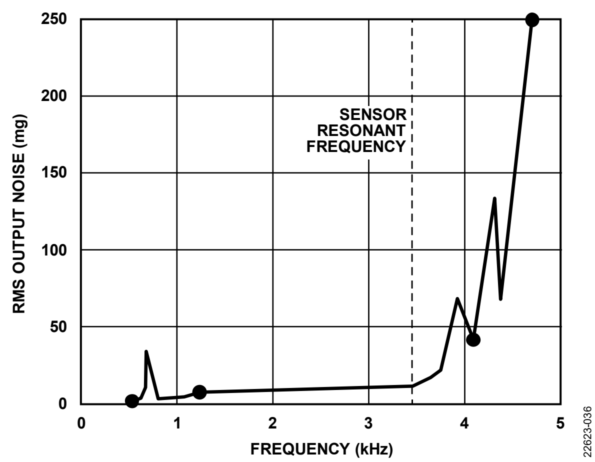


Figure 36. Z-Axis Noise vs. Frequency for All Filter Settings (See Table 15 for Specific Items in This Figure Marked with Circles)

Table 15. Low-Pass Filter Settings Combinations (X- and Y-Axes)[1]

CIC Filter		IIR Filter		Cascaded Filters Only		Entire Signal Chain					
						−3 dB Frequency		Group Delay at 200 Hz		RMS Noise	
Setting	−3 dB Frequency (Hz)	Setting	−3 dB Frequency (Hz)	−3 dB Frequency (Hz)[2]	Group Delay at 200 Hz (µs)[3]	X- and Y-Axes (Hz)	Z-Axis (Hz)	X- and Y-Axes (µs)	Z-Axis (µs)	X- and Y-Axes (m*g*)	Z-Axis (m*g*)
00	7668	00	5002	4051[4]	70.9[4]	6841[4]	4691[4]	84.7[4]	91.3[4]	85 m*g*[4]	120[4]
00	7668	01	2501	2343	103	6297	4314	117	123		
00	7668	10	1250	1229	166	1384	3912	180	187		
00	7668	11	625	622	294	639	668	308	314		
01	3829	00	5002	2926	113	6113	4369	126	133		
01	3829	01	2501	2025[4]	144[4]	5747[4]	4091[4]	158[4]	165[4]	22.5[4]	30[4]
01	3829	10	1250	1171	208	1295	3754	222	228		
01	3829	11	625	614	335	630	657	349	356		
10	1914	00	5002	1752	196	2100	3642	210	216		
10	1914	01	2501	1463	228	1659	3437	242	248		
10	1914	10	1250	1012[4]	291[4]	1078[4]	1224[4]	305[4]	312[4]	5.5[4]	7.0[4]
10	1914	11	625	586	419	599	620	433	439		
11	957	00	5002	934	363	974	1046	376	383		
11	957	01	2501	876	394	909	968	408	415		
11	957	10	1250	731	458	752	786	472	478		
11	957	11	625	506[4]	585[4]	513[4]	525[4]	599[4]	606[4]	2.5[4]	4.0[4]

[1] A blank cell in this table indicates that the associated value is not measured for this setting.
[2] The −3 dB frequencies shown in this table are from the combination of the CIC and IIR filters only. These frequencies do not include the effects of the resonant frequency of the sensor.
[3] The group delay values shown in this table are from the cascaded filters only. These group delay values do not include the additional delay imposed by the front-end electronics or the ADC.
[4] See the circles in Figure 33 through Figure 36 for more information.

REGISTER MAP

Table 16. Register Summary

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset[1]	RW
0x00	DEVICE_ID0	[7:0]	VARIANT[2:0]			REVID					0x22	R
0x01	DEVICE_ID1	[7:0]	XL_X	XL_Y	XL_Z	YAW	ROLL	PITCH	VARIANT[4:3]		0xE2	R
0x80	USER_REG_KEY	[7:0]	USER_REG_KEY								0xBC	RW
0x81	I2S_CFG0	[7:0]	INV	Early	ALT	TDMSS	RSVD	TDMMODE			0x01	RW
0x82	I2S_CFG1	[7:0]	RSVD					TXBCLKINV	TX1EN	TX0EN	0x00	RW
0x83	CLOCK_RATE	[7:0]	RSVD					A2B_CLK_RATE			0x00	RW
0x84	X_ST	[7:0]	RSVD					X_ST_AC	X_ST_POS	X_ST_NEG	0x00	RW
0x85	X_FILT	[7:0]	X_HPF_EN	X_IIR_EN	X_HPF_CORNER		X_IIR_CORNER		X_CIC_CORNER_LPF		0x40	RW
0x86	Y_ST	[7:0]	RSVD					Y_ST_AC	Y_ST_NEG	Y_ST_POS	0x00	RW
0x87	Y_FILT	[7:0]	Y_HPF_EN	Y_IIR_EN	Y_HPF_CORNER		Y_IIR_CORNER		Y_CIC_CORNER_LPF		0x40	RW
0x88	Z_ST	[7:0]	RSVD					Z_ST_AC	Z_ST_POS	Z_ST_NEG	0x00	RW
0x89	Z_FILT	[7:0]	Z_HPF_EN	Z_IIR_EN	Z_HPF_CORNER		Z_IIR_CORNER		Z_CIC_CORNER_LPF		0x40	RW
0x8A	X_DATA_LO	[7:0]	X_DATA[7:0]								N/A	R
0x8B	X_DATA_HI	[7:0]	X_DATA[15:8]								N/A	R
0x8C	Y_DATA_LO	[7:0]	Y_DATA[7:0]								N/A	R
0x8D	Y_DATA_HI	[7:0]	Y_DATA[15:8]								N/A	R
0x8E	Z_DATA_LO	[7:0]	Z_DATA[7:0]								N/A	R
0x8F	Z_DATA_HI	[7:0]	Z_DATA[15:8]								N/A	R

[1] N/A means not applicable.

REGISTER DETAILS

This section describes the functions of the ADXL317 registers. The ADXL317 powers up with the default register values shown in the Reset column of Table 16 in the Register Map section. Unless otherwise noted, values in the Settings and Reset columns of the tables in this section are in binary.

Registers with a value of R in the RW column are read only. Any attempt to write to these registers is ignored. Any bits labeled RSVD are reserved for use by Analog Devices only and must not be changed.

To make changes to any of the writeable registers, the user register key must first be written to the USER_REG_KEY register. See the USER_REG_KEY register explanation for details.

DEVICE ID REGISTERS

The device ID registers contain the information necessary to identify the specific version of the ADXL317 device.

Table 17. DEVICE_ID0 Register Summary (Address: 0x00, Name: DEVICE_ID0, Reset: 0x22)

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	VARIANT[2:0]		Analog Devices Variant Identification. This field contains the lower three bits of the Analog Devices device variant information. This 5-bit field is set to 0x11 (17 decimal). Therefore, the lower three bits are 001.	001	R
		000	Not used.		
		001	ADXL317.		
		010 … 111	Not used.		
[4:0]	REVID		Analog Devices Product Revision Identification. This field contains the revision ID for this product. This field identifies each major revision of the ADXL317, beginning with 0 and incrementing for each significant change.	0xXX	R
		0x00	A samples.		
		0x01	B samples.		
		0x02	C samples.		
		0x03 … 0x1F	Future releases.		

The DEVICE_IDx registers contain information necessary to distinguish the particular version of the ADXL317 device being implemented in the customer application. The device ID is implemented with sufficient flexibility to track the following types of information:

- Axes of sensitivity.
- Temperature range.
- Performance grade.
- SPI interface version.
- Major product revisions.

The device ID provides an electronically readable identification mechanism for the ADXL317. The specific function of each subset of the device ID is provided in this section. The device ID is implemented across the Analog Devices portfolio of inertial sensing components. It is not expected that all functions of the device ID be implemented for all products.

At the time of this data sheet release, the full device ID for the ADXL317 is 0xE222.

REVID

REVID contains the customer revision ID for the ADXL317. This field is intended to store significant changes to the device revision throughout its lifetime. Examples include

- Prerelease: A sample, B sample, C sample, and so on.
- Postrelease: major changes to silicon (ASIC or MEMS).

At the time of this data sheet release, the REVID value is 0x02.

Variant

The variant field provides an identification value that corresponds to the specific model number purchased by the customer. There is no significance to the value stored in the variant field, only that it is uniquely associated with a given model number. The variant field for the ADXL317 is 0x11.

Pitch

The pitch field indicates if the inertial sensor is capable of sensing angular rate along the pitch axis of the package.

Table 18. Pitch Bit Settings

State	Pitch Angular Rate Sensitive
0	No
1	Yes

Roll

The roll field indicates if the inertial sensor is capable of sensing angular rate along the roll axis of the package.

Table 19. Roll Bit Settings

State	Roll Angular Rate Sensitive
0	No
1	Yes

Yaw

The yaw field indicates if the inertial sensor is capable of sensing angular rate along the yaw axis of the package.

Table 20. Yaw Bit Settings

State	Yaw Angular Rate Sensitive
0	No
1	Yes

XL_Z

The XL_Z field indicates if the inertial sensor is capable of sensing acceleration relative to the z-axis of the package.

Table 21. XL_Z Bit Settings

State	Z-Axis Acceleration Sensitive
0	No
1	Yes

XL_Y

The XL_Y field indicates if the inertial sensor is capable of sensing acceleration relative to the y-axis of the package.

Table 22. XL_Y Bit Settings

State	Y-Axis Acceleration Sensitive
0	No
1	Yes

XL_X

The XL_X field indicates if the inertial sensor is capable of sensing acceleration relative to the x-axis of the package.

Table 23. XL_X Bit Settings

State	X-Axis Acceleration Sensitive
0	No
1	Yes

Table 24. DEVICE_ID1 Register Summary (Address: 0x01, Name: DEVICE_ID1, Reset: 0xE2)

Bits	Bit Name	Settings	Description	Reset	Access
7	XL_X		X-Sensitive Accelerometer.	1	R
		0	The device does not contain an accelerometer sensitive to the x-axis.		
		1	The device contains an accelerometer sensitive to the x-axis.		
6	XL_Y		Y-Sensitive Accelerometer.	1	R
		0	The device does not contain an accelerometer sensitive to the y-axis.		
		1	The device contains an accelerometer sensitive to the y-axis.		
5	XL_Z		Z-Sensitive Accelerometer.	1	R
		0	The device does not contain an accelerometer sensitive to the z-axis.		
		1	The device contains an accelerometer sensitive to the z-axis.		
4	YAW		Yaw Sensitive Gyroscope.	0	R
		0	The device does not contain a yaw sensitive gyroscope.		
		1	The device contains a yaw sensitive gyroscope.		
3	ROLL		Roll Sensitive Gyroscope.	0	R
		0	The device does not contain a roll sensitive gyroscope.		
		1	The device contains a roll sensitive gyroscope.		
2	PITCH		Pitch Sensitive Gyroscope.	0	R
		0	The device does not contain a pitch sensitive gyroscope.		
		1	The device contains a pitch sensitive gyroscope.		
[1:0]	VARIANT[4:3]		Analog Devices Variant Identification. This field contains the upper two bits of the Analog Devices device variant information. This 5-bit field is set to 0x11 (17 decimal). Therefore, the upper two bits are 10.	10	R
		00 … 01	Not used.		
		10	ADXL317.		
		11	Not used.		

USER REGISTER KEY REGISTER (ADDRESS: 0x80, NAME: USER_REG_KEY, RESET: 0xBC)

The user register key register is the lockout register for the ADXL317 and prevents unintended writes to the device during system power-up. When the ADXL317 first powers up, all attempts to write to any of the device registers are ignored until the proper key is written to the USER_REG_KEY register. This write protects the device from entering an unexpected state during potential transient activity on the I^2C bus.

Before making changes to any of the subsequent registers, the following procedure must be completed:

1. Write 0xBC to the USER_REG_KEY register (Address 0x80).
2. Write 0x43 to the USER_REG_KEY register (Address 0x80).

After writing these two values, all writeable registers are unlocked and can be written to as normal. After being unlocked, the USER_REG_KEY register returns 0xBC. The two writes to enter user test mode must be performed using two separate, single-byte writes. A multibyte write cannot be used to enter user test mode.

After entering test mode, the user must observe a wait time before reading the x_DATA_LO or x_DATA_HI registers (Address 0x8A to Address 0x8F). This wait time is equal to the group delay time shown in Table 15.

I^{2}S CONFIGURATION REGISTERS

The I^{2}S configuration registers control various settings for the I^{2}S bus of the ADXL317. For more information about how these settings affect the timing of the I^{2}S output, see the I^{2}S/TDM Interface section.

Table 25. I2S_CFG0 Register Summary (Address: 0x81, Name: I2S_CFG0, Reset: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
7	INV		I^{2}S Clock Polarity. This bit sets the clock polarity for I^{2}S communications.	0	RW
		0	Audio frame begins on rising edge of SYNC signal.		
		1	Audio frame begins on falling edge of SYNC signal.		
6	Early		I^{2}S Early Sync. This bit sets the timing of the SYNC signal.	0	RW
		0	SYNC changes in same cycle as the MSB of the first data channel.		
		1	SYNC changes one cycle before the MSB of the first data channel.		
5	ALT		I^{2}S Alternating Sync. This bit sets the behavior of the SYNC signal.	0	RW
		0	SYNC is asserted for one BCLK cycle only.		
		1	SYNC is asserted at the beginning of each sampling period and then toggled in the middle of each sampling period.		
4	TDMSS		I^{2}S TDM Slot Size. This bit sets the size for each TDM slot.	0	RW
		0	Each slot transmits 32 bits of data.		
		1	Each slot transmits 16 bits of data.		
3	RSVD		Reserved Bits.	00	RW
[2:0]	TDMMODE		I^{2}S TDM Mode. This field sets the TDM mode for I^{2}S communications.	01	RW
		00	TDM2.		
		01	TDM4.		
		10	TDM8.		

Table 26. I2S_CFG1 Register Summary (Address: 0x82, Name: I2S_CFG1, Reset: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RSVD		Reserved Bits.	0000	RW
2	TXBCLKINV		I^{2}S Transmit Clock Inversion. This bit sets the edge of BCLK on which the data transmit pins change.	0	RW
		0	DTX0 and DTX1 pins change on the rising edge of BCLK.		
		1	DTX0 and DTX1 pins change on the falling edge of BCLK.		
1	TX1EN		I^{2}S Channel 1 Enable. This bit enables the transmission of data on I^{2}S Channel 1 (DTX1).	0	RW
		0	Data transmission is disabled on Channel 1.		
		1	Data transmission is enabled on Channel 1.		
0	TX0EN		I^{2}S Channel 0 Enable. This bit enables the transmission of data on I^{2}S Channel 0 (DTX0).	0	RW
		0	Data transmission is disabled on Channel 0.		
		1	Data transmission is enabled on Channel 0.		

CLOCK RATE REGISTER

Table 27. I2S_CFG1 Register Summary (Address: 0x83, Name: CLOCK_RATE, Reset: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RSVD		Reserved Bits.	0x00	RW
[2:0]	A2B_CLK_RATE		A^{2}B Clock Rate Select. This field sets the rate of the BCLK signal. Supplying a clock that does not match the setting in this field may result in unpredictable behavior and incorrect data.	000	RW
		000	6.144 MHz.		
		001	3.072 MHz.		
		010…111	Not used.		

X-AXIS SELF TEST CONFIGURATION REGISTER

The x-axis self test configuration register enables the self test functionality on the x-axis. Although the ADXL317 supports three types of self test on each axis (negative, positive, and ac), only one such test can be enabled at one time. The X_ST_AC, X_ST_POS, and X_ST_NEG bits are mutually exclusive. If more than one of these bits are asserted, self test is disabled. See Table 8 for a list of all possible combinations of settings for this register and how they affect the self test output. See the Using Self Test section for more information.

Table 28. X_ST Register Summary (Address: 0x84, Name: X_ST, Reset: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RSVD		Reserved Bits.	00000	RW
2	X_ST_AC		X-Axis AC Self Test Enable. This bit enables the ac self test functionality on the x-axis.	0	RW
		0	AC self test is disabled on the x-axis.		
		1	A 100 Hz square wave self test is applied to the x-axis.		
1	X_ST_POS		X-Axis Positive Self Test Enable. This bit enables the positive self test functionality on the x-axis.	0	RW
		0	Positive self test is disabled on the x-axis.		
		1	A positive (dc) self test is applied to the x-axis.		
0	X_ST_NEG		X-Axis Negative Self Test Enable. This bit enables the negative self test functionality on the x-axis.	0	RW
		0	Negative self test is disabled on the x-axis.		
		1	A negative (dc) self test is applied to the x-axis.		

X-AXIS FILTER CONFIGURATION REGISTER

The x-axis filter configuration register controls the various filters along the x-axis signal chain in the ADXL317.

Table 29. X_FILT Register Summary (Address: 0x85, Name: X_FILT, Reset: 0x40)

Bits	Bit Name	Settings	Description	Reset	Access
7	X_HPF_EN		X-Axis High-Pass Filter Enable. This bit enables the high-pass filter in the x-axis signal chain. This filter is disabled by default.	0	RW
		0	The high-pass filter is disabled in the x-axis signal chain.		
		1	The high-pass filter is enabled in the x-axis signal chain.		
6	X_IIR_EN		X-Axis IIR Filter Enable. This bit enables the IIR filter in the x-axis signal chain. This filter is enabled by default.	1	RW
		0	The IIR filter is disabled in the x-axis signal chain.		
		1	The IIR filter is enabled in the x-axis signal chain.		
[5:4]	X_HPF_CORNER		X-Axis High-Pass Filter Corner Select. This field controls the corner frequency of the high-pass filter in the x-axis signal chain, if enabled.	00	RW
		00	29.8 Hz.		
		01	7.46 Hz.		
		10	1.85 Hz.		
		11	0.46 Hz.		
[3:2]	X_IIR_CORNER		X-Axis IIR Filter Corner Select. This field controls the corner frequency of the IIR filter in the x-axis signal chain, if enabled.	00	RW
		00	5002 Hz.		
		01	2501 Hz.		
		10	1250 Hz.		
		11	625 Hz.		
[1:0]	X_CIC_CORNER_LPF		X-Axis CIC Low-Pass Filter Corner Select. This field controls the corner frequency of the CIC low-pass filter in the x-axis signal chain.	00	RW
		00	7668 Hz.		
		01	3829 Hz.		
		10	1914 Hz.		
		11	957 Hz.		

Y-AXIS SELF TEST CONFIGURATION REGISTER

The y-axis self test configuration register enables self test functionality on the y-axis. Although the ADXL317 supports three types of self test on each axis (negative, positive, and ac), only one such test can be enabled at a time. The Y_ST_AC, Y_ST_POS, and Y_ST_NEG bits are mutually exclusive. If more than one of these bits are asserted, self test is disabled. See Table 8 for a list of all possible combinations of settings for this register and how they affect the self test output. See the Using Self Test section for more information.

Table 30. Y_ST Register Summary (Address: 0x86, Name: Y_ST, Reset: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RSVD		Reserved Bits	0x00	RW
2	Y_ST_AC		Y-Axis AC Self Test Enable. This bit enables the ac self test functionality on the Y-axis.	0	RW
		0	AC self test is disabled on the y-axis.		
		1	A 100 Hz square wave self test is applied to the y-axis.		
1	Y_ST_NEG		Y-Axis Negative Self Test Enable. This bit enables the negative self test functionality on the y-axis.	0	RW
		0	Negative self test is disabled on the y-axis.		
		1	A negative (dc) self test is applied to the y-axis.		
0	Y_ST_POS		Y-Axis Positive Self Test Enable. This bit enables the positive self test functionality on the y-axis.	0	RW
		0	Positive self test is disabled on the y-axis.		
		1	A positive (dc) self test is applied to the y-axis.		

Y-AXIS FILTER CONFIGURATION REGISTER

The y-axis filter configuration register controls the various filters along the y-axis signal chain in the ADXL317.

Table 31. Y_FILT Register Summary (Address: 0x87, Name: Y_FILT, Reset: 0x40)

Bits	Bit Name	Settings	Description	Reset	Access
7	Y_HPF_EN		Y-Axis High-Pass Filter Enable. This bit enables the high-pass filter in the y-axis signal chain. This filter is disabled by default.	0	RW
		0	The high-pass filter is disabled in the y-axis signal chain.		
		1	The high-pass filter is enabled in the y-axis signal chain.		
6	Y_IIR_EN		Y-Axis IIR Filter Enable. This bit enables the IIR filter in the y-axis signal chain. This filter is enabled by default.	1	RW
		0	The IIR filter is disabled in the y-axis signal chain.		
		1	The IIR filter is enabled in the y-axis signal chain.		
[5:4]	Y_HPF_CORNER		Y-Axis High-Pass Filter Corner Select. This field controls the corner frequency of the high-pass filter in the y-axis signal chain, if enabled.	00	RW
		00	29.8 Hz.		
		01	7.46 Hz.		
		10	1.85 Hz.		
		11	0.46 Hz.		
[3:2]	Y_IIR_CORNER		Y-Axis IIR Filter Corner Select. This field controls the corner frequency of the IIR filter in the y-axis signal chain, if enabled.	00	RW
		00	5002 Hz.		
		01	2501 Hz.		
		10	1250 Hz.		
		11	625 Hz.		
[1:0]	Y_CIC_CORNER_LPF		Y-Axis CIC Low-Pass Filter Corner Select. This field controls the corner frequency of the CIC low-pass filter in the y-axis signal chain.	00	RW
		00	7668 Hz.		
		01	3829 Hz.		
		10	1914 Hz.		
		11	957 Hz.		

Z-AXIS SELF TEST CONFIGURATION REGISTER

The z-axis self test configuration register enables self test functionality on the z-axis. Although the ADXL317 supports three types of self test on each axis (negative, positive, and ac), only one such test can be enabled at a time. The Z_ST_AC, Z_ST_POS, and Z_ST_NEG bits are mutually exclusive. If more than one of these bits are asserted, self test is disabled. See Table 8 for a list of all possible combinations of settings for this register and how they affect the self test output. See the Using Self Test section for more information.

Table 32. Z_ST Register Summary (Address: 0x88, Name: Z_ST, Reset: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RSVD		Reserved Bits.	0x00	RW
2	Z_ST_AC		Z-Axis AC Self Test Enable. This bit enables the ac self test functionality on the z-axis.	0	RW
		0	AC self test is disabled on the z-axis.		
		1	A 100 Hz square wave self test is applied to the z-axis.		
1	Z_ST_POS		Z-Axis Positive Self test Enable. This bit enables the positive self test functionality on the z-axis.	0	RW
		0	Positive self test is disabled on the z-axis.		
		1	A positive (dc) self test is applied to the z-axis.		
0	Z_ST_NEG		Z-Axis Negative Self test Enable. This bit enables the negative self test functionality on the z-axis.	0	RW
		0	Negative self test is disabled on the z-axis.		
		1	A negative (dc) self test is applied to the z-axis.		

Z-AXIS FILTER CONFIGURATION REGISTER

The z-axis filter configuration register controls the various filters along the z-axis signal chain in the ADXL317.

Table 33. Z_FILT Register Summary (Address: 0x89, Name: Z_FILT, Reset: 0x40)

Bits	Bit Name	Settings	Description	Reset	Access
7	Z_HPF_EN		Z-Axis High-Pass Filter Enable. This bit enables the high-pass filter in the z-axis signal chain. This filter is disabled by default.	0	RW
		0	The high-pass filter is disabled in the z-axis signal chain.		
		1	The high-pass filter is enabled in the z-axis signal chain.		
6	Z_IIR_EN		Z-Axis IIR Filter Enable. This bit enables the IIR filter in the z-axis signal chain. This filter is enabled by default.	1	RW
		0	The IIR filter is disabled in the z-axis signal chain.		
		1	The IIR filter is enabled in the z-axis signal chain.		
[5:4]	Z_HPF_CORNER		Z-Axis High-Pass Filter Corner Select. This field controls the corner frequency of the high-pass filter in the z-axis signal chain, if enabled.	00	RW
		00	29.8 Hz.		
		01	7.46 Hz.		
		10	1.85 Hz.		
		11	0.46 Hz.		
[3:2]	Z_IIR_CORNER		Z-Axis IIR Filter Corner Select. This field controls the corner frequency of the IIR filter in the z-axis signal chain, if enabled.	00	RW
		00	5002 Hz.		
		01	2501 Hz.		
		10	1250 Hz.		
		11	625 Hz.		
[1:0]	Z_CIC_CORNER_LPF		Z-Axis CIC Low-Pass Filter Corner Select. This field controls the corner frequency of the CIC low-pass filter in the z-axis signal chain.	00	RW
		00	7668 Hz.		
		01	3829 Hz.		
		10	1914 Hz.		
		11	957 Hz.		

X-AXIS ACCELEROMETER DATA REGISTERS

The x-axis accelerometer data registers contain the 14-bit, zero padded, x-axis acceleration data. X_DATA_LO contains the 6 LSBs, and X_DATA_HI contains the 8 MSBs.

The 14-bit acceleration value is left justified, with Bit 0 and Bit 1 in the X_DATA_LO register fixed at 0. This setup mimics the format for 16-bit I²S data.

Table 34. X_DATA_LO Bit Map (Address: 0x8A, Reset: Not Applicable; B1 and B0 Are Fixed at 0)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LSB	0	0

Table 35. X_DATA_HI Bit Map (Address: 0x8B, Reset: Not Applicable)

B7	B6	B5	B4	B3	B2	B1	B0
MSB	0	0	0	0	0	0	0

Y-AXIS ACCELEROMETER DATA REGISTERS

The y-axis accelerometer data registers contain the 14-bit, zero padded y-axis acceleration data. Y_DATA_LO contains the 6 LSBs, and Y_DATA_HI contains the 8 MSBs.

The 14-bit acceleration value is left justified, with Bit 0 and Bit 1 in the Y_DATA_LO register fixed at 0. This setup mimics the format for 16-bit I²S data.

Table 36. Y_DATA_LO Bit Map (Address: 0x8C, Reset: Not Applicable; B1 and B0 Are Fixed at 0)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LSB	0	0

Table 37. Y_DATA_HI Bit Map (Address: 0x8D, Reset: Not Applicable)

B15	B14	B13	B12	B11	B10	B9	B8
MSB	0	0	0	0	0	0	0

Z-AXIS ACCELEROMETER DATA REGISTERS

The z-axis accelerometer data registers contain the 14-bit, zero padded z-axis acceleration data. Z_DATA_LO contains the 6 LSBs, and Z_DATA_HI contains the 8 MSBs.

The 14-bit acceleration value is left justified, with Bit 0 and Bit 1 in the Z_DATA_LO register fixed at 0. This setup mimics the format for 16-bit I²S data.

Table 38. Z_DATA_LO Bit Map (Address: 0x8E, Reset: Not Applicable; B1 and B0 Are Fixed at 0)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LSB	0	0

Table 39. Z_DATA_HI Bit Map (Address: 0x8F, Reset: Not Applicable)

B15	B14	B13	B12	B11	B10	B9	B8
MSB	0	0	0	0	0	0	0

MECHANICAL CONSIDERATIONS FOR MOUNTING

Care must be taken when mounting the ADXL317 to ensure the device is in a location immune to vibrations within the frequency range of desired measurements. Mount the ADXL317 on the PCB in a location close to a hard mounting point of the PCB to the case. Mounting the ADXL317 at a poorly supported PCB location, as shown in Figure 37, may result in large apparent measurement errors due to undamped PCB vibrations. Locating the accelerometer near a hard mounting point ensures that any PCB vibrations at the accelerometer are above the resonant frequency of the mechanical sensors and, therefore, effectively invisible to the device. Multiple mounting points close to the sensor and/or a thicker PCB also reduce the effect of system resonance on the performance of the sensor.

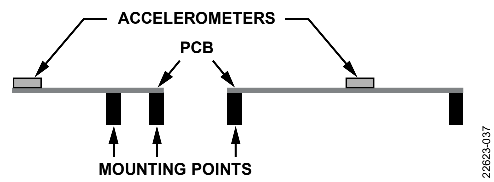


Figure 37. Examples of Incorrectly Placed Accelerometers

SOLDER REFLOW PROFILE

Figure 38 and Table 40 show the recommended solder profile and profile parameters for the ADXL317.

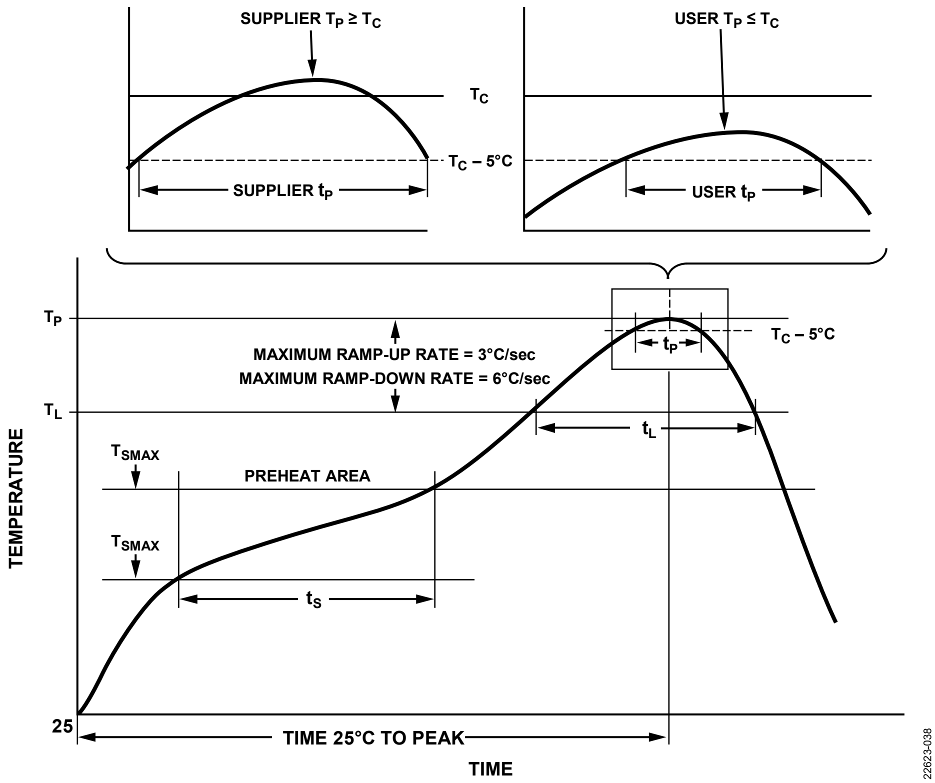


Figure 38. Pb-Free Solder Profile

Table 40. Solder Profile Parameters, per JEDEC J-STD-020D.1

Profile Feature	Symbol	Small Body Pb-Free Assemblies
Preheat/Soak		
Temperature Minimum	T_{SMIN}	150°C
Temperature Maximum	T_{SMAX}	200°C
Time from T_{SMIN} to T_{SMAX}	t_S	60 sec to 120 sec
Liquidous Temperature	T_L	217 °C
Time Maintained Above T_L	t_L	60 sec to 150 sec
Classification Temperature	T_C	260 °C
Peak Package Body Temperature	T_P	T_C–5 < T_P < T_C
Ramp-Up Rate (T_L to T_P)		3 °C/sec maximum
Time Within 5 °C of Classification Temperature (T_C)	t_P	30 sec maximum
Ramp-Down Rate (T_P to T_L)		6 °C/sec maximum
Time 25 °C to Peak Temperature		8 minutes maximum

AXES OF ACCELERATION SENSITIVITY

Figure 39 and Figure 40 show the default axes of sensitivity for the ADXL317.

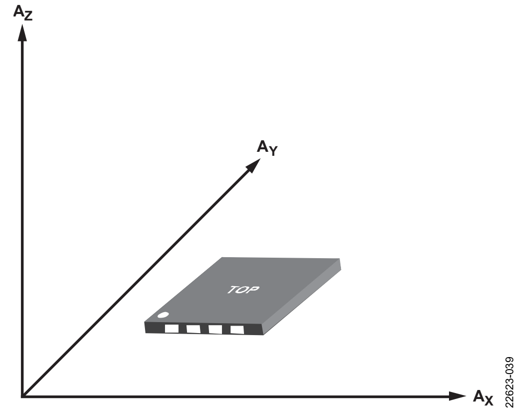


Figure 39. Axes of Acceleration Sensitivity (Corresponding Output Increases When Accelerated Along the Sensitive Axis)

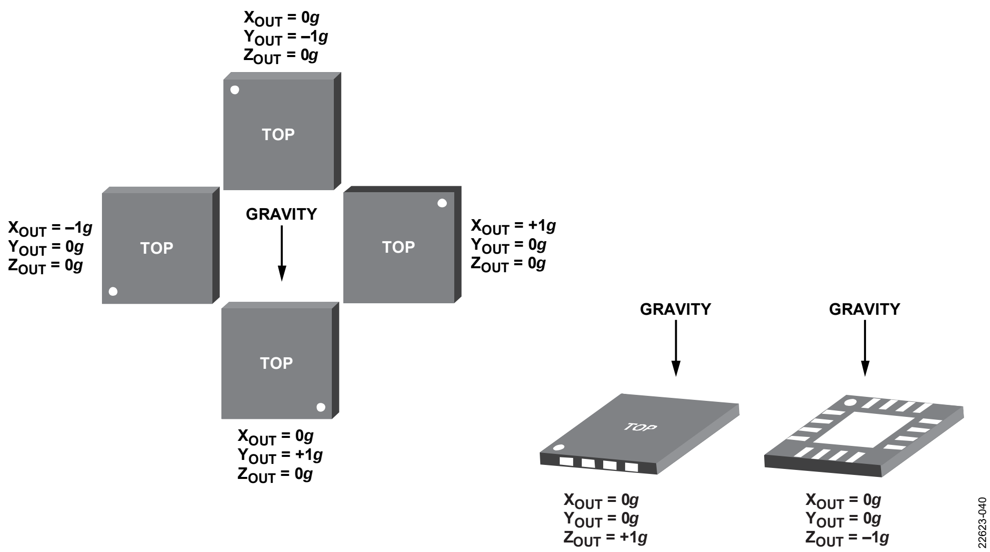


Figure 40. Output Response vs. Orientation to Gravity

OUTLINE DIMENSIONS

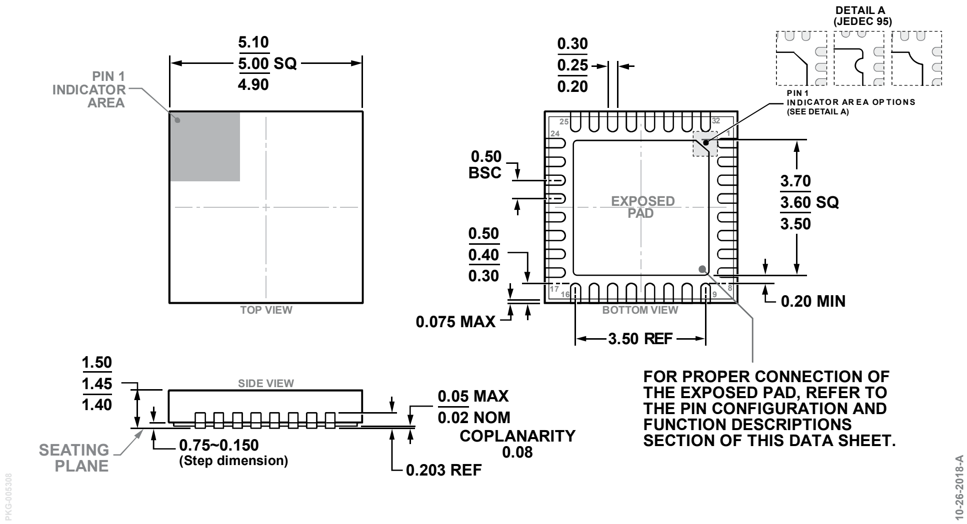


Figure 41. 32-Lead Frame Chip Scale Package [LFCSP_SS]
5 mm × 5 mm Body and 1.45 mm Package Height, with Side Solderable Leads
(CS-32-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADXL317WBCSZ-RL	−40°C to +125°C	32-Lead LFCSP_SS	CS-32-4

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADXL317W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

D22623-0-12/19(0)

ANALOG DEVICES

www.analog.com