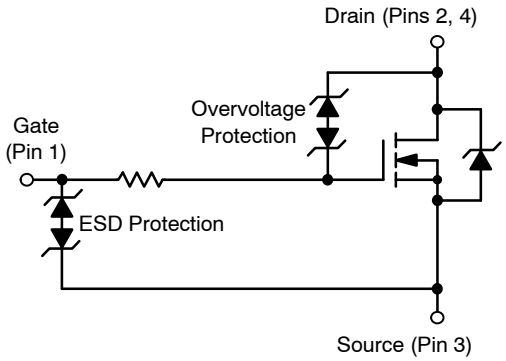
# Protected Power MOSFET

## 2.6 A, 52 V, N−Channel, Logic Level, Clamped MOSFET w/ ESD Protection

# NCV8440, NCV8440A

| $V_{DSS}$ (Clamped) | $R_{DS(ON)}$ TYP | $I_D$ MAX |
|---|---|---|
| 52 V | 95 mΩ @ 10 V | 2.6 A |




### Features

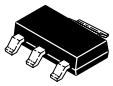
- Diode Clamp Between Gate and Source
- ESD Protection − Human Body Model 5000 V
- Active Over−Voltage Gate to Drain Clamp
- Scalable to Lower or Higher $R_{DS(on)}$
- Internal Series Gate Resistance
- These are Pb−Free Devices

### Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

### Applications

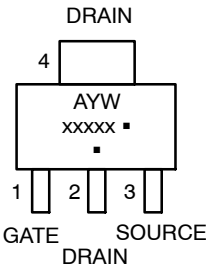
- Automotive and Industrial Markets:
  Solenoid Drivers, Lamp Drivers, Small Motor Drivers
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable



**SOT−223**
**CASE 318E**
**STYLE 3**

1 = Gate
2 = Drain
3 = Source

### MARKING DIAGRAM




A = Assembly Location
Y = Year
W = Work Week
xxxxx = V8440 or 8440A
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage Internally Clamped | $V_{DSS}$ | 52−59 | V |
| Gate−to−Source Voltage − Continuous | $V_{GS}$ | ±15 | V |
| Drain Current<br>− Continuous @ $T_A$ = 25°C<br>− Single Pulse ($t_p$ = 10 μs) (Note 1) | $I_D$<br><br>$I_{DM}$ | <br>2.6<br>10 | A |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1) | $P_D$ | 1.69 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to 150 | °C |
| Single Pulse Drain−to−Source Avalanche Energy ($V_{DD}$ = 50 V, $I_{D(pk)}$ = 1.17 A, $V_{GS}$ = 10 V, L = 160 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 110 | mJ |
| Load Dump Voltage ($V_{GS}$ = 0 and 10 V, $R_I$ = 2.0 Ω, $R_L$ = 9.0 Ω, td = 400 ms) | $V_{LD}$ | 60 | V |
| Thermal Resistance,<br>Junction−to−Ambient (Note 1)<br>Junction−to−Ambient (Note 2) | <br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>74<br>169 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to a FR4 board using 1″ pad size, (Cu area 1.127 $in^2$).
2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 $in^2$).

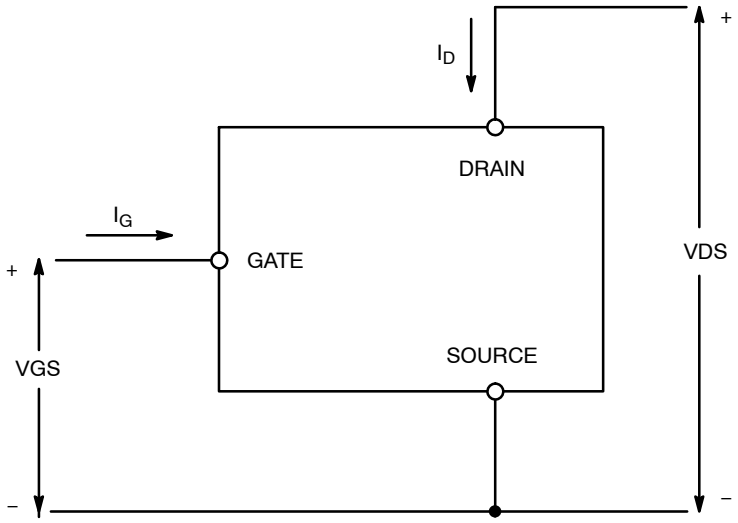



**Figure 1. Voltage and Current Convention**

**MOSFET ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain−to−Source Breakdown Voltage (Note 3)<br>($V_{GS}$ = 0 V, $I_D$ = 1.0 mA, $T_J$ = 25°C)<br>($V_{GS}$ = 0 V, $I_D$ = 1.0 mA, $T_J$ = −40°C to 125°C) (Note 4)<br>Temperature Coefficient (Negative) | $V_{(BR)DSS}$ | <br>52<br>50.8 | <br>55<br>54<br>−9.3 | <br>59<br>59.5 | <br>V<br>V<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 40 V, $V_{GS}$ = 0 V)<br>($V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_J$ = 125°C) (Note 4) | $I_{DSS}$ | | | <br>10<br>25 | μA |
| Gate−Body Leakage Current<br>($V_{GS}$ = ±8 V, $V_{DS}$ = 0 V)<br>($V_{GS}$ = ±14 V, $V_{DS}$ = 0 V) | $I_{GSS}$ | | <br>±35 | ±10 | μA |
| **ON CHARACTERISTICS** (Note 3) | | | | | |
| Gate Threshold Voltage (Note 3)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 100 μA)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | 1.1 | 1.5<br>−4.1 | 1.9 | V<br>mV/°C |
| Static Drain−to−Source On−Resistance (Note 3)<br>($V_{GS}$ = 3.5 V, $I_D$ = 0.6 A)<br>($V_{GS}$ = 4.0 V, $I_D$ = 1.5 A)<br>($V_{GS}$ = 10 V, $I_D$ = 2.6 A) | $R_{DS(on)}$ | | <br>150<br>135<br>95 | <br>180<br>160<br>110 | mΩ |
| Forward Transconductance (Note 3) ($V_{DS}$ = 15 V, $I_D$ = 2.6 A) | $g_{FS}$ | | 3.8 | | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | $V_{DS}$ = 35 V, $V_{GS}$ = 0 V, f = 10 kHz | $C_{iss}$ | | 155 | | pF |
| Output Capacitance | | $C_{oss}$ | | 60 | | |
| Transfer Capacitance | | $C_{rss}$ | | 25 | | |
| Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 10 kHz | $C_{iss}$ | | 170 | | pF |
| Output Capacitance | | $C_{oss}$ | | 70 | | |
| Transfer Capacitance | | $C_{rss}$ | | 30 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Not subject to production testing.
5. Switching characteristics are independent of operating junction temperatures.

**MOSFET ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| Turn−On Delay Time | $V_{GS}$ = 4.5 V, $V_{DD}$ = 40 V, $I_D$ = 2.6 A, $R_D$ = 15.4 Ω | $t_{d(on)}$ | | 375 | | ns |
| Rise Time | | $t_r$ | | 1525 | | |
| Turn−Off Delay Time | | $t_{d(off)}$ | | 1530 | | |
| Fall Time | | $t_f$ | | 1160 | | |
| Turn−On Delay Time | $V_{GS}$ = 4.5 V, $V_{DD}$ = 40 V, $I_D$ = 1.0 A, $R_D$ = 40 Ω | $t_{d(on)}$ | | 325 | | ns |
| Rise Time | | $t_r$ | | 1275 | | |
| Turn−Off Delay Time | | $t_{d(off)}$ | | 1860 | | |
| Fall Time | | $t_f$ | | 1150 | | |
| Turn−On Delay Time | $V_{GS}$ = 10 V, $V_{DD}$ = 15 V, $I_D$ = 2.6 A, $R_D$ = 5.8 Ω | $t_{d(on)}$ | | 190 | | ns |
| Rise Time | | $t_r$ | | 710 | | |
| Turn−Off Delay Time | | $t_{d(off)}$ | | 2220 | | |
| Fall Time | | $t_f$ | | 1180 | | |
| Gate Charge | $V_{GS}$ = 4.5 V, $V_{DS}$ = 40 V, $I_D$ = 2.6 A (Note 3) | $Q_T$ | | 4.5 | | nC |
| | | $Q_1$ | | 0.9 | | |
| | | $Q_2$ | | 2.6 | | |
| Gate Charge | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 1.5 A (Note 3) | $Q_T$ | | 3.9 | | nC |
| | | $Q_1$ | | 1.0 | | |
| | | $Q_2$ | | 1.7 | | |
| **SOURCE−DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On−Voltage | $I_S$ = 2.6 A, $V_{GS}$ = 0 V (Note 3)<br>$I_S$ = 2.6 A, $V_{GS}$ = 0 V, $T_J$ = 125°C | $V_{SD}$ | | 0.81<br>0.66 | 1.5 | V |
| Reverse Recovery Time | $I_S$ = 1.5 A, $V_{GS}$ = 0 V, $dI_s/dt$ = 100 A/μs (Note 3) | $t_{rr}$ | | 730 | | ns |
| | | $t_a$ | | 200 | | |
| | | $t_b$ | | 530 | | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | | 6.3 | | μC |
| **ESD CHARACTERISTICS** (Note 4) | | | | | | |
| Electro−Static Discharge Capability | Human Body Model (HBM) | ESD | 5000 | | | V |
| | Machine Model (MM) | | 500 | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Not subject to production testing.
5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES

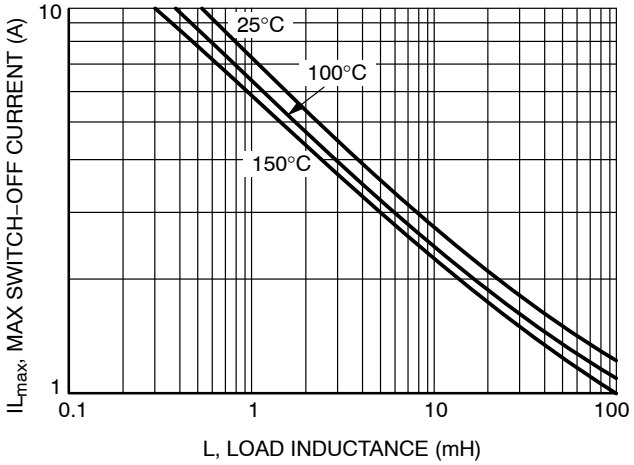



**Figure 1. Single Pulse Maximum Switch−off Current vs. Load Inductance**

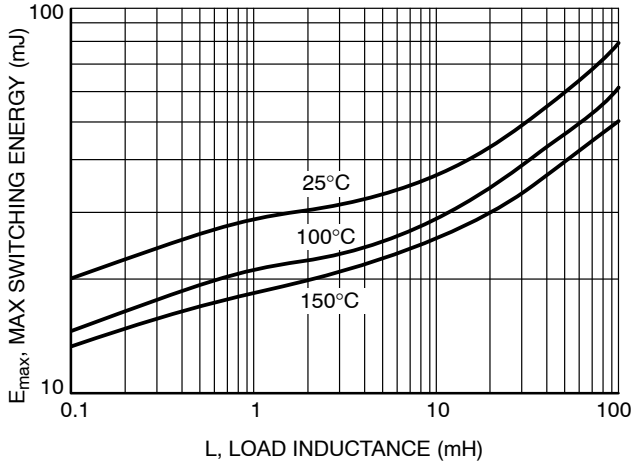



**Figure 2. Single Pulse Maximum Switching Energy vs. Load Inductance**

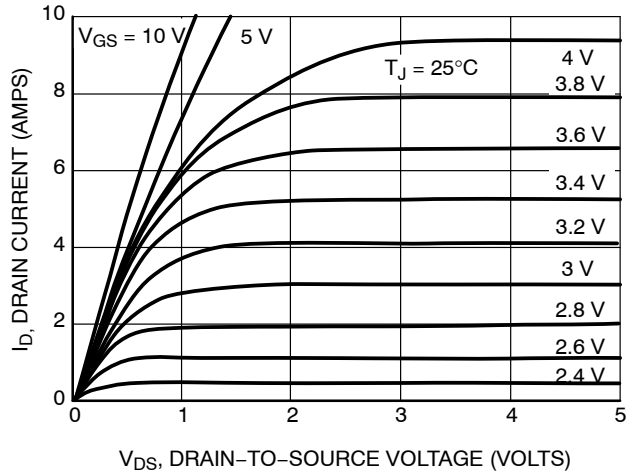



**Figure 3. On−State Output Characteristics**

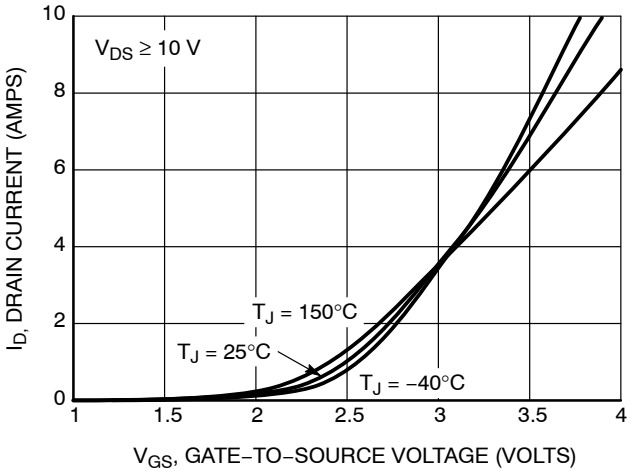



**Figure 4. Transfer Characteristics**

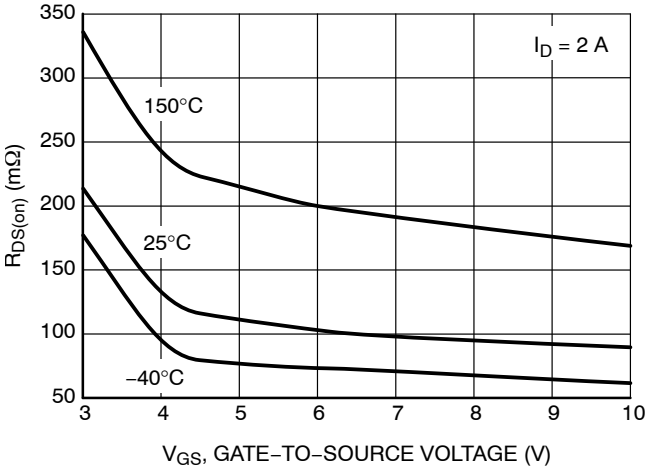



**Figure 5. $R_{DS(on)}$ vs. Gate−Source Voltage**

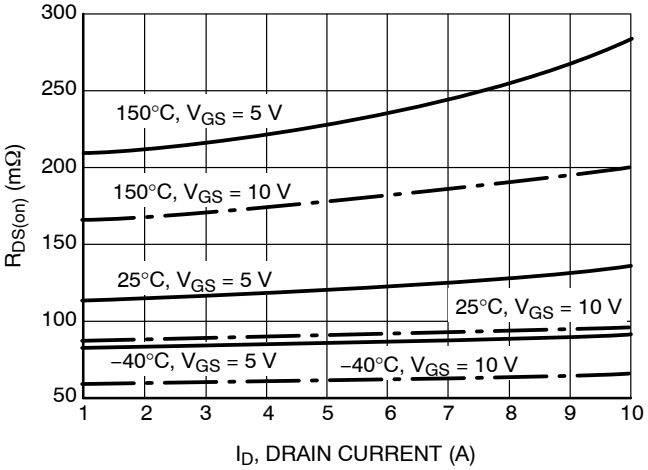



**Figure 6. $R_{DS(on)}$ vs. Drain Current**

## TYPICAL PERFORMANCE CURVES

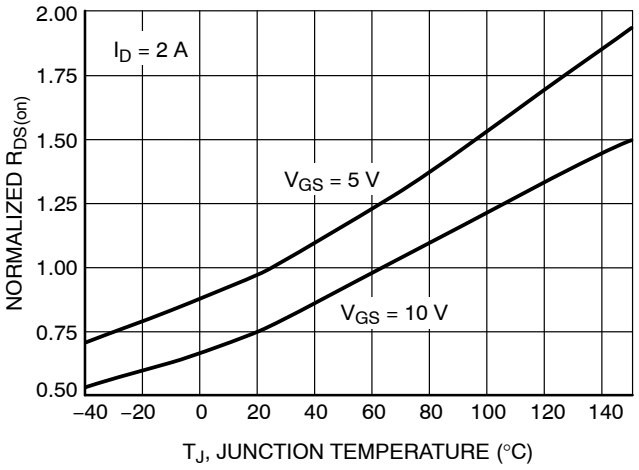



**Figure 7. Normalized $R_{DS(on)}$ vs. Temperature**

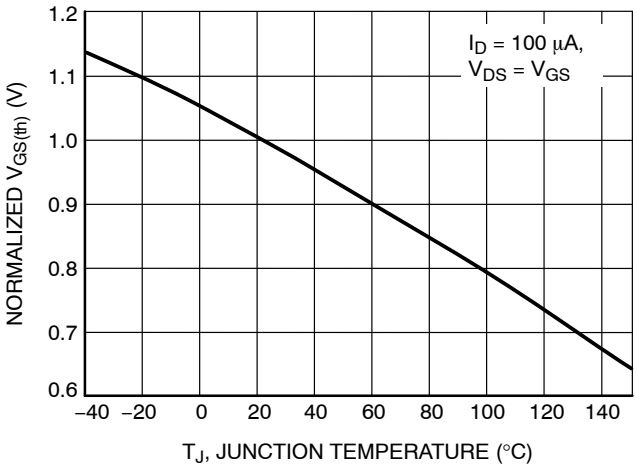



**Figure 8. Normalized Threshold Voltage vs. Temperature**

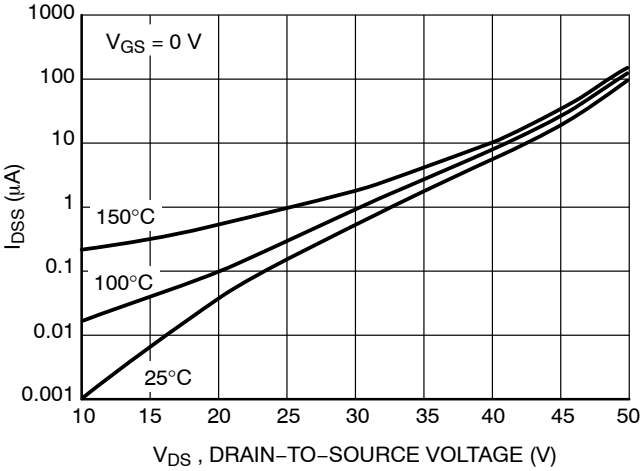



**Figure 9. Drain−to−Source Leakage Current**

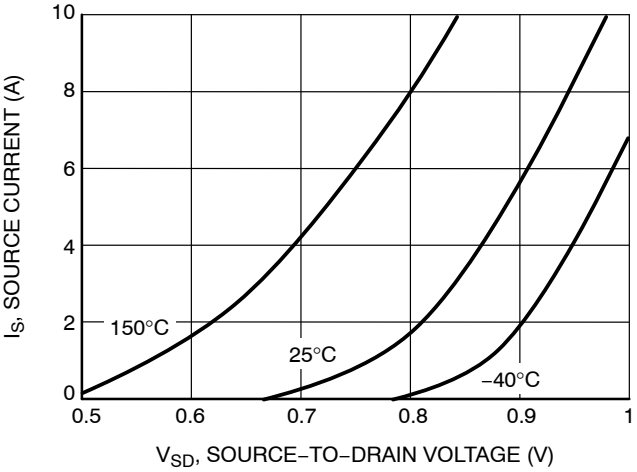



**Figure 10. Source−Drain Diode Forward Characteristics**

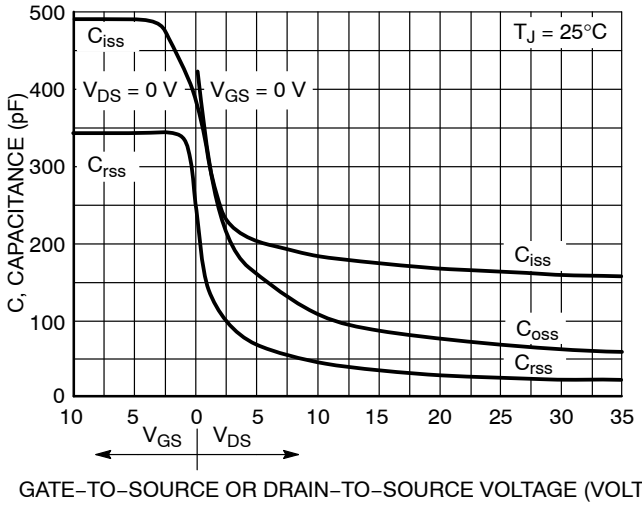



**Figure 11. Capacitance Variation**

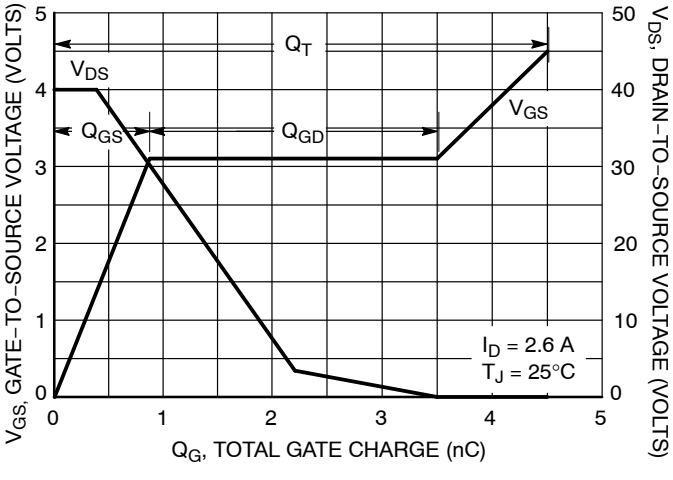



**Figure 12. Gate−to−Source Voltage vs. Total Gate Charge**

## TYPICAL PERFORMANCE CURVES

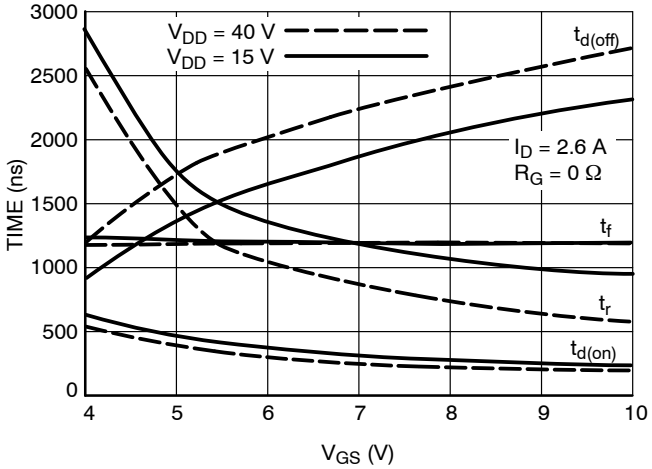



**Figure 13. Resistive Load Switching Time vs. Gate−Source Voltage**

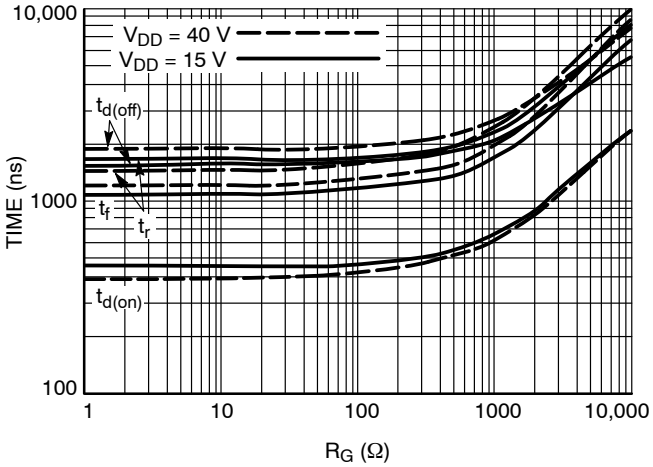



**Figure 14. Resistive Load Switching Time vs. Gate Resistance ($V_{GS}$ = 5 V, $I_D$ = 2.6 A)**

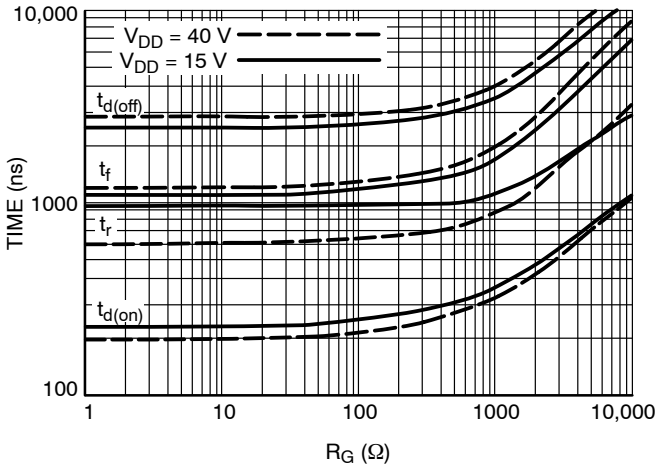



**Figure 15. Resistive Load Switching Time vs. Gate Resistance ($V_{GS}$ = 10 V, $I_D$ = 2.6 A)**

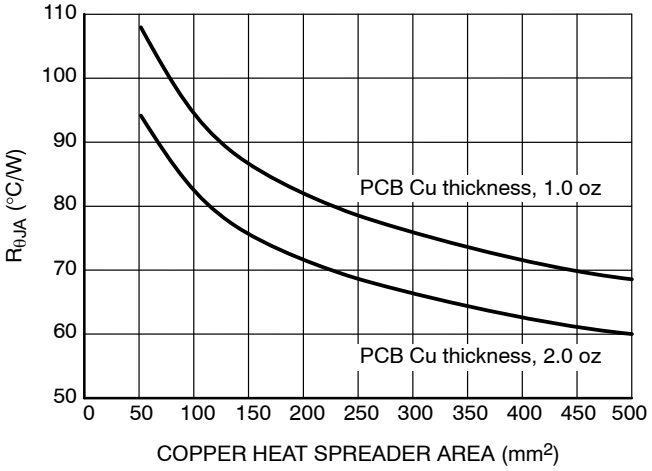



**Figure 16. $R_{\theta JA}$ vs. Copper Area**

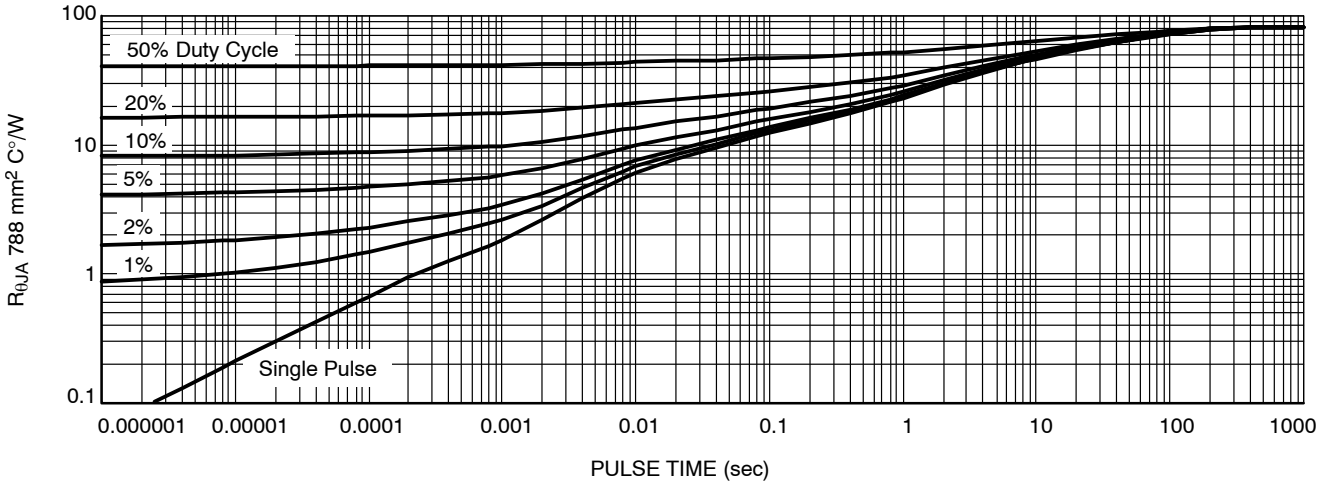



**Figure 17. Transient Thermal Resistance**

## ORDERING INFORMATION

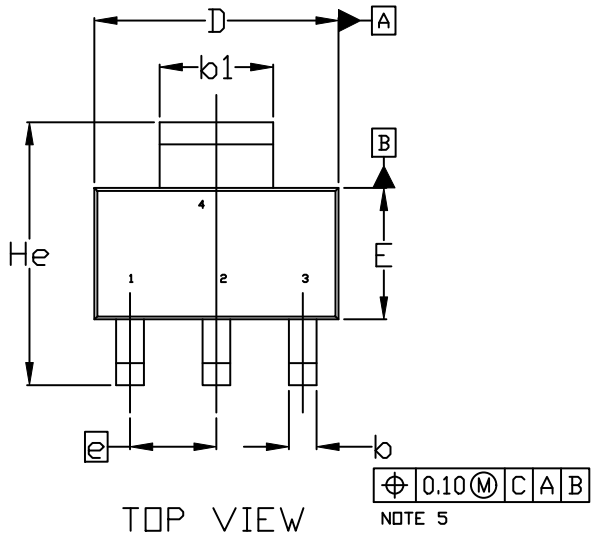
| Device | Package | Shipping† |
|---|---|---|
| NCV8440STT1G | SOT−223 (Pb−Free) | 1000 / Tape & Reel |
| NCV8440ASTT1G | SOT−223 (Pb−Free) | 1000 / Tape & Reel |
| NCV8440STT3G | SOT−223 (Pb−Free) | 4000 / Tape & Reel |
| NCV8440ASTT3G | SOT−223 (Pb−Free) | 4000 / Tape & Reel |

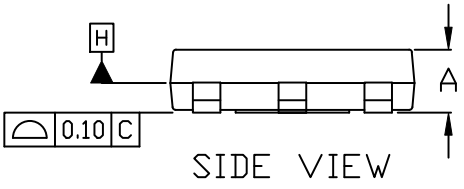
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

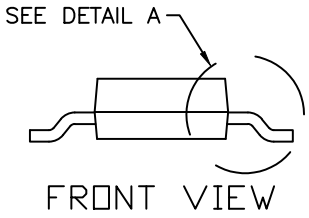
**SCALE 1:1**

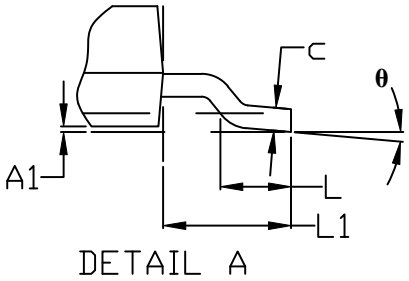
**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



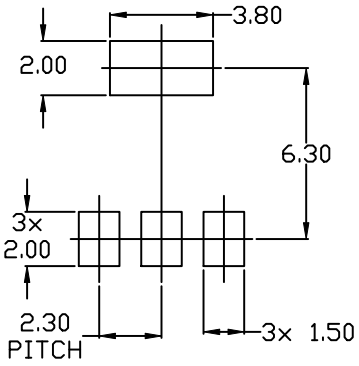




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |




RECOMMENDED MOUNTING FOOTPRINT

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42680B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOT−223 (TO−261)** | **PAGE 1 OF 2** |

**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

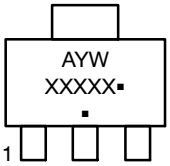
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAM*




A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
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