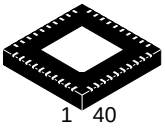
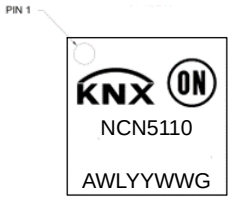
# Transceiver for KNX Twisted Pair Networks

# NCN5110




**QFN40**
**MN SUFFIX**
**CASE 485AU**

### MARKING DIAGRAM




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 23 of this data sheet.

### Introduction

NCN5110 is a receiver-transmitter IC suitable for use in KNX twisted pair networks (KNX TP1-256). It supports the connection of actuators, sensors, microcontrollers, switches or other applications in a building network.

NCN5110 handles the transmission and reception of active pulses on the bus. It generates from the unregulated bus voltage stabilized voltages for its own power needs as well as to power external devices, for example, a microcontroller.

NCN5110 assures safe coupling to and decoupling from the bus. Bus monitoring warns the external microcontroller in case of loss of power so that critical data can be stored in time.

### Key Features

- Supervision of KNX Bus Voltage and Current
- Supports Bus Current Consumption up to 40 mA
- High Efficient DC-DC Converters
  - 3.3 V Fixed
  - 1.2 V to 21 V Selectable
- Control and Monitoring of Power Regulators
- Linear 20 V Regulator
- Direct Coupling of Analog Signaling to Host
- No Crystal Required
- Optional Clock of 8 or 16 MHz for External Devices
- Temperature Monitoring
- Extended Operating Temperature Range −40 °C to +105 °C
- These Devices are Pb-Free and are RoHS Compliant

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## BLOCK DIAGRAM

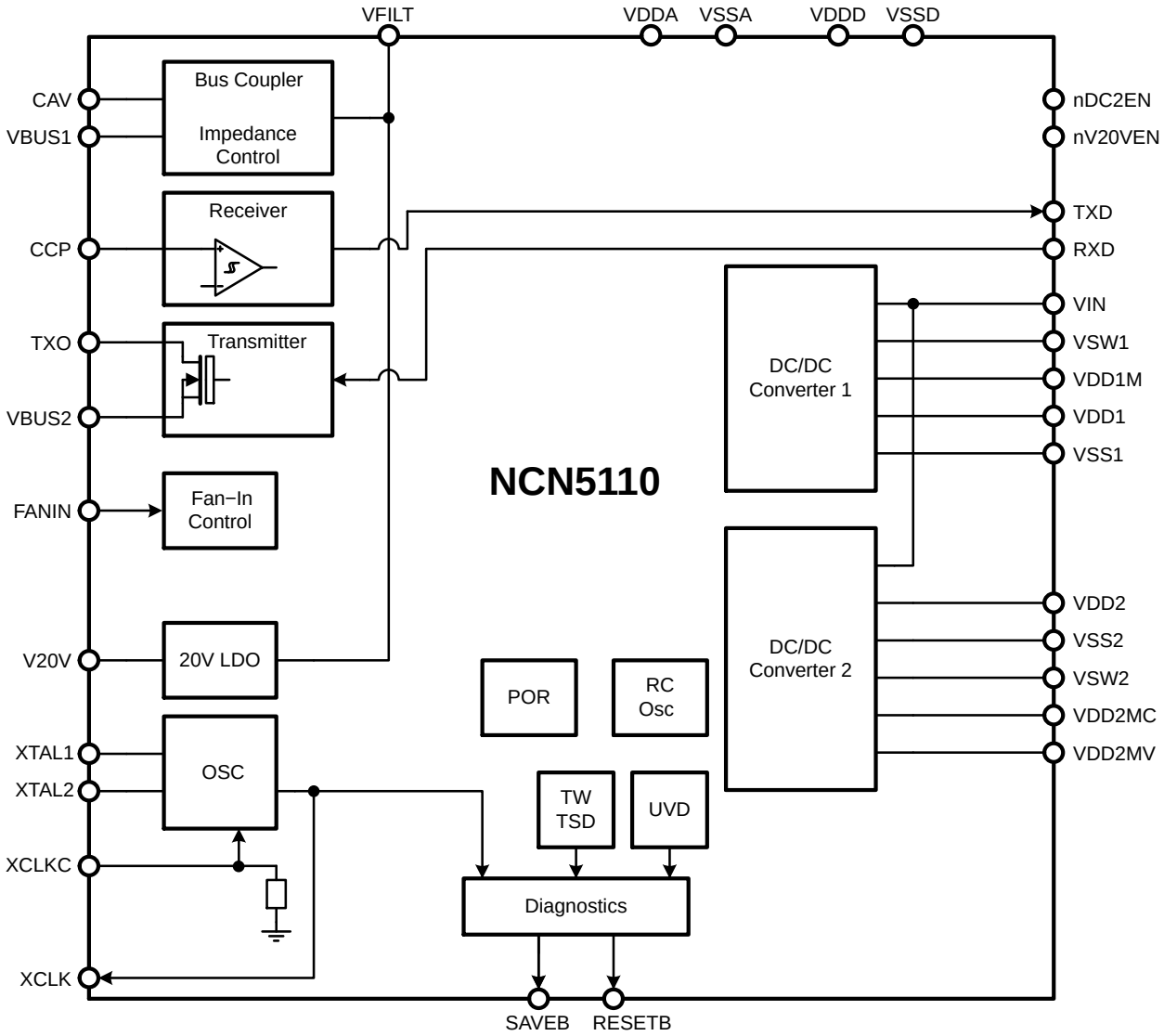


**Figure 1. Block Diagram NCN5110**

## PIN OUT

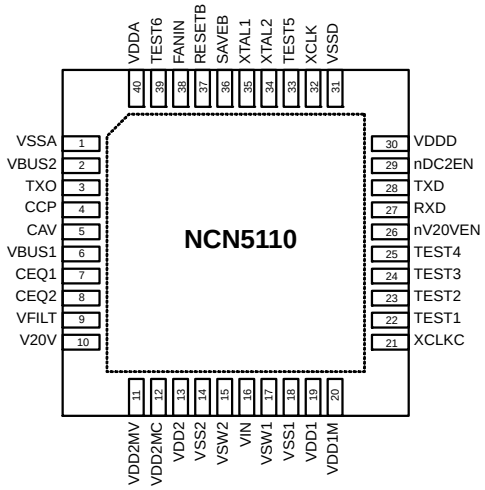


**Figure 2. Pin Out NCN5110 (Top View)**



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## PIN DESCRIPTION

**Table 1. PIN LIST AND DESCRIPTION**

| Name | Pin | Description | Type | Equivalent Schematic |
|---|---|---|---|---|
| VSSA | 1 | Analog Supply Voltage Ground | Supply | |
| VBUS2 | 2 | Ground for KNX Transmitter | Supply | |
| TX0 | 3 | KNX Transmitter Output | Analog Output | Type 1 |
| CCP | 4 | AC coupling external capacitor connection | Analog I/O | Type 2 |
| CAV | 5 | Capacitor connection to average bus DC voltage | Analog I/O | Type 3 |
| VBUS1 | 6 | KNX power supply input | Supply | Type 5 |
| CEQ1 | 7 | Capacitor connection 1 for defining equalization pulse | Analog I/O | Type 4 |
| CEQ2 | 8 | Capacitor connection 2 for defining equalization pulse | Analog I/O | Type 4 |
| VFILT | 9 | Filtered bus voltage | Supply | Type 5 |
| V20V | 10 | 20V supply output | Supply | Type 5 |
| VDD2MV | 11 | Voltage monitor of Voltage Regulator 2 | Analog Input | Type 8 |
| VDD2MC | 12 | Current monitor input 1 of Voltage Regulator 2 | Analog Input | Type 9 |
| VDD2 | 13 | Current monitor input 2 of Voltage Regulator 2 | Analog Input | Type 8 |
| VSS2 | 14 | Voltage Regulator 2 Ground | Supply | |
| VSW2 | 15 | Switch output of Voltage Regulator 2 | Analog Output | Type 6 |
| VIN | 16 | Voltage Regulator 1 and 2 Power Supply Input | Supply | Type 5 |
| VSW1 | 17 | Switch output of Voltage Regulator 1 | Analog Output | Type 6 |
| VSS1 | 18 | Voltage Regulator 1 Ground | Supply | |
| VDD1 | 19 | Current Input 2 and Voltage Monitor Input of Voltage Regulator 1 | Analog Input | Type 8 |
| VDD1M | 20 | Current Monitor Input 1 of Voltage Monitor 1 | Analog Input | Type 9 |
| XCLKC | 21 | Clock Frequency Configure | Digital Input | Type 12 |
| TEST1 | 22 | Test pin. Leave unconnected. | Digital Output | Type 13 |
| TEST2 | 23 | Test pin. Connect to VSS. | Digital Input | Type 12 |
| TEST3 | 24 | Test pin. Connect to VSS. | Digital Input | Type 12 |
| TEST4 | 25 | Test pin. Connect to VSS. | Digital Input | Type 12 |
| nV20VEN | 26 | 20 V LDO Disable | Digital Input | Type 14 |
| RXD | 27 | Receive Input | Digital Input | Type 14 |
| TXD | 28 | Transmit Output | Digital Output | Type 13 |
| nDC2EN | 29 | Voltage Regulator 2 Disable | Digital Input | Type 14 |
| VDDD | 30 | Digital Supply Voltage Input | Supply | Type 7 |
| VSSD | 31 | Digital Supply Voltage Ground | Supply | |
| XCLK | 32 | Oscillator Clock Output | Digital Output | Type 13 |
| TEST5 | 33 | Test pin. Connect to VSS. | Digital Input | Type 12 |
| XTAL2 | 34 | Clock Generator Output (Quartz) | Analog Output | Type 10 |
| XTAL1 | 35 | Clock Generator Input (Quartz) | Analog Input | Type 10 |
| SAVEB | 36 | Save Signal (open drain with pull-up) | Digital Output | Type 15 |
| RESETB | 37 | Reset Signal (open drain with pull-up) | Digital Output | Type 15 |
| FANIN | 38 | Fan-In Input | Analog Input | Type 11 |
| TEST6 | 39 | Test pin. Leave unconnected. | Analog Output | Type 16 |
| VDDA | 40 | Analog Supply Voltage Input | Supply | Type 7 |



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## EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

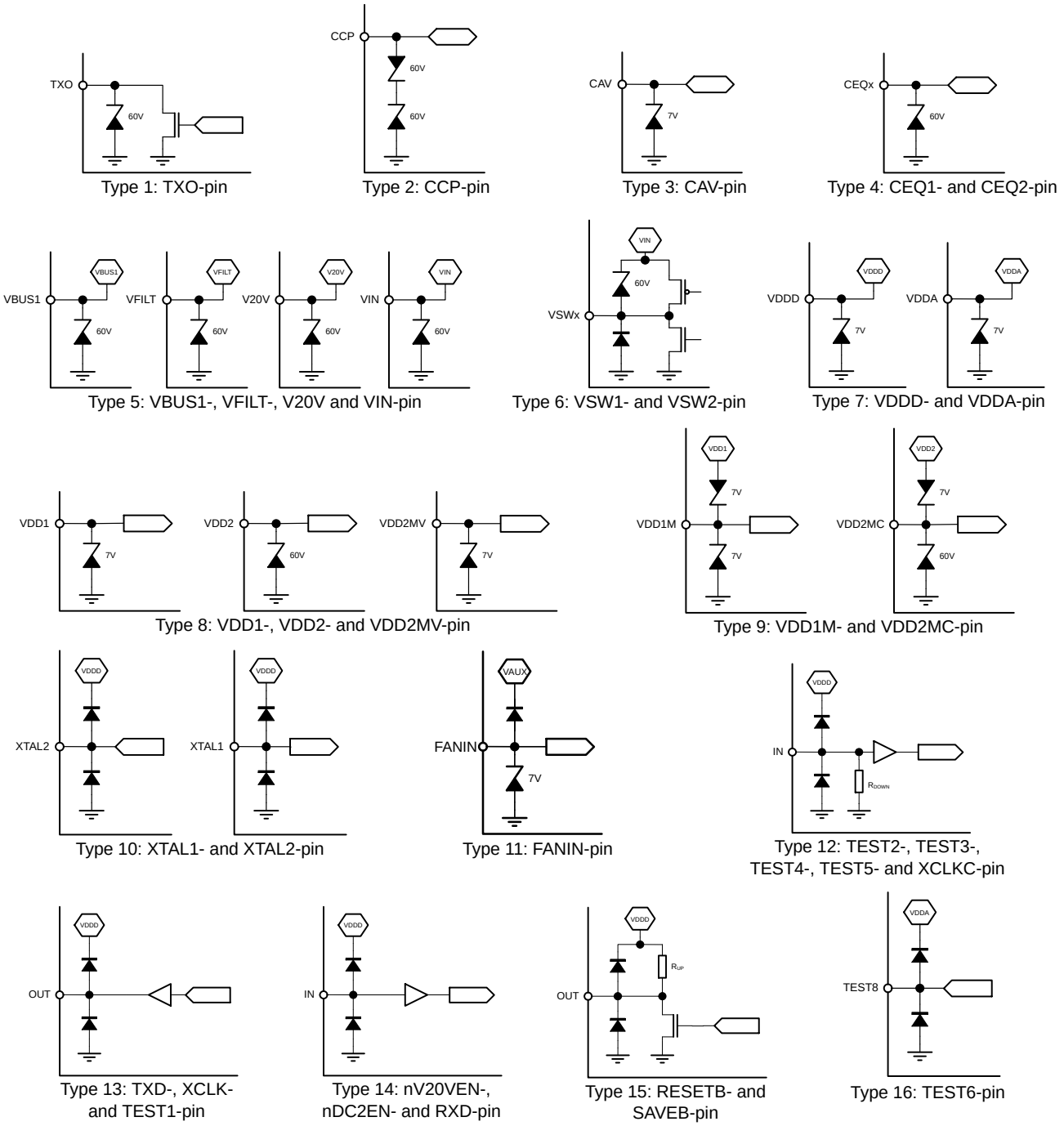


**Figure 3. In− and Output Equivalent Diagrams**



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## ELECTRICAL SPECIFICATION

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Notes 1 and 2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{TXO}$ | KNX Transmitter Output Voltage | −0.3 | +45 | V |
| $I_{TXO}$ | KNX Transmitter Output Current (Note 3) | | 250 | mA |
| $V_{CCP}$ | Voltage on CCP-pin | −10.5 | +14.5 | V |
| $V_{CAV}$ | Voltage on CAV-pin | −0.3 | +3.6 | V |
| $V_{BUS1}$ | Voltage on VBUS1-pin | −0.3 | +45 | V |
| $I_{BUS1}$ | Current Consumption VBUS1-pin | 0 | 120 | mA |
| $V_{FILT}$ | Voltage on VFILT-pin | −0.3 | +45 | V |
| $V_{20V}$ | Voltage on V20V-pin | −0.3 | +25 | V |
| $V_{DD2MV}$ | Voltage on VDD2MV-pin | −0.3 | +3.6 | V |
| $V_{DD2MC}$ | Voltage on VDD2MC-pin | −0.3 | +45 | V |
| $V_{DD2}$ | Voltage on VDD2-pin | −0.3 | +45 | V |
| $V_{SW}$ | Voltage on VSW1- and VSW2-pin | −0.3 | +45 | V |
| $V_{IN}$ | Voltage on VIN-pin | −0.3 | +45 | V |
| $V_{DD1}$ | Voltage on VDD1-pin | −0.3 | +3.6 | V |
| $V_{DD1M}$ | Voltage on VDD1M-pin | −0.3 | +3.6 | V |
| $V_{DIG}$ | Voltage on pins nV20VEN, nDC2EN, TXD, RXD, XCLK, SAVEB, RESETB, XCLKC, and FANIN | −0.3 | +3.6 | V |
| $V_{DD}$ | Voltage on VDDD- and VDDA-pin | −0.3 | +3.6 | V |
| $V_{XTAL}$ | Voltage on XTAL1- and XTAL2-pin | −0.3 | +3.6 | V |
| $T_{ST}$ | Storage temperature | −55 | +150 | °C |
| $T_J$ | Junction Temperature (Note 4) | −40 | +155 | °C |
| $V_{HBM}$ | Human Body Model electronic discharge immunity (Note 5) | −2 | +2 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Convention: currents flowing in the circuit are defined as positive.
2. VBUS2, VSS1, VSS2, VSSA and VSSD form the common ground. They are hard connected to the PCB ground layer.
3. Room temperature, 27 Ω shunt resistor for transmitter, 250 mA over temperature range.
4. Normal performance within the limitations is guaranteed up to the Thermal Warning level. Between Thermal Warning and Thermal Shutdown temporary loss of function or degradation of performance (which ceases after the disturbance ceases) is possible.
5. According to JEDEC JESD22-A114.



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## RECOMMENDED OPERATING RANGES

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

**Table 3. OPERATING RANGES**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{BUS1}$ | VBUS1 Voltage (Note 6) | +20 | +33 | V |
| $V_{DD}$ | Digital and Analog Supply Voltage (VDDD- and VDDA-pin) | +3.13 | +3.47 | V |
| $V_{IN}$ | Input Voltage DC-DC Converter 1 and 2 | (Note 7) | +33 | V |
| $V_{CCP}$ | Input Voltage at CCP-pin | −10.5 | +14.5 | V |
| $V_{CAV}$ | Input Voltage at CAV-pin | 0 | +3.3 | V |
| $V_{DD1}$ | Input Voltage on VDD1-pin | +3.13 | +3.47 | V |
| $V_{DD1M}$ | Input Voltage on VDD1M-pin | +3.13 | +3.57 | V |
| $V_{DD2}$ | Input Voltage on VDD2−pin | +1.2 | +21 | V |
| $V_{DD2MC}$ | Input Voltage on VDD2MC-pin | +1.2 | +21.1 | V |
| $V_{DD2MV}$ | Input Voltage on VDD2MV-pin | +1.2 | VDD | V |
| $V_{DIG}$ | Input Voltage on pins nV20VEN, nDC2EN, RXD and XCLKC | 0 | VDD | V |
| $V_{FANIN}$ | Input Voltage on FANIN-pin | 0 | 3.6 | V |
| $f_{clk}$ | Clock Frequency External Quartz | 16 | | MHz |
| $T_A$ | Ambient Temperature | −40 | +105 | °C |
| $T_J$ | Junction Temperature (Note 8) | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Voltage indicates DC value. With equalization pulse bus voltage must be between 11 V and 45 V.
7. Minimum operating voltage on VIN-pin should be at least 1 V larger than the highest value of VDD1 and VDD2.
8. Higher junction temperature can result in reduced lifetime.



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**Table 4. DC PARAMETERS**
(The DC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| $V_{BUS1}$ | VBUS1 | Bus DC voltage | Excluding active and equalization pulse | 20 | | 33 | V |
| $I_{BUS1_Int}$ | VBUS1 | Bus Current Consumption | $V_{BUS}$ = 30 V, $I_{BUS}$ = 10mA, DC2, V20V disabled, no crystal or clock | | 1.25 | 1.70 | mA |
| | | | $V_{BUS}$ = 20 V, $I_{BUS}$ = 40 mA | | 2.75 | 3.40 | |
| $V_{BUSH}$ | VBUS1 | Undervoltage release level | $V_{BUS1}$ rising, see Figure 4 | 17.1 | 18.0 | 18.9 | V |
| $V_{BUSL}$ | VBUS1 | Undervoltage trigger level | $V_{BUS1}$ falling, see Figure 4 | 15.9 | 16.8 | 17.7 | V |
| $V_{BUS_Hyst}$ | VBUS1 | Undervoltage hysteresis | | 0.6 | | | V |
| $V_{DDD}$ | VDDD | Digital Power Supply | | 3.13 | 3.3 | 3.47 | V |
| $V_{DDA}$ | VDDA | Analog Power Supply | | 3.13 | 3.3 | 3.47 | V |
| $V_{AUX}$ | | Auxiliary Supply | Internal supply, for info only | 2.8 | 3.3 | 3.6 | V |
| **KNX BUS COUPLER** | | | | | | | |
| $\Delta I_{coupler}/\Delta t$ | VBUS1 | Bus Coupler Current Slope Limitation | FANIN floating, $V_{FILT} > V_{FILTH}$ | | 0.40 | 0.50 | A/s |
| | | | FANIN = GND, VFILT > VFILTH | | 0.80 | 1.00 | |
| | | | Resistor R6 = 10k, $V_{FILT} > V_{FILTH}$ | | 1.51 | 1.95 | |
| | | | Resistor R6 = 13.3k, $V_{FILT} > V_{FILTH}$ | | 1.17 | 1.47 | |
| | | | Resistor R6 = 20k, $V_{FILT} > V_{FILTH}$ | | 0.78 | 0.98 | |
| | | | Resistor R6 = 42.2k, $V_{FILT} > V_{FILTH}$ | | 0.37 | 0.48 | |
| | | | Resistor R6 = 93.1k, $V_{FILT} > V_{FILTH}$ | | 0.17 | 0.23 | |
| $I_{coupler_lim, startup}$ | VBUS1 | Bus Coupler Startup Current Limitation | FANIN floating, $V_{FILT} > V_{FILTH}$ | 20.0 | 25.0 | 30.0 | mA |
| | | | FANIN = GND, $V_{FILT} > V_{FILTH}$ | 40.0 | 50.0 | 60.0 | |
| | | | Resistor R6 = 10k, $V_{FILT} > V_{FILTH}$ | 45.0 | 72.2 | 114.0 | |
| | | | Resistor R6 = 13.3k, $V_{FILT} > V_{FILTH}$ | 45.0 | 70.7 | 86.0 | |
| | | | Resistor R6 = 20k, $V_{FILT} > V_{FILTH}$ | 40.0 | 48.5 | 57.5 | |
| | | | Resistor R6 = 42.2k, $V_{FILT} > V_{FILTH}$ | 19.5 | 23.4 | 27.8 | |
| | | | Resistor R6 = 93.1k, $V_{FILT} > V_{FILTH}$ | 9.4 | 11.3 | 13.1 | |
| $I_{coupler_lim}$ | VBUS1 | Bus Coupler Current Limitation | FANIN floating, $V_{FILT} > V_{FILTH}$ | 10.8 | 11.4 | 12 | mA |
| | | | FANIN = GND, $V_{FILT} > V_{FILTH}$ | 20.5 | 22.3 | 24 | |
| | | | Resistor R6 = 10k, $V_{FILT} > V_{FILTH}$ | 39.6 | 43.9 | 47.0 | |
| | | | Resistor R6 = 13.3k, $V_{FILT} > V_{FILTH}$ | 30.0 | 33.0 | 35.2 | |
| | | | Resistor R6 = 20k, $V_{FILT} > V_{FILTH}$ | 20.2 | 22.1 | 23.6 | |
| | | | Resistor R6 = 42.2k, $V_{FILT} > V_{FILTH}$ | 9.4 | 10.7 | 11.9 | |
| | | | Resistor R6 = 93.1k, $V_{FILT} > V_{FILTH}$ | 4.2 | 5.1 | 6.0 | |
| $V_{coupler_drop}$ | VBUS1, VFILT | Coupler Voltage Drop ($V_{coupler_drop} = V_{BUS1} - V_{FILT}$) | $I_{BUS1}$ = 10 mA | | 1.72 | 2.32 | V |
| | | | $I_{BUS1}$ = 20 mA | | 2.34 | 2.80 | |
| | | | $I_{BUS1}$ = 30 mA | | 2.94 | 3.40 | |
| | | | $I_{BUS1}$ = 40 mA | | 3.57 | 4.25 | |
| $V_{FILTH}$ | VFILT | Undervoltage release level | $V_{FILT}$ rising, see Figure 5 | 10.1 | 10.6 | 11.2 | V |
| $V_{FILTL}$ | VFILT | Undervoltage trigger level | $V_{FILT}$ falling, see Figure 5 | 8.4 | 8.9 | 9.4 | V |



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**Table 4. DC PARAMETERS** (continued)
(The DC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **FIXED DC-DC CONVERTER** | | | | | | | |
| $V_{IN}$ | VIN | Input Voltage | | 4.47 | | 33 | V |
| $V_{DD1}$ | VDD1 | Output Voltage | | 3.13 | 3.3 | 3.47 | V |
| $V_{DD1_rip}$ | | Output Voltage Ripple | $V_{IN}$ = 25 V, $I_{DD1}$ = 40 mA, L1 = 220 μH | | 40 | | mV |
| $I_{DD1_lim}$ | | Overcurrent Threshold | $R_2$ = 1 Ω | −100 | | −200 | mA |
| $\eta_{VDD1}$ | | Power Efficiency (DC Converter Only) | $V_{in}$ = 25 V, $I_{DD1}$ = 35 mA, $L_1$ = 220 μH (1.26 Ω ESR) | | 90 | | % |
| $R_{DS(on)_p1}$ | | $R_{DS(on)}$ of power switch | See Figure 12 | | | 8 | Ω |
| $R_{DS(on)_n1}$ | | $R_{DS(on)}$ of flyback switch | See Figure 12 | | | 4 | Ω |
| $V_{DD1M}$ | VDD1M | Input voltage VDD1M-pin | | | | 3.57 | V |
| **ADJUSTABLE DC-DC CONVERTER** | | | | | | | |
| $V_{IN}$ | VIN | Input Voltage | | $V_{DD2}$ + 1 | | 33 | V |
| $V_{DD2}$ | VDD2 | Output Voltage | $V_{IN} \geq V_{DD2}$ | 1.2 | | 21 | V |
| $V_{DD2H}$ | | Undervoltage release level | $V_{DD2}$ rising, see Figure 6 | | 0.9 x $V_{DD2}$ | | V |
| $V_{DD2L}$ | | Undervoltage trigger level | $V_{DD2}$ falling, see Figure 6 | | 0.8 x $V_{DD2}$ | | V |
| $V_{DD2_rip}$ | | Output Voltage Ripple | $V_{IN}$ = 25 V, $V_{DD2}$ = 3.3 V, $I_{DD2}$ = 40 mA, L2 = 220 μH | | 40 | | mV |
| $I_{DD2_lim}$ | | Overcurrent Threshold | $R_3$ = 1 Ω | −100 | | −250 | mA |
| $\eta_{VDD2}$ | | Power Efficiency (DC Converter Only) | $V_{in}$ = 25 V, $V_{DD2}$ = 3.3 V, $I_{DD2}$ = 35 mA, $L_2$ = 220 μH (1.26 Ω ESR) | | 90 | | % |
| $R_{DS(on)_p2}$ | | $R_{DS(on)}$ of power switch | See Figure 12 | | | 8 | Ω |
| $R_{DS(on)_n2}$ | | $R_{DS(on)}$ of flyback switch | See Figure 12 | | | 4 | Ω |
| $V_{DD2M}$ | VDD2MC | Input voltage VDD2MC-pin | | | | 21.1 | V |
| $R_{VDD2M}$ | VDD2MV | Input Resistance VDD2MV-pin | | 1 | | | MΩ |
| $I_{leak,vsw2}$ | | Half-bridge leakage | | | | 20 | μA |
| **V20V REGULATOR** | | | | | | | |
| $V_{20V}$ | V20V | V20V Output Voltage | $I_{20V} < I_{20V_lim}$, $V_{FILT} \geq 21$ V | 18 | 20 | 22 | V |
| $I_{20V_lim}$ | | V20V Output Current Limitation | $R_6$ > 250 kΩ | 4.34 | 5.68 | 8.00 | mA |
| | | | 10 kΩ < $R_6$ < 93.1 kΩ | 132.0/$R_6$ | 273.4/$R_6$ | 392.0/$R_6$ | A |
| | | | $R_6$ < 2 kΩ | 9.52 | 12.37 | 16.00 | mA |
| $V_{20VH}$ | | V20V Undervoltage release level | $V_{20V}$ rising, see Figure 7 | 14.2 | 15.0 | 15.8 | V |
| $V_{20VL}$ | | V20V Undervoltage trigger level | $V_{20V}$ falling, see Figure 7 | 13.2 | 14.0 | 14.8 | V |
| $V_{20V_hyst}$ | | V20V Undervoltage hysteresis | $V_{20V_hyst} = V_{20VH} - V_{20VL}$ | | 1.0 | | V |
| **XTAL OSCILLATOR** | | | | | | | |
| $V_{XTAL}$ | XTAL1, XTAL2 | Voltage on XTAL-pin | | | | $V_{DDD}$ | V |
| **FAN-IN CONTROL** | | | | | | | |
| $I_{pu,fanin}$ | FANIN | Pull-Up Current FANIN-pin | FANIN shorted to GND, Pull-up connected to $V_{AUX}$ | 10 | 20 | 40 | μA |



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**Table 4. DC PARAMETERS** (continued)
(The DC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | |
| $V_{IL}$ | nV20VEN, nDC2EN, RXD, XCLKC | Logic Low Threshold | | 0 | | 0.7 | V |
| $V_{IH}$ | | Logic High Threshold | | 2.65 | | $V_{DDD}$ | V |
| $R_{DOWN}$ | XCLKC | Internal Pull-Down Resistor | | 5 | 10 | 28 | kΩ |
| **DIGITAL OUTPUTS** | | | | | | | |
| $V_{OL}$ | TXD, XCLK | Logic low output level | | 0 | | 0.4 | V |
| $V_{OH}$ | | Logic high output level | | $V_{DDD}$ − 0.45 | | $V_{DDD}$ | V |
| $I_L$ | XCLK | Load Current | | | | 8 | mA |
| | TXD | | | | | 4 | mA |
| $V_{OL}$ | SAVEB, RESETB | Logic low level open drain | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $R_{up}$ | | Internal Pull-up Resistor | | 20 | 40 | 80 | kΩ |
| **TEMPERATURE MONITOR** | | | | | | | |
| $T_{TW}$ | | Thermal Warning | Rising temperature See Figure 8 | 105 | 115 | 125 | °C |
| $T_{TSD}$ | | Thermal shutdown | Rising temperature See Figure 8 | 130 | 140 | 150 | °C |
| $T_{Hyst}$ | | Thermal Hysteresis | See Figure 8 | 5 | 11 | 15 | °C |
| ΔT | | Delta $T_{TSD}$ and $T_{TW}$ | See Figure 8 | | 21.7 | | °C |
| **PACKAGE THERMAL RESISTANCE VALUE** | | | | | | | |
| $R_{\theta,ja}$ | | Thermal Resistance Junction-to-Ambient | Simulated Conform JEDEC JESD-51, (2S2P) | | 30 | | K/W |
| | | | Simulated Conform JEDEC JESD-51, (1S0P) | | 60 | | K/W |
| $R_{\theta,jp}$ | | Thermal Resistance Junction-to-Exposed Pad | | | 0.95 | | K/W |

**Table 5. AC PARAMETERS**
(The AC parameters are given for a device operating within the Recommended Operating Conditions unless otherwise specified.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| $t_{BUS_FILTER}$ | VBUS1 | VBUS1 filter time | See Figure 4 | | 2 | | ms |
| **FIXED DC-DC CONVERTER** | | | | | | | |
| $t_{VSW1_rise}$ | VSW1 | Rising slope at VSW1-pin | | | 0.45 | | V/ns |
| $t_{VSW1_fall}$ | | Falling slope at VSW1-pin | | | 0.6 | | V/ns |
| **ADJUSTABLE DC-DC CONVERTER** | | | | | | | |
| $t_{VSW2_rise}$ | VSW2 | Rising slope at VSW2-pin | | | 0.45 | | V/ns |
| $t_{VSW2_fall}$ | | Falling slope at VSW2-pin | | | 0.6 | | V/ns |
| **XTAL OSCILLATOR** | | | | | | | |
| $f_{XTAL}$ | XTAL1, XTAL2 | XTAL Oscillator Frequency | | | 16 | | MHz |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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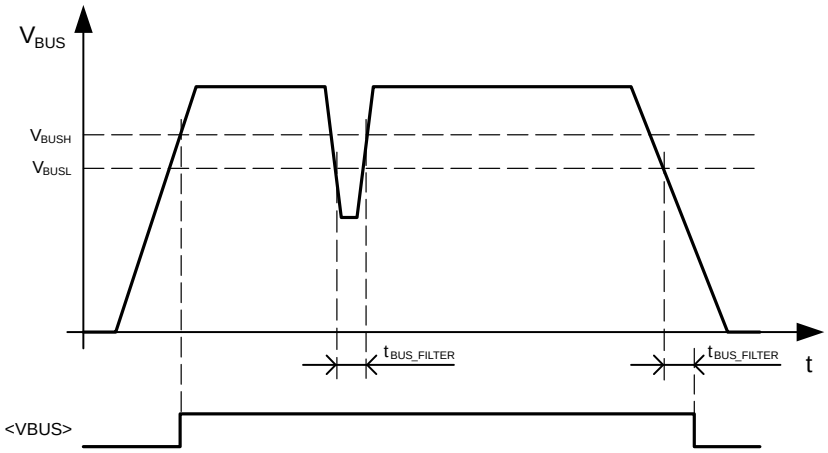
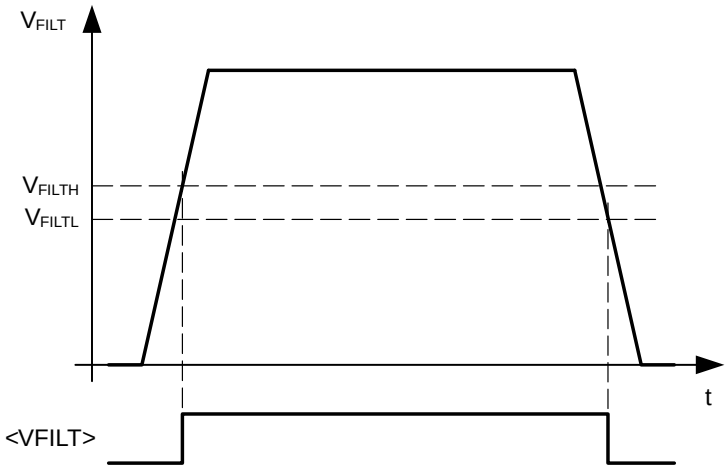


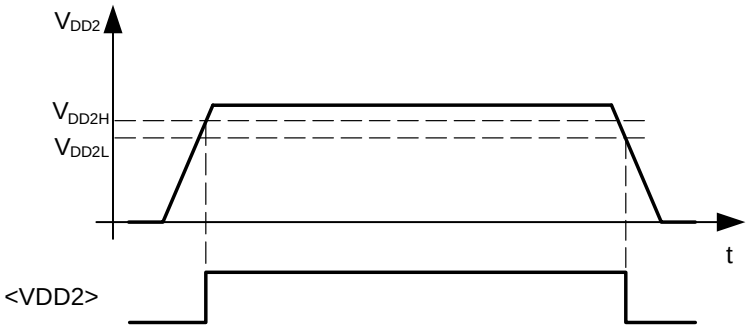

Comments:
<VBUS> is an internal signal which ca be verified with the Internal State Service.

**Figure 4. Bus Voltage Undervoltage Threshold**




Comments:
<VFILT> is an internal signal which ca be verified with the Internal State Service.

**Figure 5. VFILT Undervoltage Threshold**




Comments:
<VDD2> is an internal signal which ca be verified with the Internal State Service.

**Figure 6. VDD2 Undervoltage Thresholds**



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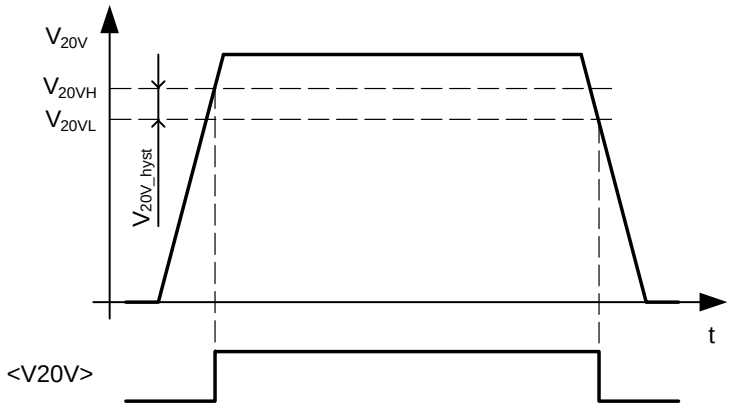
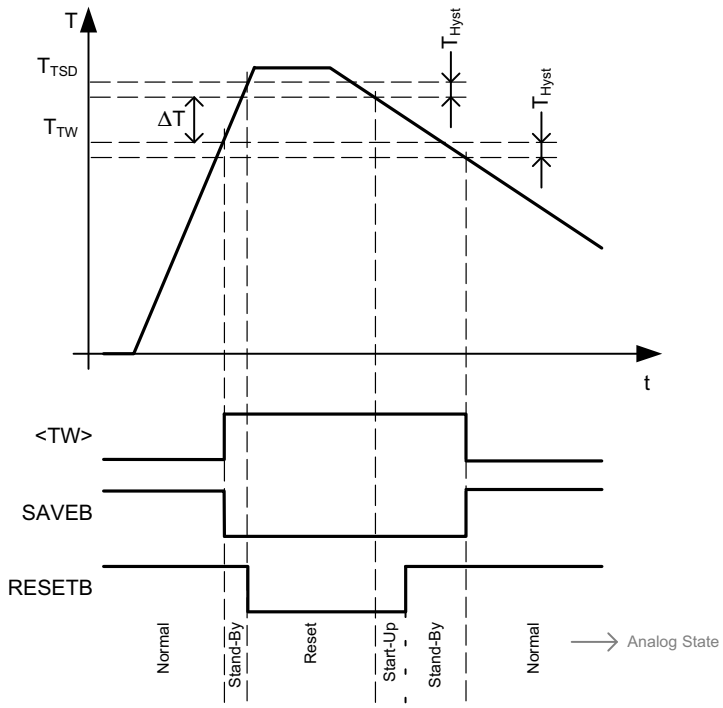



Comments:
<V20V> is an internal signal which ca be verified with the Internal State Service.

**Figure 7. V20V Undervoltage Threshold levels**




Comments:
− <TW> is an internal signal which can be verified with the System State Service
− No communication possible when RESETB is low!
− It's assumed all voltage supplies are withing their operating condition.

**Figure 8. Temperature Monitoring Levels**



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## TYPICAL APPLICATION SCHEMATICS

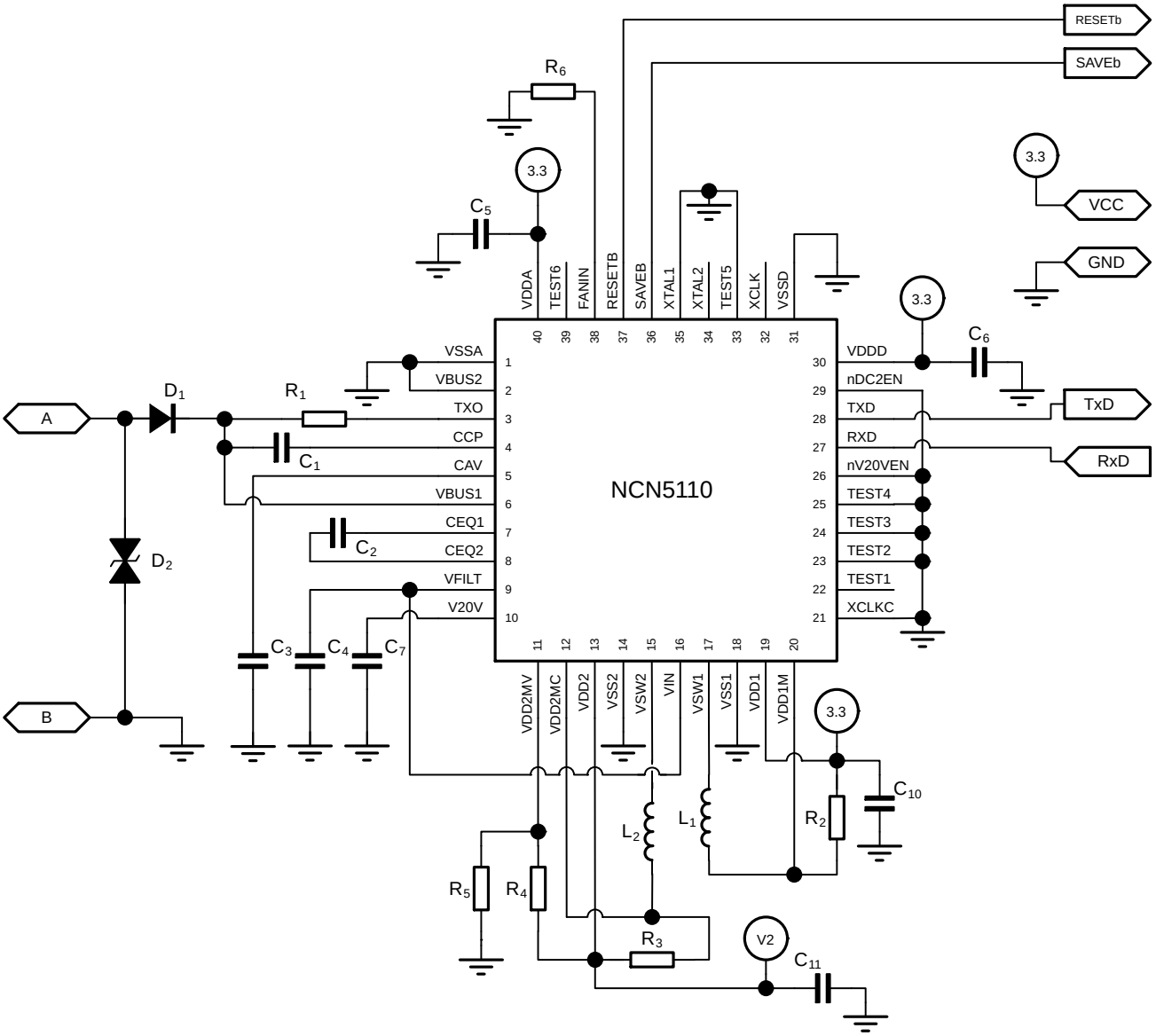


**Figure 9. Typical Application Schematic, 20 mA Bus Current Limit and 1.0 mA/ms Bus Current Slopes**



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**Table 6. EXTERNAL COMPONENTS LIST AND DESCRIPTION**

| Comp. | Function | Min | Typ | Max | Unit | Remarks | Notes |
|---|---|---|---|---|---|---|---|
| $C_1$ | AC coupling capacitor | 42.3 | 47 | 51.7 | nF | 50 V, Ceramic | 9 |
| $C_2$ | Equalization capacitor | 198 | 220 | 242 | nF | 50 V, Ceramic | 9 |
| $C_3$ | Capacitor to average bus DC voltage | 80 | 100 | 120 | nF | 50 V, Ceramic | 9 |
| $C_4$ | Storage and filter capacitor VFILT | 12.5 | 100 | 4000 | μF | 35 V | 9, 15 |
| $C_5$ | VDDA HF rejection capacitor | 80 | 100 | | nF | 6.3 V, Ceramic | |
| $C_6$ | VDDD HF rejection capacitor | 80 | 100 | | nF | 6.3 V, Ceramic | |
| $C_7$ | Load Capacitor V20V | | 1 | | μF | 35 V, Ceramic, ESR < 2 Ω | 12, 13, 15 |
| $C_{10}$ | Load capacitor VDD1 | 8 | 10 | | μF | 6.3 V, Ceramic, ESR < 0.1 Ω | |
| $C_{11}$ | Load capacitor VDD2 | 8 | 10 | | μF | Ceramic, ESR < 0.1 Ω | 10 |
| $R_1$ | Shunt resistor for transmitting | 24.3 | 27 | 29.7 | Ω | 1 W | 9 |
| $R_2$ | DC1 sensing resistor | 0.47 | 1 | 10 | Ω | 1/16 W | |
| $R_3$ | DC2 sensing resistor | 0.47 | 1 | 10 | Ω | 1/16 W | |
| $R_4$ | Voltage divider to specify VDD2 | 0 | | | Ω | 1/16 W, see p15 for calculating the exact value | |
| $R_5$ | | 0 | | 1000 | kΩ | | |
| $L_1$, $L_2$ | DC1/DC2 inductor | | 220 | | μH | | |
| $D_1$ | Reverse polarity protection diode | SS16 | | | | | 11 |
| $D_2$ | Voltage suppressor | 1SMA40CA | | | | | |
| $R_6$ | Fan-In Programming Resistor | 10 | | 93.1 | kΩ | 1% precision | 14 |

9. Component must be between minimum and maximum value to fulfill the KNX requirement.
10. Voltage of capacitor depends on VDD2 value defined by R4 and R5. See p16 for more details on defining VDD2 voltage value.
11. Reverse polarity diode is mandatory to fulfill the KNX requirement.
12. It's allowed to short this pin to VFILT-pin
13. High capacitor value might affect the start up time
14. If no resistor connected or pulled up to 3.3 V the KNX device should be certified as a bus load of 10 mA. If shorted to ground the KNX device should be certified as a bus load of 20 mA. If a resistor to ground is connected between 10 kΩ and 93.1 kΩ the device should be certified as a bus load of 10 mA (42.2 k), 20 mA (20 k), 30 mA (13.3 k) or 40 mA (10 k).
15. Total charge of C4 and C7 may not be higher than 121 mC to fulfill the KNX requirement.



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## ANALOG FUNCTIONAL DESCRIPTION

Because NCN5110 follows the KNX standard only a brief description of the KNX related blocks is given in this datasheet. Detailed information on the KNX Bus can be found on the KNX website (www.knx.org) and in the KNX standards.

### KNX Bus Interfacing

Each bit period is 104 µs. Logic 1 is simply the DC level of the bus voltage which is between 20 V and 33 V. Logic 0 is encoded as a drop in the bus voltage with respect to the DC level. Logic 0 is known as the active pulse.

The active pulse is produced by the transmitter and is ideally rectangular. It has a duration of 35 µs and a depth between 6 and 9 V ($V_{act}$). Each active pulse is followed by an equalization pulse with a duration of 69 µs. The latter is an abrupt jump of the bus voltage above the DC level followed by an exponential decay down to the DC level. The equalization pulse is characterized by its height $V_{eq}$ and the voltage $V_{end}$ reached at the end of the equalization pulse.

See the KNX Twisted Pair Standard (KNX TP1-256) for more detailed KNX information.

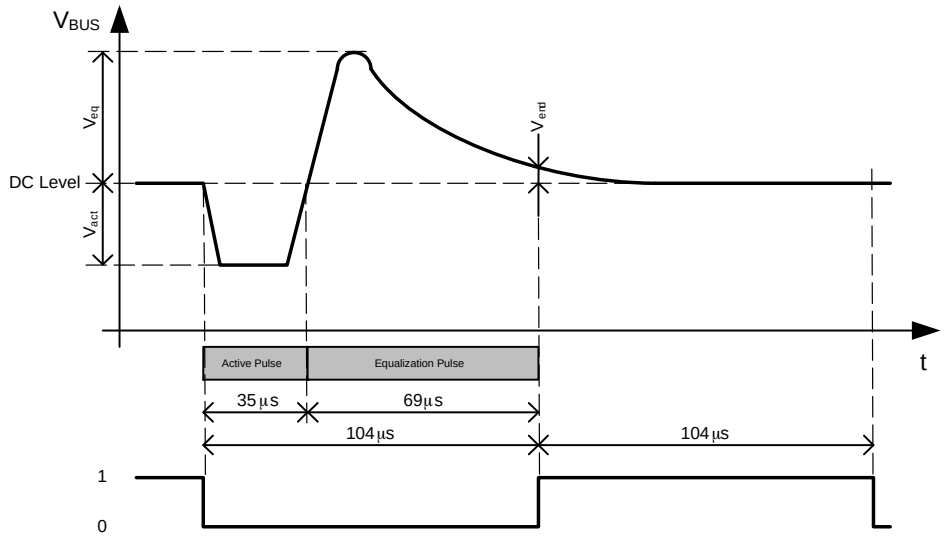


**Figure 10. KNX Bus Voltage versus Digital Value**

### KNX Bus Transmitter

The purpose of the transmitter is to produce an active pulse (see Figure 10) between 6 V and 9 V regardless of the bus impedance (Note 1). In order to do this the transmitter will sink as much current as necessary until the bus voltage drops by the desired amount. The transmitter will produce an active pulse whenever the TX pin is brought high. It is up to the microcontroller to provide the bit-level coding and provide the correct active pulse duration.

### KNX Bus Receiver

The receiver detects the beginning and the end of the active pulse. The detection threshold for the start of the active pulse is −0.61 V (typ.) below the average bus voltage. The detection threshold for the end of the active pulse is −0.38 V (typ.) below the average bus voltage yielding a typical hysteresis of 0.23 V.

The receiver also has a blanking time of 24 µs. This is the minimum time that the bus voltage must remain below the receiver threshold to detect the active pulse.

Prior to FPCN26053XB, the detection thresholds for the start and end of the active pulse were −0.45 V and −0.2 V (typ.), yielding a typical hysteresis of 0.25 V. The new thresholds are slightly more robust in highly−loaded networks or during extended frame communication.

The result of this detection is available as a pulse on the RXD pin.

### Bus Coupler

The role of the bus coupler is to extract the DC voltage from the bus and provide a stable voltage supply for the purpose of powering the NCN5110. This stable voltage supplied by the bus coupler is called VFILT, and will follow the average bus voltage. The bus coupler also makes sure that the current drawn from the bus changes very slowly. For this a large filter capacitor is used on the VFILT-pin. Abrupt load current steps are absorbed by the filter capacitor. Long-term stability requires that the average bus coupler input current is equal to the average (bus coupler) load current. This is shown by the parameter $\Delta I_{coupler}/\Delta t$, which indicated the bus current slope limit. The bus coupler will also limit the current to a maximum of $I_{coupler_lim}$. At startup, this current limit is increased to $I_{coupler_lim,startup}$ to allow for fast charging of the VFILT bulk capacitance.

There are 4 conditions that determine the dimensioning of the VFILT capacitor.

1. Maximum bus impedance is specified in the KNX Twisted Pair Standard



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First, the capacitor value should be between 12.5 μF and 4000 μF to garantuee proper operation of the part.

The next requirement on the VFILT capacitor is determined by the startup time of the system. According to the KNX specification, the total startup time must be below 10s. This time is comprised of the time to charge the VFILT capacitor to 12 V (where the DCDC convertor becomes operatonal) and the startup time of the rest of the system $t_{startup,system}$. This gives the following formula:

$$C < \frac{\left(10s - t_{startup,system}\right) \times I_{coupler_lim,startup}}{VFILTH}$$

The third limit on VFILT capacitor value is the required capacitor value to filter out current steps $\Delta I_{step}$ of the system without going into reset.

$$C > \frac{\Delta I_{step}^{2}}{\left(2 \times \left(V_{BUS1} - V_{coupler_drop} - V_{FILTL}\right) \times I_{slope}\right)}$$

The last condition on the size of VFILT is the desired warning time twarning between SAVEB and RESETB in case the bus voltage drops away. This is determined by the current consumption of the system Isystem.

$$C > \frac{I_{system} \times \left(t_{warning} + t_{busfilter}\right)}{\left(V_{BUS1} - V_{coupler_drop} - V_{FILTL}\right)}$$

The bus coupler is implemented as a linear voltage regulator. For efficiency purpose, the voltage drop over the bus coupler is kept minimal (see Table 4).

### KNX Impedance Control

The impedance control circuit defines the impedance of the bus device during the active and equalization pulses. The impedance can be divided into a static and a dynamic component, the latter being a function of time. The static impedance defines the load for the active pulse current and the equalization pulse current. The dynamic impedance is produced by a block, called an equalization pulse generator, that reduces the device current consumption (i.e. increases the device impedance) as a function of time during the equalization phase so as to return energy to the bus.

### Fixed and Adjustable DC-DC Converter

The device contains two DC-DC buck converters, both supplied from VFILT.

DC1 provides a fixed voltage of 3.3 V. This voltage is used as an internal low voltage supply ($V_{DDA}$ and $V_{DDD}$) but can also be used to power external devices (VDD1-pin). DC1 is automatically enabled during the power-up procedure (see Analog State Diagram, p19).

DC2 provides a programmable voltage by means of an external resistor divider. It is not used as an internal voltage supply making it not mandatory to use this DC-DC converter (if not needed, tie the VDD2MV pin to VDD1).

DC2 will only be enabled when the nDC2EN pin is pulled low. When nDC2EN is pulled to VDDD, the DC2 controller is disabled.

The voltage divider can be calculated as follows:

$$R_4 = R_5 \times \frac{V_{DD2} - 1.2}{1.2} \qquad \text{(eq. 1)}$$

Both DC-DC converters make use of slope control to improve EMC performance (see Table 5). To operate DC1 and DC2 correctly, the voltage on the VIN-pin should be higher than the highest value of DC1 and DC2.

Although both DC-DC converters are capable of delivering 100 mA, the maximum current capability will not always be usable. One always needs to make sure that the KNX bus power consumption stays within the KNX specification. The maximum allowed current for the DC-DC converters and V20V regulator can be estimated as next:

$$\frac{V_{BUS} \times \left(I_{BUS} - I_{20V}\right)}{2 \times \left[\left(V_{DD1} \times I_{DD1}\right) + \left(V_{DD2} \times I_{DD2}\right)\right]} \geq 1 \qquad \text{(eq. 2)}$$

$I_{BUS}$ will be limited by the KNX standard and should be lower or equal to $I_{coupler}$ (see Table 4). Minimum $V_{BUS}$ is 20 V (see KNX standard). $V_{DD1}$ and $V_{DD2}$ can be found back in Table 4. $I_{DD1}$, $I_{DD2}$ and $I_{20V}$ must be chosen in a correct way to be in line with the KNX specification (Note 2).

Although DC2 can operate up to 21 V, it will not be possible to generate this 21 V under all operating conditions. See application note AND9135 for defining the optimum inductor and capacitor of the DC-DC converters. When using low series resistance output capacitors on DC2, it is advised to split the current sense resistor as shown in Figure 12 to reduce ripple current for low load conditions.

### V20V Regulator

This is the 20 V low drop linear voltage regulator used to supply external devices. As it draws current from VFILT, this current is seen without any power conversion directly at the VBUS1 pin.

The V20V regulator is enabled by pulling the nV20VEN pin low. When the nV20VEN pin is pulled high, the 20V regulator is disabled. When the V20V regulator is not used, no load capacitor needs to be connected (see C7 of Figure 9). Connect V20V-pin with VFILT-pin in this case.

The 20 V regulator has a current limit that depends on the FANIN resistor value. In Table 4, the typical value of the current limit at startup is given as $I_{20V_lim}$.

2. The formula is for a typical KNX application. It's only given as guidance and does not guarantee compliance with the KNX standard.



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### Xtal Oscillator

An analog oscillator cell generates an optional clock of 16 MHz.

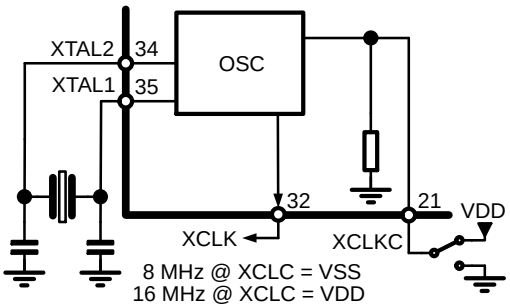


**Figure 11. XTAL Oscillator**

The XCLK-pin can be used to supply a clock signal to the host controller.

After power-up, a 4 MHz (Note 3) clock signal will be present on the XCLK-pin during Stand-By. When Normal State is entered, a 8 or 16 MHz clock signal will be present on the XCLK-pin. See also Figure 14. To output an 8 MHz clock on the XCLK pin, the XCLKC pin must be pulled to ground. When the XCLKC pin is pulled up to $V_{DDD}$, the XCLK pin will output a 16 MHz clock signal.

When Normal State is left and Stand-By State is re-entered due to an issue different than an Xtal issue, the 8 or 16 MHz clock signal will still be present on the XCLK-pin during the Stand-By State. If however Stand-By is entered from Normal State due to an Xtal issue, the 4 MHz clock signal will be present on the XCLK-pin. See also Table 7.

### FANIN-pin

The FANIN-pin defines the maximum allowed bus current and bus current slopes. If the FANIN-pin is kept floating, pulled up to $V_{DD}$, or pulled down with a resistance higher than 250 kΩ, NCN5110 will limit the KNX bus current slopes to 0.5 mA/ms at all times. NCN5110 will also limit the KNX bus current to 30 mA during start-up. During normal operation, NCN5110 is capable of taking 10.6 mA (= $I_{coupler}$) from the KNX bus for supplying external loads (DC1, DC2 and V20V).

If the FANIN-pin is pulled to ground with a resistance smaller than 2 kΩ the operation is similar as above with the exception that the KNX bus current slopes will be limited to 1 mA/ms at all times, the KNX bus current will be limited to 60 mA during start-up and up to 20.5 mA ($I_{coupler}$) can be taken from the KNX bus during normal operation. When the FANIN-pin is pulled to ground with a resistance between 10 kΩ and 93.1 kΩ, the current slope and current limit are defined by the values from Table 4. For different resistor values, the typical current limit can be approximated by the formula $I_{bus} = 0.0004 + 434/R_6$ A. Using different resistor values is, however, not recommended.

Definitions for Start-Up and Normal Operation (as given above) can be found in the KNX Specification.

### RESETB- and SAVEB-pin

The RESETB signal can be used to keep the host controller in a reset state. When RESETB is low this indicates that the bus voltage is too low for normal operation and that the fixed DC-DC converter has not started up. It could also indicate a Thermal Shutdown (TSD). The RESETB signal also indicates if communication between host and NCN5110 is possible.

The SAVEB signal indicates correct operation. When SAVEB goes low, this indicates a possible issue (loss of bus power or too high temperature) which could trigger the host controller to save critical data or go to a save state. SAVEB goes low immediately when VFILT goes below 14 V (due to sudden large current usage) or after 2 ms when VBUS goes below 20 V. RESETB goes low when VFILT goes below 12 V.

RESETB- and SAVEB-pin are open-drain pins with an internal pull-up resistor to $V_{DDD}$.

### Voltage Supervisors

NCN5110 has different voltage supervisors monitoring VBUS, VFILT, VDD2 and V20V. The general function of a voltage supervisor is to detect when a voltage is above or below a certain level. The levels for the different voltages monitored can be found back in Table 4 (see also Figures 4, 5, 6 and 7).

Depending on the voltage supervisor outputs, the device can enter different states (see Analog State Diagram, p19).

3. The 4 MHz clock signal is internally generated and will be less accurate as the crystal generated clock signal of 8 or 16 MHz.



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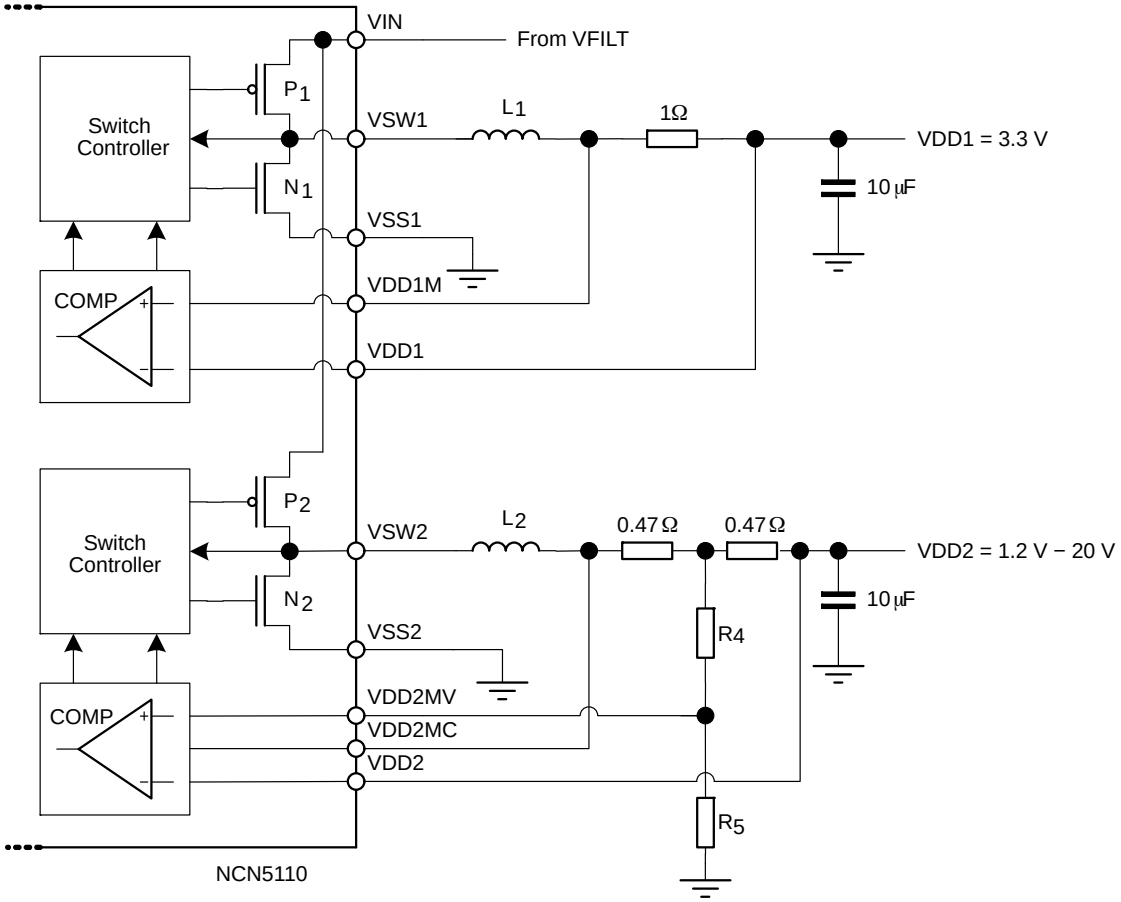


**Figure 12. Fixed (VDD1) and Adjustable (VDD2) DC-DC Converter**



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**Table 7. STATUS OF SEVERAL BLOCKS DURING THE DIFFERENT (ANALOG) STATES**

| State | Osc | XCLK | VDD1 | VDD2/V20V | COMMUNICATION | KNX |
|---|---|---|---|---|---|---|
| **Reset** | Off | Off | Off | Off | Inactive | Inactive |
| **Start-Up** | Off | Off | Start-up | Off | Inactive | Inactive |
| **Stand-By (Note 16)** | Off | 4 MHz | On | Start-Up | Active | Active |
| **Stand-By (Note 17)** | On (Note 19) | On (Note 19) | On | On (Note 20) | Active | Active |
| **Normal** | On | On (Note 18) | On | On | Active | Active |

16. Only valid when entering Stand-By from Start-Up State.
17. Only valid when entering Stand-By from Normal State.
18. 8 MHz or 16 MHz depending on XCLKC.
19. 4 MHz signal if Stand-By state was entered due to oscillator issue. Otherwise 8 MHz or 16 MHz clock signal.
20. Only operational if Stand-By state was not entered due to VDD2 or V20V issue.

**Temperature Monitor**

The device produces an over-temperature warning (TW) and a thermal shutdown warning (TSD). Whenever the junction temperature rises above the Thermal Warning level ($T_{TW}$), the SAVEB-pin will go low to signal the issue to the host controller. When the junction temperature is above TW, the host controller should undertake actions to reduce the junction temperature and/or store critical data.

When the junction temperature reaches Thermal Shutdown ($T_{TSD}$), the device will go to the Reset State and the analog and digital power supply will be stopped (to protect the device). The device will stay in the Reset State as long as the temperature stays above $T_{TSD}$.

If the temperature drops below $T_{TSD}$, Start-Up State will be entered (see also Figure 13). At the moment VDD1 is back up and the OTP memory is read, Stand-By State will be entered and RESETB will go high. Once the temperature has dropped below $T_{TW}$ and all voltages are high enough, Normal State will be entered. SAVEB will go high and KNX communication is again possible.

Figure 8 gives a better view on the temperature monitor.



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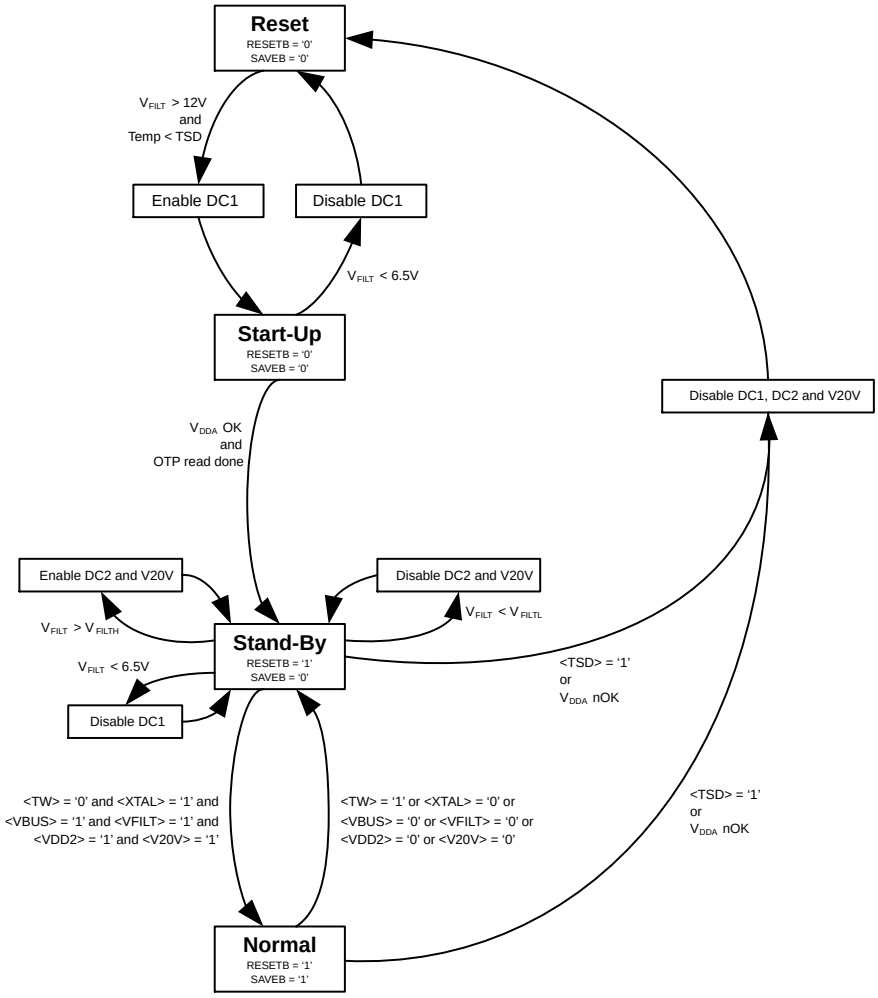
### Analog State Diagram

The analog state diagram of NCN5110 is given in Figure 13. The status of the DC-DC converters, V20V regulator and KNX communication during the different (analog) states is given in Table 7.

Figure 14 gives a detailed view on the start-up behavior of NCN5110. After applying the bus voltage, the filter capacitor starts to charge. During this Reset State, the current drawn from the bus is limited to $I_{coupler}$ (for details see the KNX Standards). Once the voltage on the filter capacitor reaches 10 V (typ.), the fixed DC-DC converter (powering VDDA) will be enabled and the device enters the Start-Up State. When $V_{DD1}$ gets above 2.8 V (typ.), the OTP memory is read out to trim some analog parameters (OTP memory is not accessible by the user). When done, the Stand-By State is entered and the RESETB-pin is made high. When $V_{FILT}$ is above $V_{FILTH}$ DC2 and V20V will be started. When the VBUS-, VFILT-, VDD2- and V20V-monitors are ok, the Normal State will be entered and SAVEB-pin will go high.

Figure 15 gives a detailed view on the shut-down behavior. If the KNX bus voltage drops below $V_{BUSL}$ for more than $t_{bus_filter}$, the Standy-By State is entered. SAVEB will go low to signal this. When VFILT drops below $V_{FILTL}$, DC2 and the V20V regulator will be switched off. When VFILT drops below 6.5 V (typ), DC1 will be switched off and $V_{DD1}$ drops below 2.8 V (typ.) the device goes to Reset State (RESETB low).




Remarks:
− <TW>, <XTAL>, <VBUS>, <VFILT>, <VDD2> and <V20V> are internal status bits
− <TSD> is an internal signal indicating a Thermal Shutdown. This internal signal cannot be read out.
− Although Reset State could be entered from Normal State on a TSD, Stand-By State will be entered first due to a TW.

**Figure 13. Analog State Diagram**



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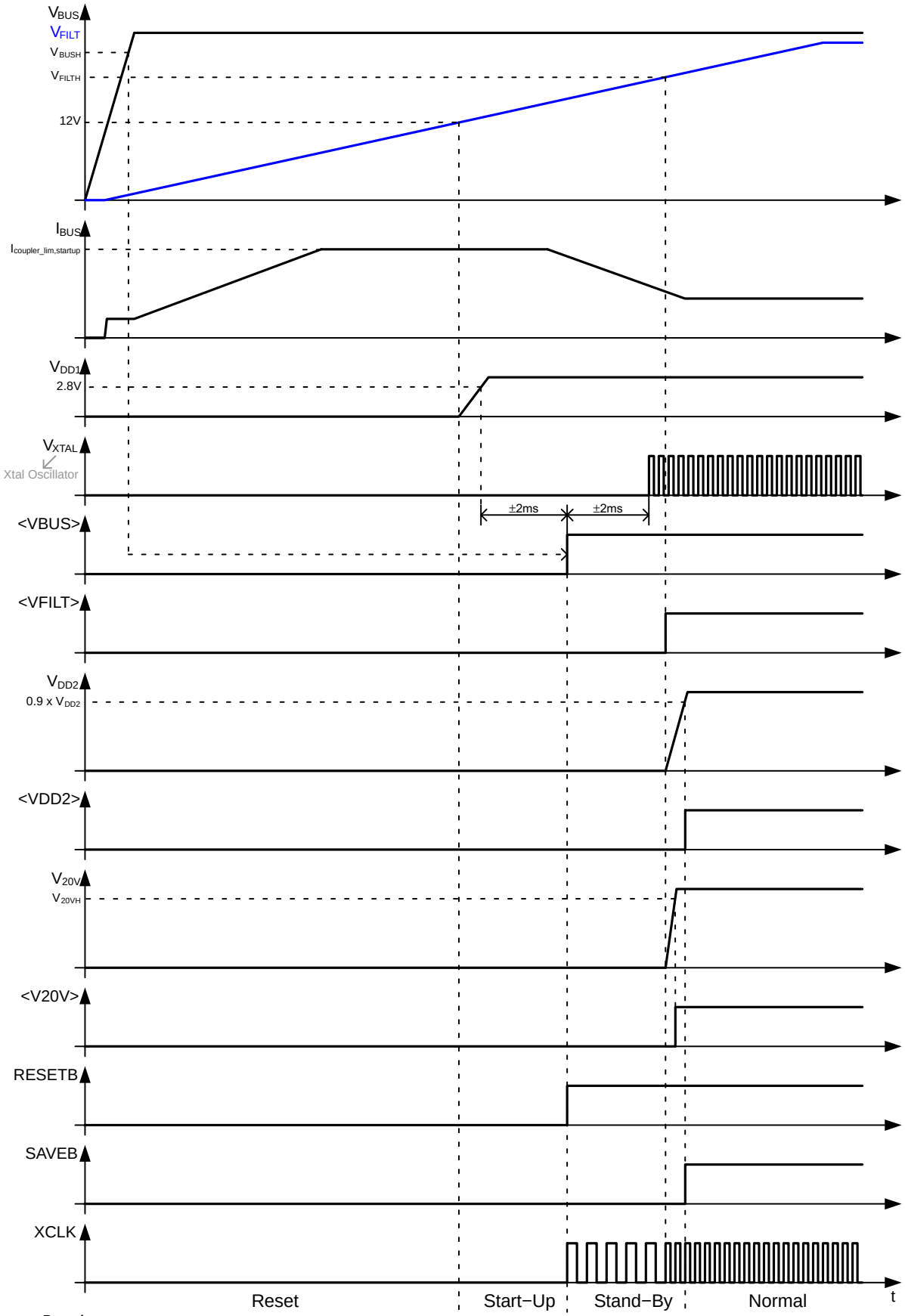


**Remarks:**
VDD1 directly connected to VDDA.

**Figure 14. Start−Up Behavior**



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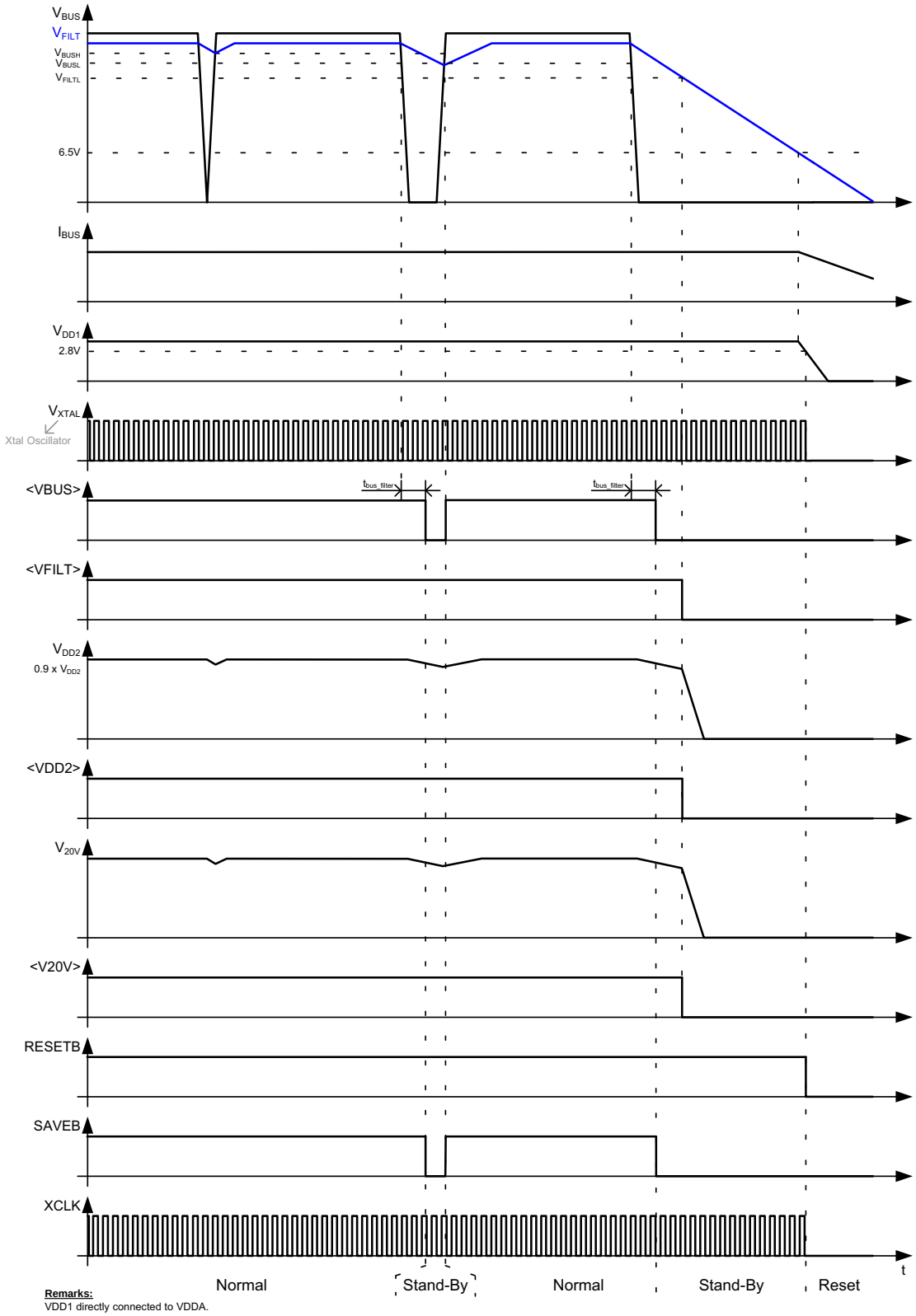


**Figure 15. Shut-Down Behavior**



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### Communication Interface

The NCN5110 communication pins (TxD and RxD) are connected immediately to the KNX transmitter/receiver. Bit level coding/decoding has to be done by the host controller. Keep in mind that the signals on the RXD- and TXD-pin are inverted. Figure 9 gives an application example.

### Layout Recommendation

Take extra care to keep the trace inductance between VBUS1 net and CCP pin on the PCB as small as possible by maximizing the trace thickness and reducing the length. As a rule of thumb, keep the trace length below approximately 5 mm.

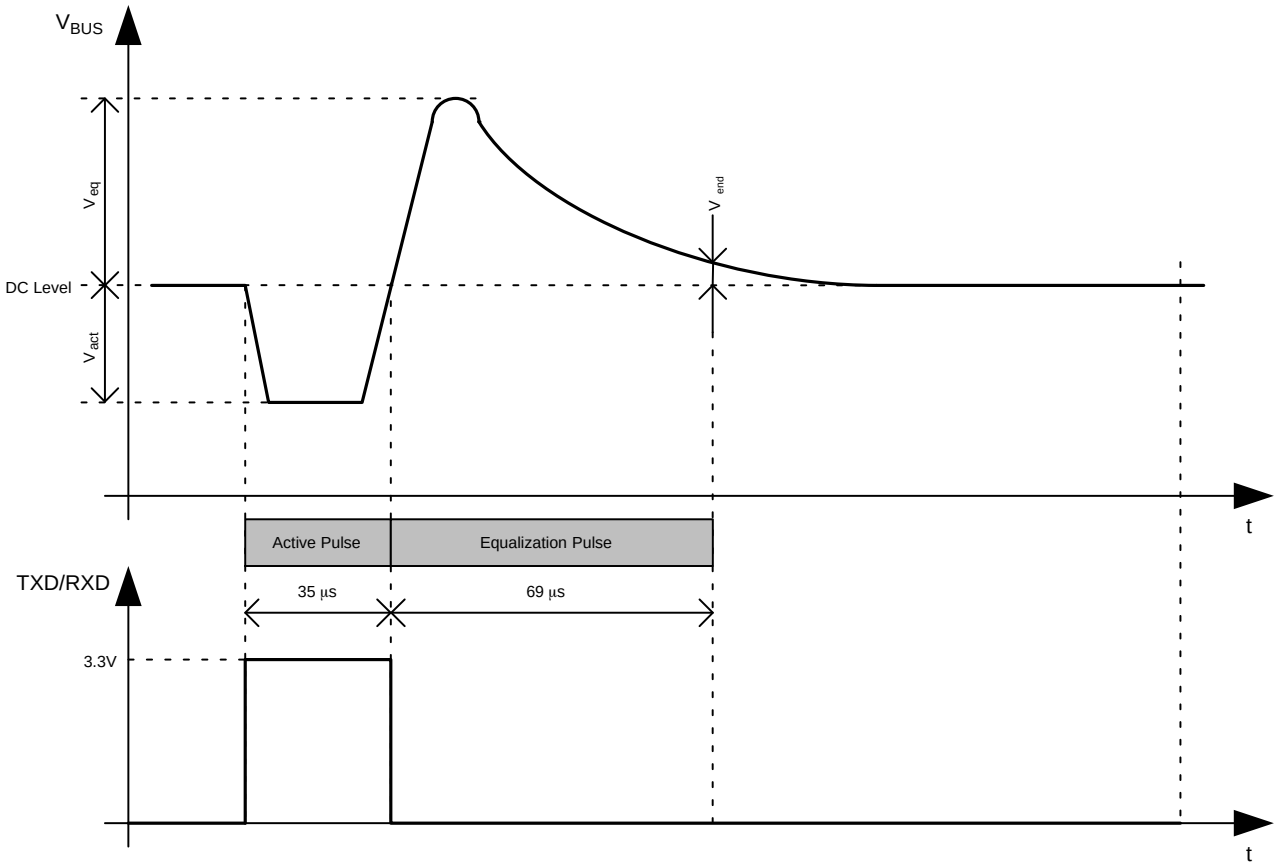


**Figure 16. Bus Communication and the Corresponding Voltage Levels on RxD and TxD**



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## PACKAGE THERMAL CHARACTERISTICS

The NCN5110 is available in a QFN40 package. For cooling optimizations, the QFN40 has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer.

Figure 17 gives an example of good heat transfer. The exposed thermal pad is soldered directly on the top ground layer (left picture of Figure 17). It‘s advised to make the top ground layer as large as possible (see arrows Figure 17). To improve the heat transfer even more, the exposed thermal pad is connected to a bottom ground layer by using thermal vias (see right picture of Figure 17). It‘s advised to make this bottom ground layer as large as possible and with as less as possible interruptions.

For precise thermal cooling calculations the major thermal resistances of the device are given (Table 4). The thermal media to which the power of the devices has to be given are:

− Static environmental air (via the case)
− PCB board copper area (via the exposed pad)

The major thermal resistances of the device are the Rth from the junction to the ambient ($Rth_{ja}$) and the overall Rth from the junction to exposed pad ($Rth_{jp}$). In Table 4 one can find the values for the $Rth_{ja}$ and $Rth_{jp}$, simulated according to JESD-51. The $Rth_{ja}$ for 2S2P is simulated conform JEDEC JESD-51 as follows:

− A 4-layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
− Board thickness is 1.46 mm (FR4 PCB material)
− The 2 signal layers: 70 μm thick copper with an area of 5500 $mm^2$ copper and 20% conductivity
− The 2 power internal planes: 36 μm thick copper with an area of 5500 $mm^2$ copper and 90% conductivity

The $Rth_{ja}$ for 1S0P is simulated conform to JEDEC JESD-51 as follows:

− A 1-layer printed circuit board with only 1 layer
− Board thickness is 1.46 mm (FR4 PCB material)
− The layer has a thickness of 70 μm copper with an area of 5500 $mm^2$ copper and 20% conductivity

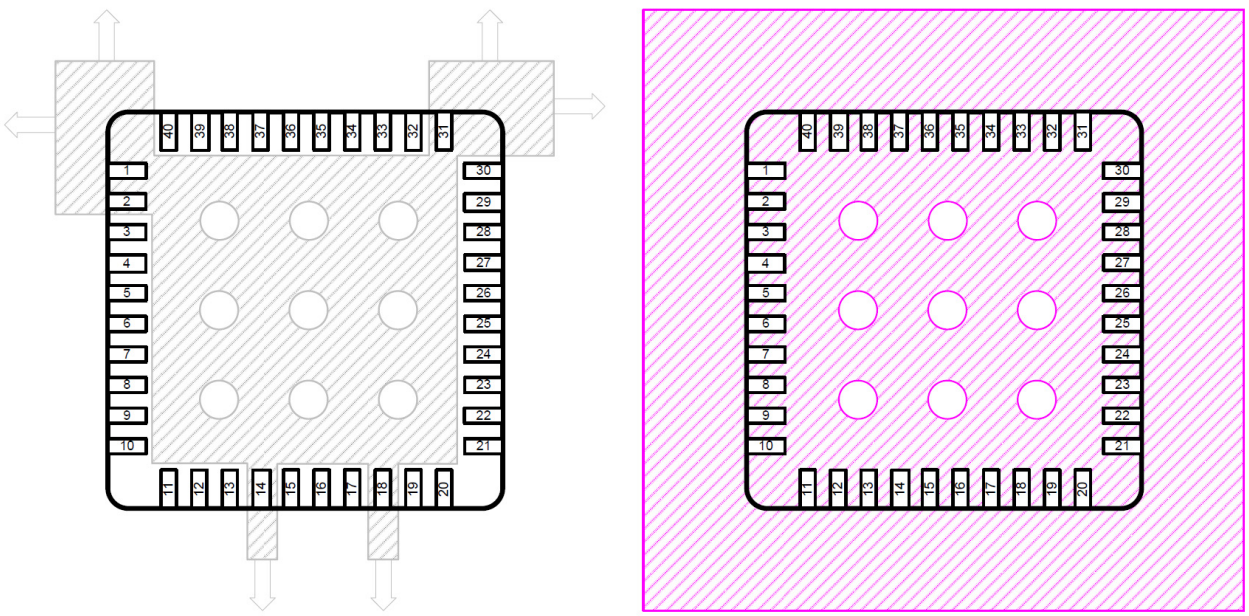


**Figure 17. PCB Ground Plane Layout Condition**
**(left picture displays the top ground layer, right picture displays the bottom ground layer)**

### ORDERING INFORMATION

| Device Number | Temperature Range | Package | Shipping† |
|---|---|---|---|
| NCN5110MNTWG | −40 °C to 105 °C | QFN-40 (Pb-Free) | 3,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 6 | Tweaked bus detection threshold. | 1/26/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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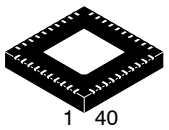
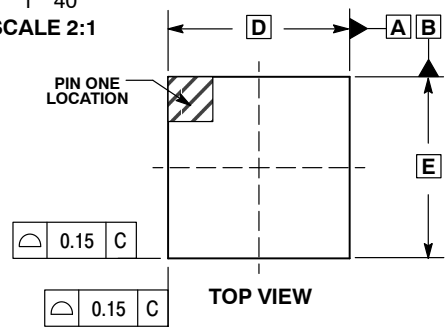
**QFN40 6x6, 0.5P**
CASE 485AU−01
ISSUE O

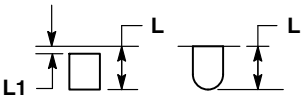
DATE 01 JUL 2008



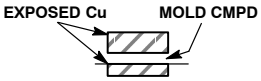

SCALE 2:1



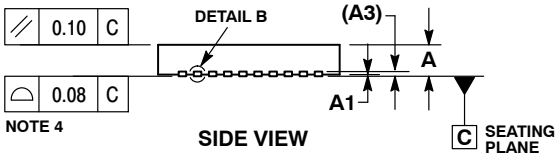

TOP VIEW



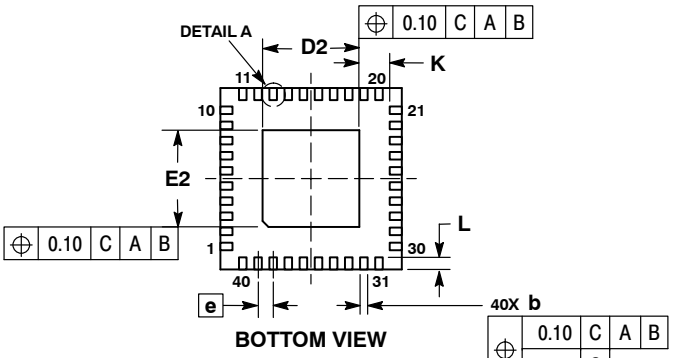

DETAIL A
OPTIONAL CONSTRUCTIONS




DETAIL B
OPTIONAL CONSTRUCTIONS

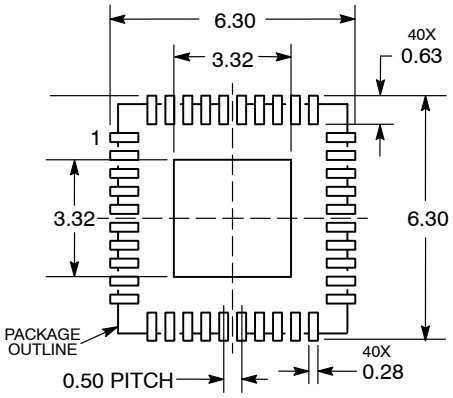



SIDE VIEW




BOTTOM VIEW

SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 6.00 BSC | |
| D2 | 3.10 | 3.30 |
| E | 6.00 BSC | |
| E2 | 3.10 | 3.30 |
| e | 0.50 BSC | |
| K | 0.20 MIN | |
| L | 0.30 | 0.50 |
| L1 | −−− | 0.15 |

GENERIC
MARKING DIAGRAM*

XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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|---|---|---|
| DESCRIPTION: | QFN40, 6x6, 0.5P | PAGE 1 OF 1 |

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