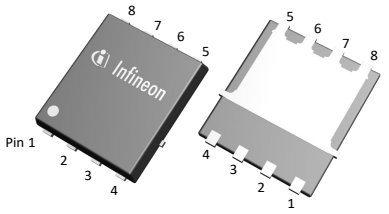
MOSFET

OptiMOS™5 Power-Transistor, 150 V

PG-TDSON-8



Features

- Optimized for high performance SMPS, e.g. Sync. Rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Low Q_{rr}

Product validation

Qualified according to JEDEC Standard

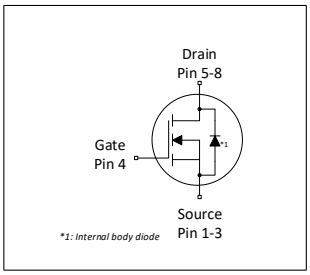


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	11	mΩ
I_D	70	A
Q_{rr}	50	nC

Type / Ordering Code	Package	Marking	Related Links
BSC0403NS	PG-TDSON-8	0403NS	-

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Electrical characteristics 3
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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	70 48	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	280	A	T_A=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	100	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	125	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.6	1	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area[3]	R_{thJA}	-	-	50	°C/W	-

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	V_{DS}=V_{GS}, I_D=91 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	9 10	11 13	mΩ	V_{GS}=10 V, I_D=35 A V_{GS}=8 V, I_D=18 A
Gate resistance	R_G	-	1	1.5	Ω	-
Transconductance	g_{fs}	-	55	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=35 A

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

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Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2100	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance	C_{oss}	-	520	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	13	-	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	4	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	16	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	5	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=3 Ω

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	V_{DD}=75 V, I_D=35 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	6.0	-	nC	V_{DD}=75 V, I_D=35 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	12	-	nC	V_{DD}=75 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	28	-	nC	V_{DD}=75 V, I_D=35 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=75 V, I_D=35 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	78	-	nC	V_{DS}=75 V, V_{GS}=0 V

Table 7 Reverse diode

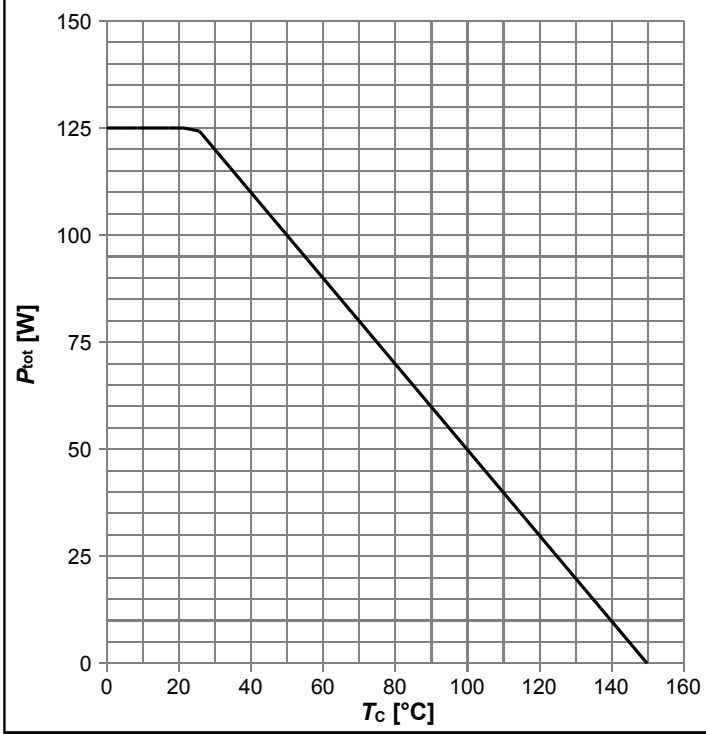
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	70	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	280	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.86	1.2	V	V_{GS}=0 V, I_F=35 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	47	-	ns	V_R=75 V, I_F=35 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	50	-	nC	V_R=75 V, I_F=35 A, di_F/dt=100 A/µs

[1)] See ″Gate charge waveforms″ for parameter definition

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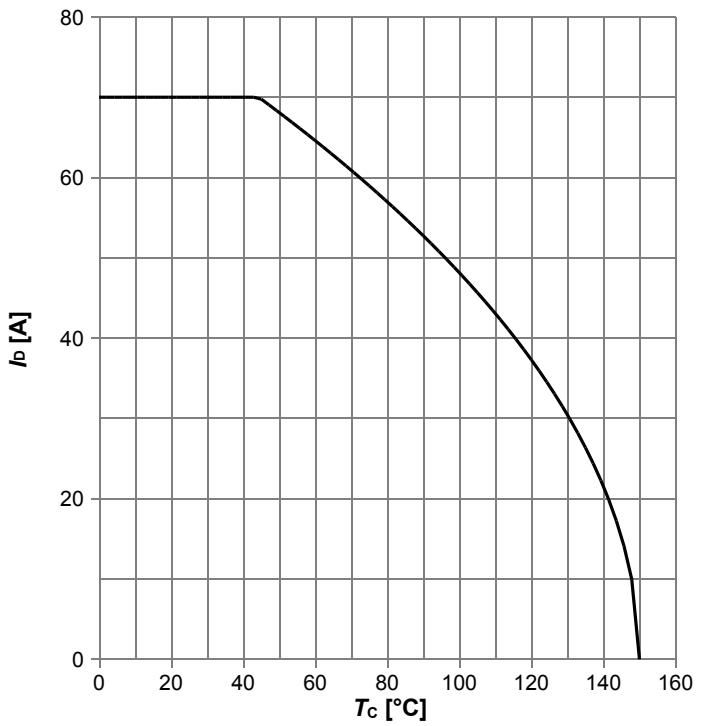
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



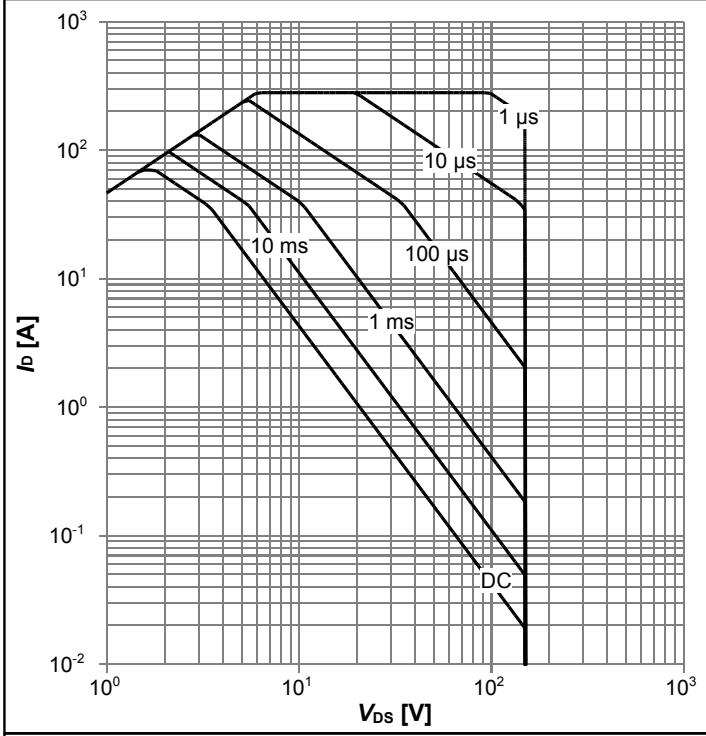
$P_{tot}=f(T_C)$

Diagram 2: Drain current



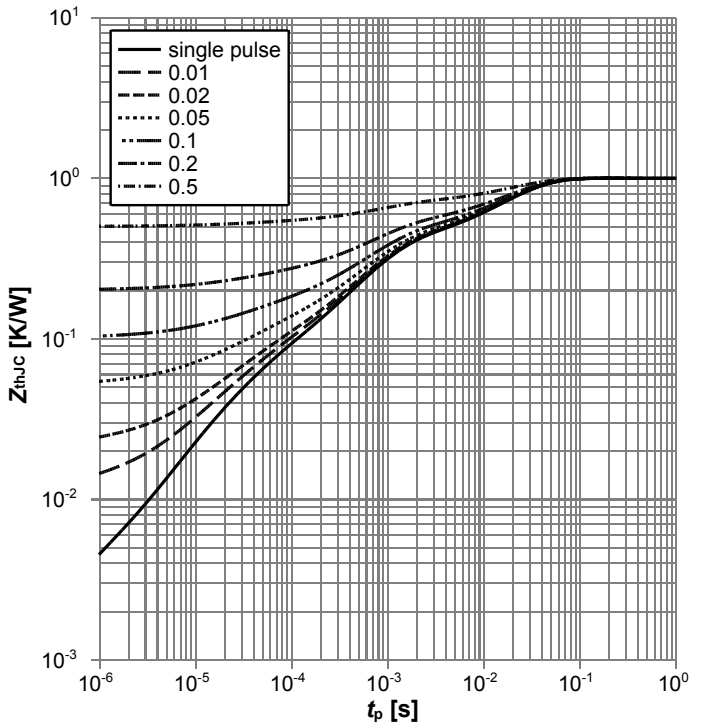
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

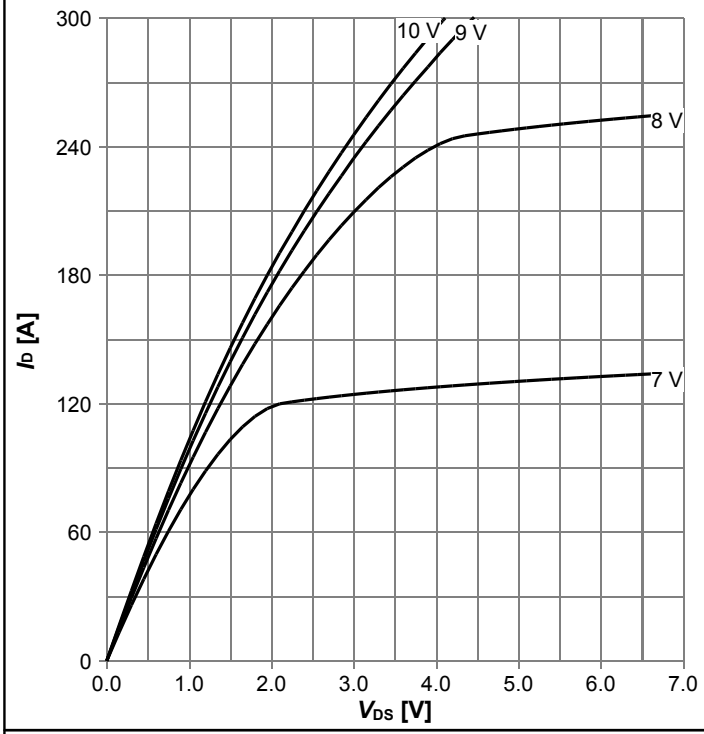
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

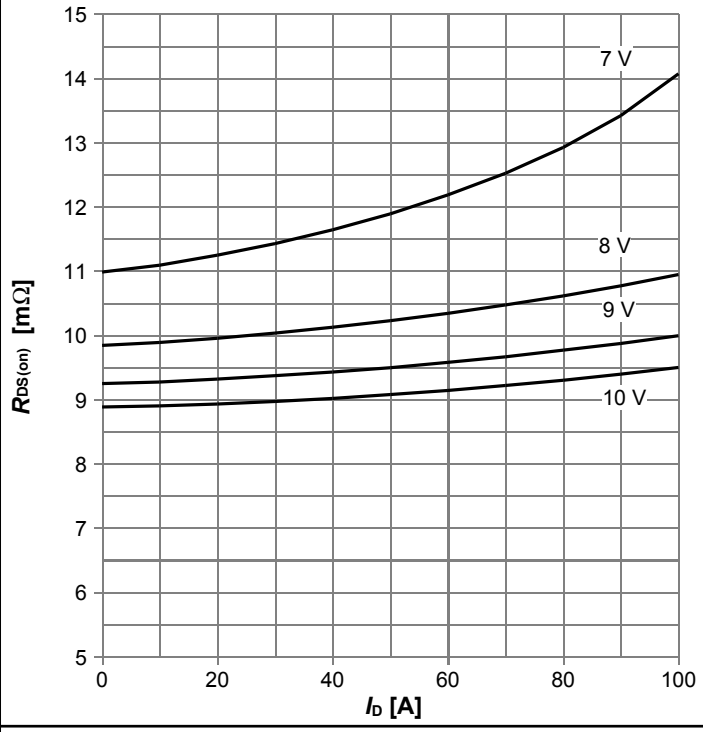
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Diagram 5: Typ. output characteristics



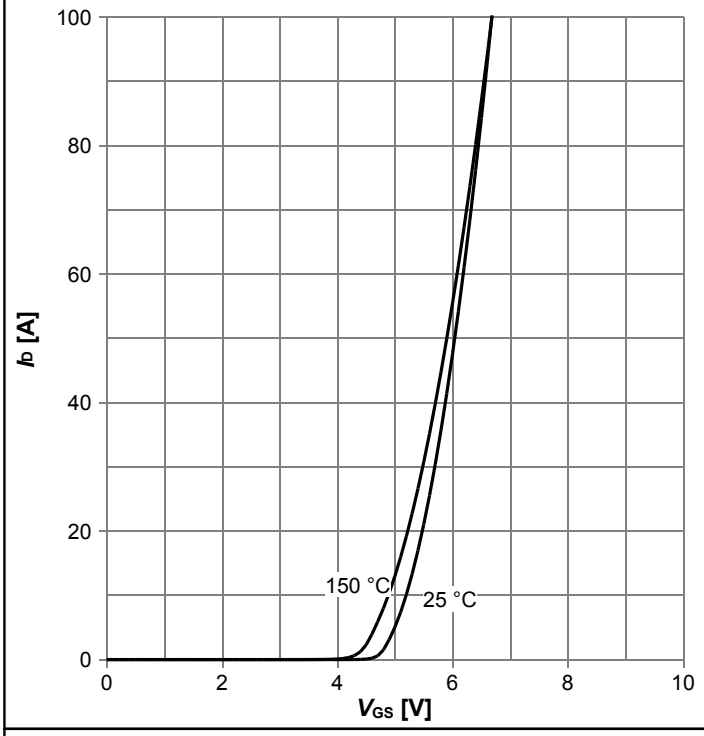
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



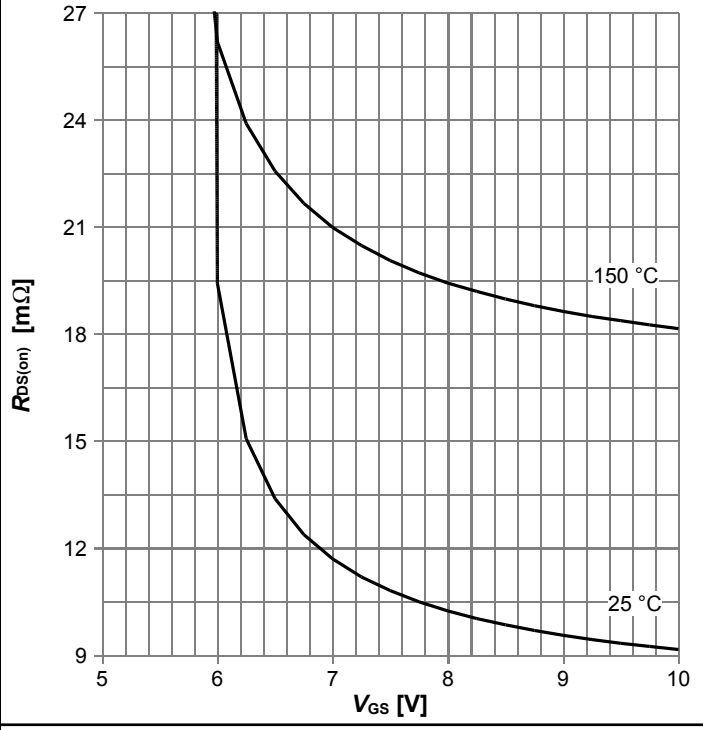
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

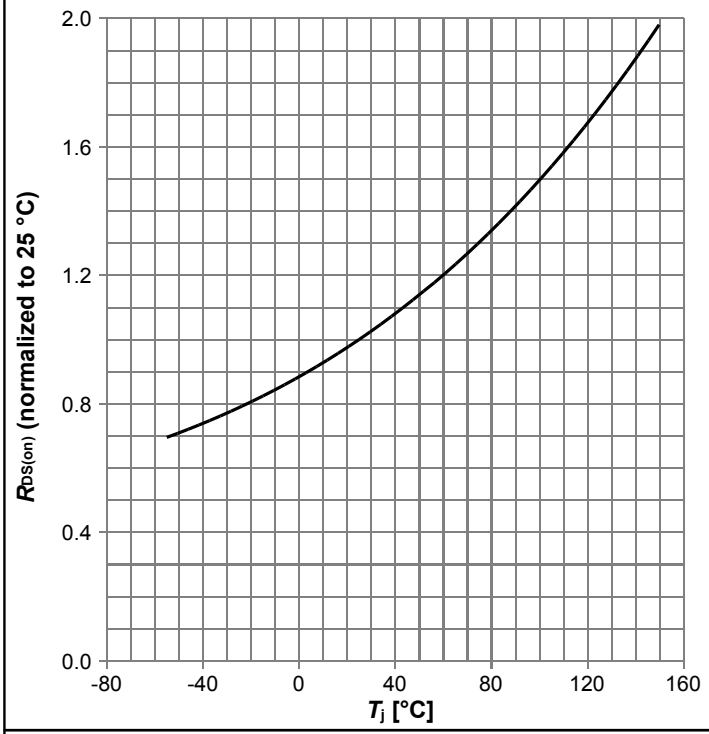
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}=f(V_{GS})$, $I_D=35$ A; parameter: T_j

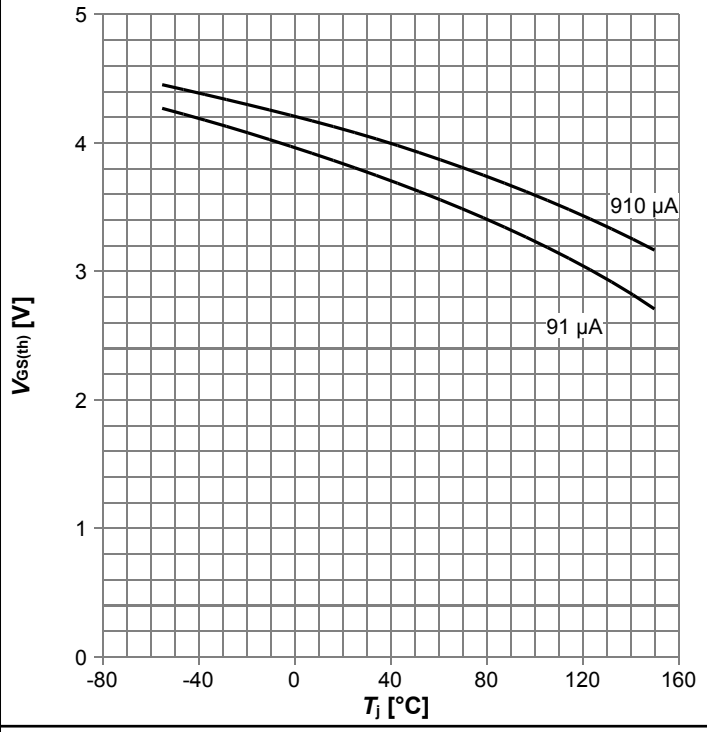
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Diagram 9: Normalized drain-source on resistance



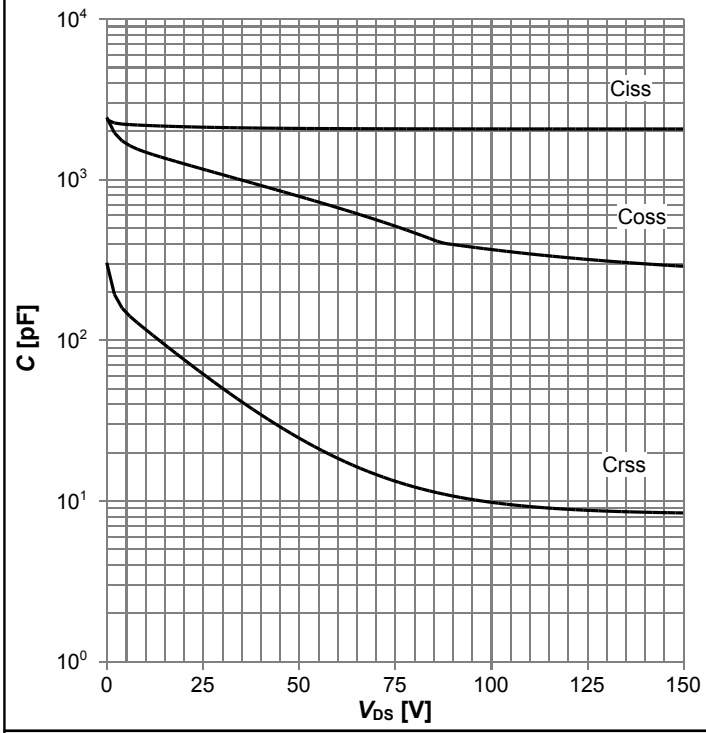
$R_{DS(on)}$=f(T_j), I_D=44 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



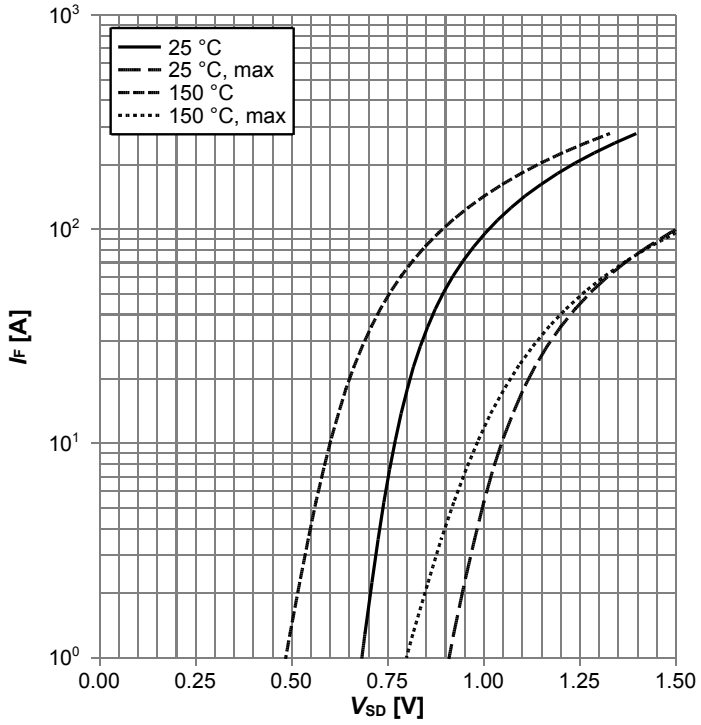
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

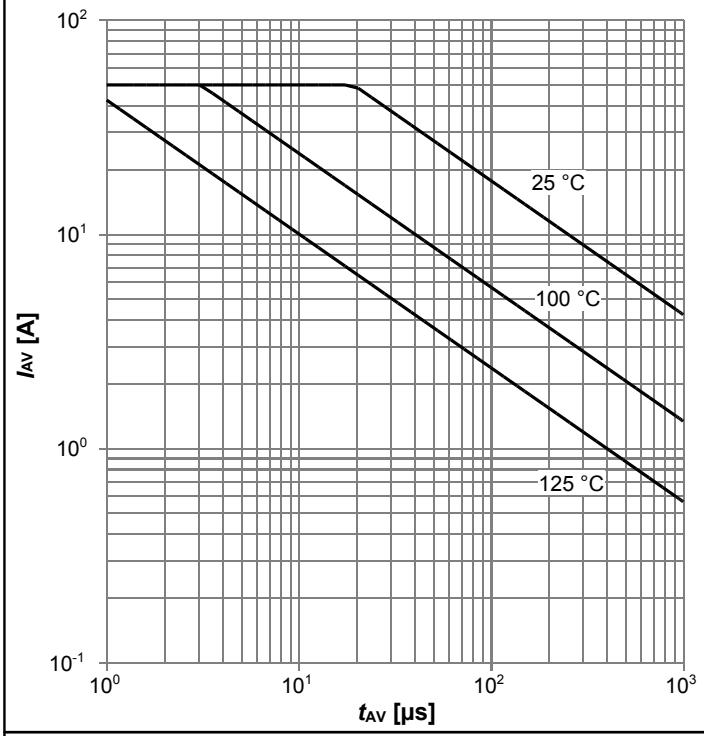
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

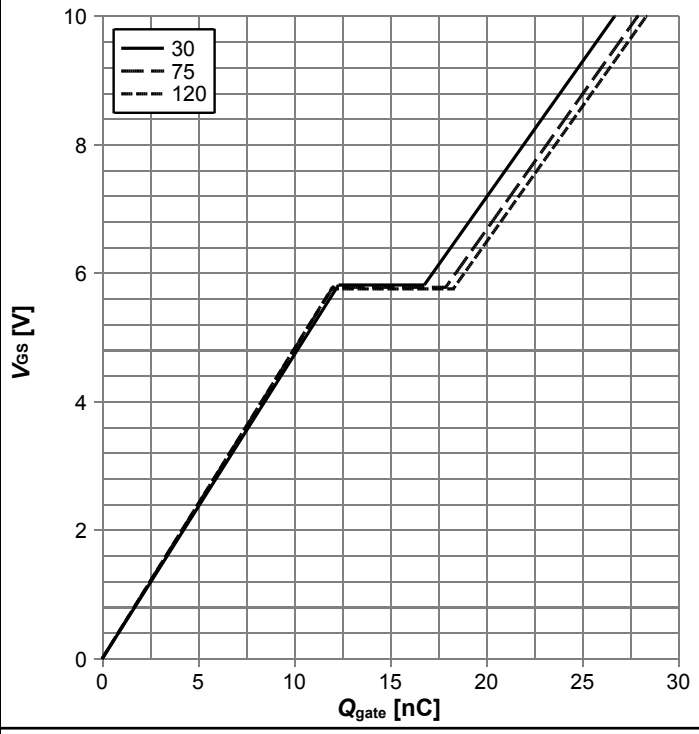
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Diagram 13: Avalanche characteristics



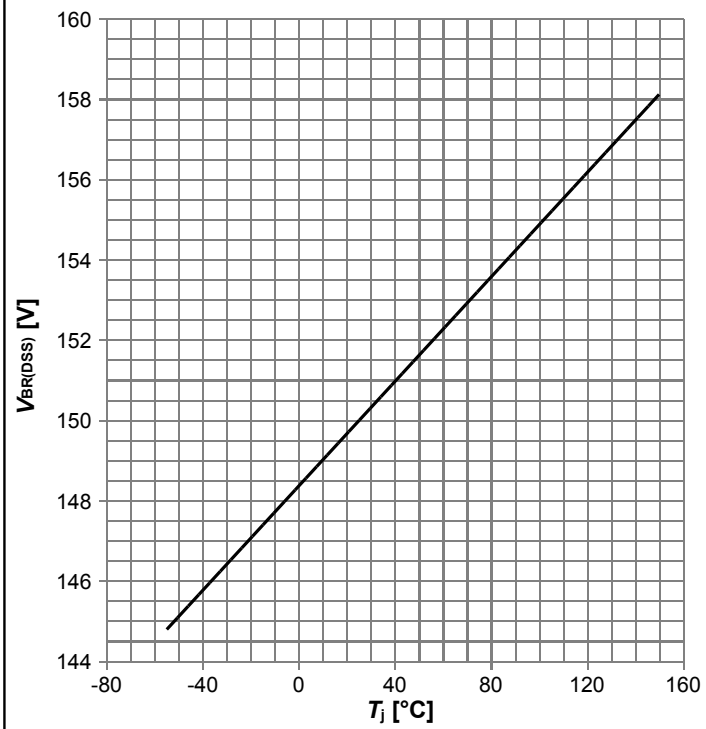
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



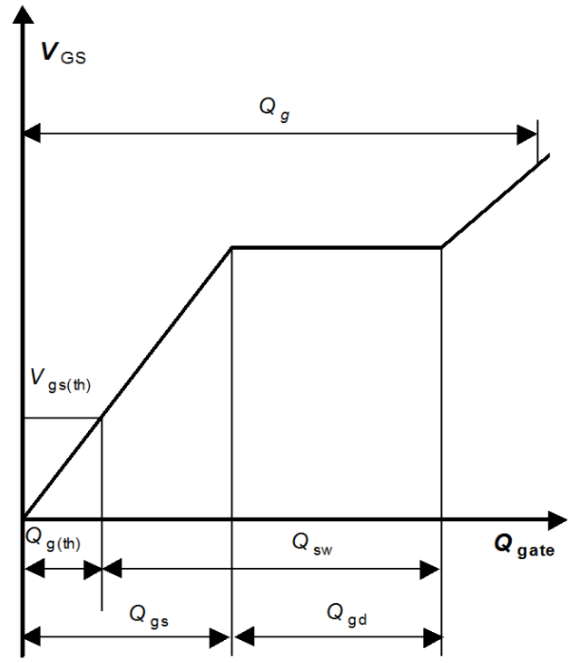
$V_{GS}=f(Q_{gate})$, $I_D=40$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



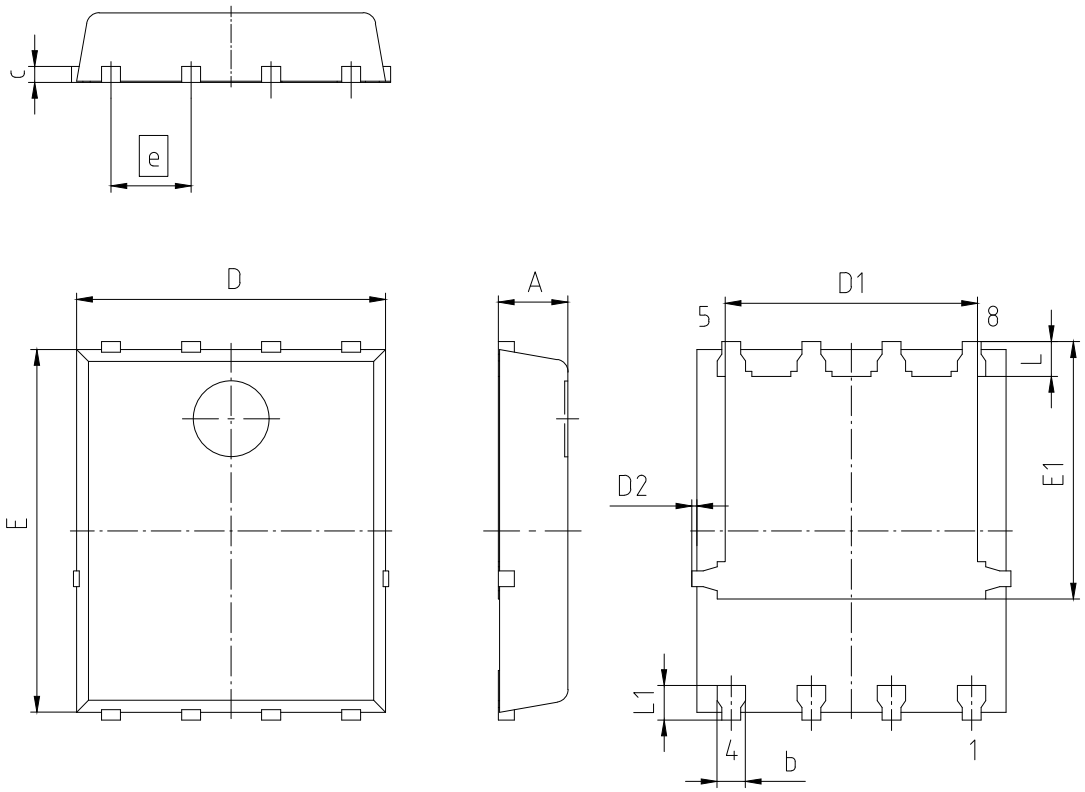
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



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5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U08	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.05	4.25
e	1.27	
L	0.45	0.65
L1	0.45	0.65

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

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Revision History

BSC0403NS

Revision: 2022-11-08, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2019-12-16	Release of final version
2.1	2022-11-08	Update package outline drawing and footnotes

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