

FDR8508P

Dual P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

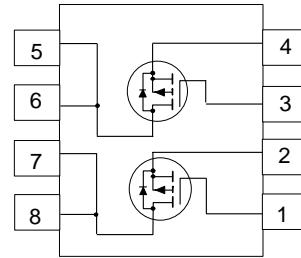
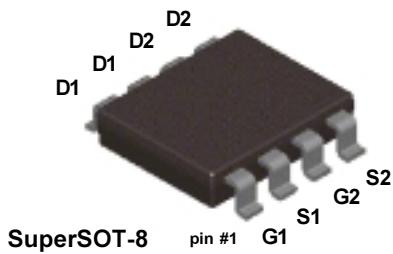
These P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Load switch
- DC/DC converter
- Motor driving

Features

- -3.0 A, -30 V. $R_{DS(ON)} = 0.052\Omega$ @ $V_{GS} = -10V$
- $R_{DS(ON)} = 0.086\Omega$ @ $V_{GS} = -4.5V$.
- Low gate charge. (8nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability.
- Small footprint (38% smaller than a standard SO-8); low profile package (1 mm thick); power handling capability similar to SO-8.



Absolute Maximum Ratings

$T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FDR8508P	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	-3	A
	- Pulsed	-20	
P_D	Power Dissipation	0.8	W
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	156	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.8508	FDR8508P	13"	12mm	3000 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	-30			V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		24		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = -24 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$			-1	μA
I_{GSSF}	Gate-Body Leakage Current	$V_{\text{GS}} = 20 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current	$V_{\text{GS}} = -20 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = -250 \mu\text{A}$	-1	-1.8	-3	V
$\Delta V_{\text{GS(th)}}/\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		-4		$\text{mV}/^\circ\text{C}$
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = -10 \text{ V}$, $I_D = -3 \text{ A}$ $V_{\text{GS}} = -10 \text{ V}$, $I_D = -3 \text{ A}$, $T_J = 125^\circ\text{C}$ $V_{\text{GS}} = -4.5 \text{ V}$, $I_D = -2.3 \text{ A}$		0.040 0.057 0.058	0.052 0.078 0.086	Ω
$I_{\text{D(on)}}$	On-State Drain Current	$V_{\text{GS}} = -10 \text{ V}$, $V_{\text{DS}} = -5 \text{ V}$	-20			A
g_{FS}	Forward Transconductance	$V_{\text{DS}} = -5 \text{ V}$, $I_D = -3 \text{ A}$		9		mS

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{\text{DS}} = -15 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$		750		pF
C_{oss}	Output Capacitance			220		pF
C_{rss}	Reverse Transfer Capacitance			100		pF

Switching Characteristics (Note 2)

$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = -15 \text{ V}$, $I_D = -1 \text{ A}$, $V_{\text{GS}} = -10 \text{ V}$, $R_{\text{GEN}} = 6 \Omega$		12	22	ns
t_r	Turn-On Rise Time			14	25	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time			24	38	ns
t_f	Turn-Off Fall Time			16	27	ns
Q_g	Total Gate Charge	$V_{\text{DS}} = -15 \text{ V}$, $I_D = -3 \text{ A}$, $V_{\text{GS}} = -5 \text{ V}$,		8	12	nC
Q_{gs}	Gate-Source Charge			1.8		nC
Q_{gd}	Gate-Drain Charge			3		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_s	Maximum Continuous Drain-Source Diode Forward Current			-0.67	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_s = -0.67 \text{ A}$	(Note 2)	-0.75	-1.2	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 board in still air.



156°C/W when mounted on a 0.0025 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Characteristics

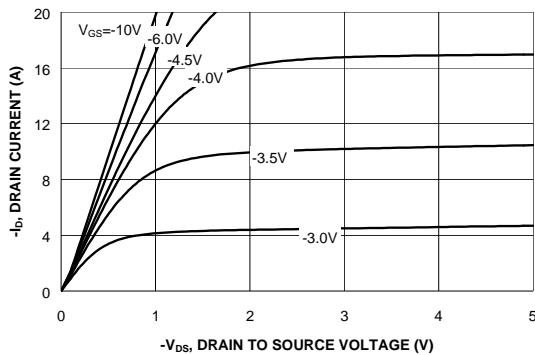


Figure 1: On-Region Characteristics

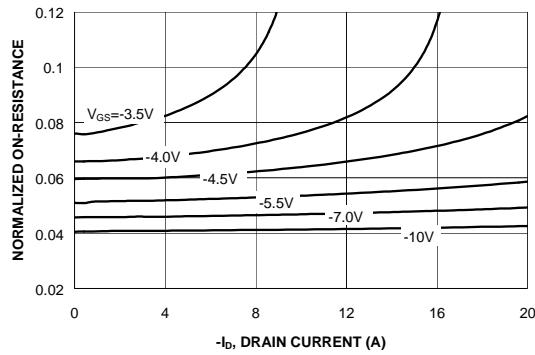


Figure 2: On-Resistance Variation vs Drain Current and Gate Voltage

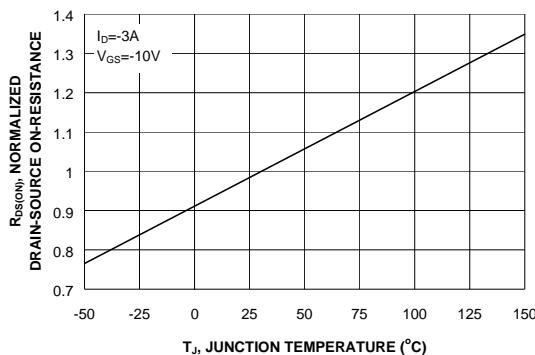


Figure 3: On-Resistance Variation vs Temperature

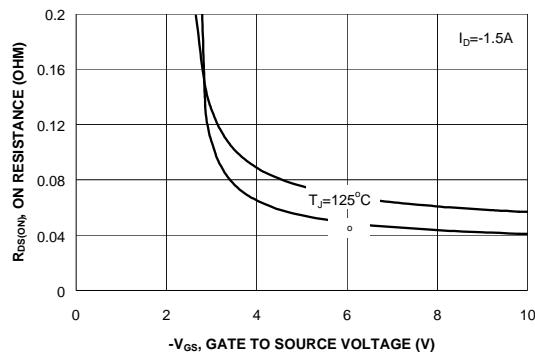


Figure 4: On-Resistance Variation vs Gate-To-Source Voltage

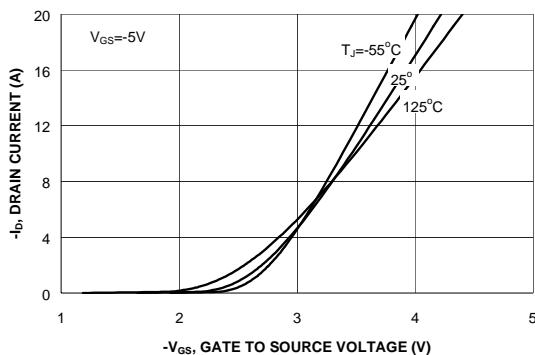


Figure 5: Transfer Characteristics

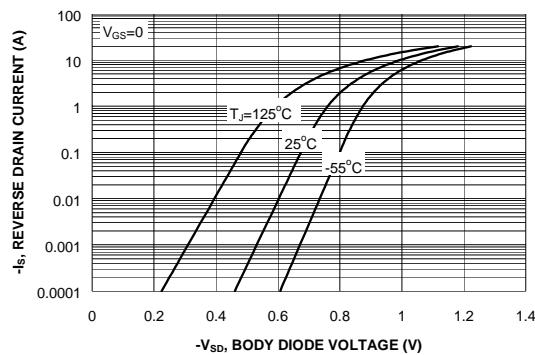


Figure 6: Body Diode Forward Voltage Variation vs Source Current and Temperature

Typical Characteristics (continued)

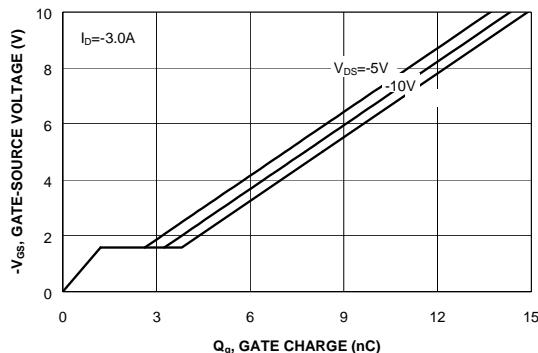


Figure 7: Gate-Charge Characteristics

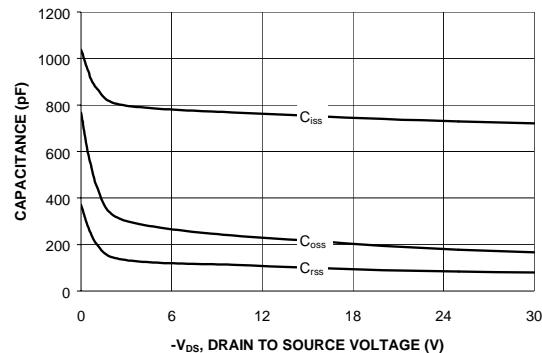


Figure 8: Capacitance Characteristics

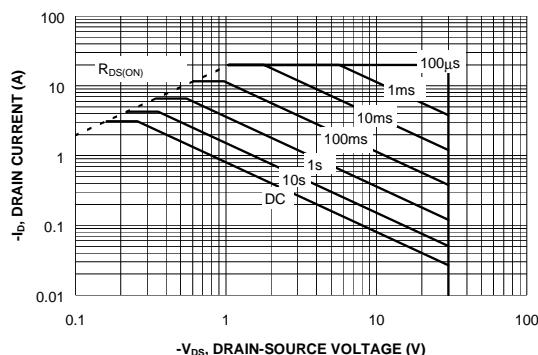


Figure 9: Maximum Safe Operating Area

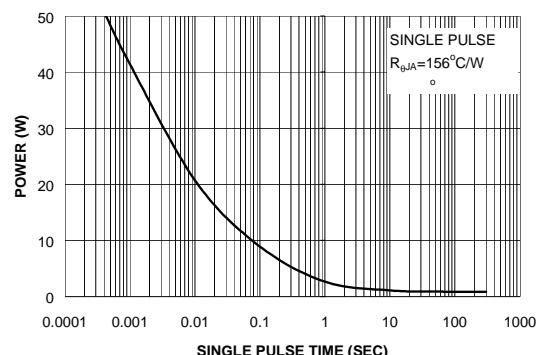


Figure 10: Single Pulse Maximum Power Dissipation

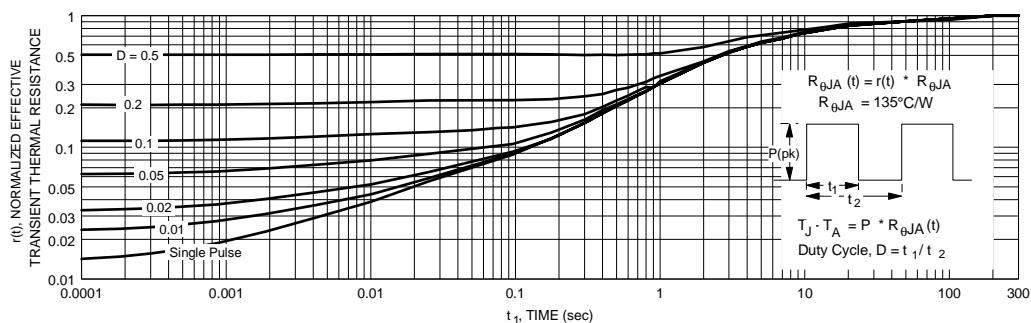


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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