



LP8867C-Q1, LP8869C-Q1 Low EMI Automotive LED Driver with 4-, 3- Channels

1 Features

- AEC-Q100 Qualified for automotive applications:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- 3-, 4-Channel 120-mA LED driver for automotive LCD display
 - High dimming ratio of 10 000:1 at 100 Hz
 - Current matching 1% (typical)
 - LED String current up to 120 mA per channel
 - Outputs can be combined externally for higher current per string
- Integrated boost and SEPIC converter for LED string power
 - Input voltage operating range 4.5 V to 40 V
 - Output voltage up to 45 V
 - Integrated 3.3-A Switch FET
 - Switching frequency 300 kHz to 2.2 MHz
 - Switching synchronization input
 - Spread spectrum for lower EMI
- Protection and fault detection
 - Fault output
 - Input voltage OVP, UVLO
 - Boost OVP
 - SW OVP
 - LED Open and short fault detection
 - Thermal shutdown

2 Applications

- Backlight for:
 - Automotive infotainment
 - Automotive instrument clusters
 - Smart mirrors
 - Heads-up displays (HUD)

3 Description

The LP8867C-Q1, LP8869C-Q1 is an automotive highly-integrated, low-EMI, easy-to-use LED driver with DC-DC converter. The DC-DC converter supports both boost and SEPIC mode operation. The device has four or three high-precision current sinks that can be combined for higher current capability.

The DC-DC converter has adaptive output voltage control based on the LED forward voltages. This feature minimizes the power consumption by adjusting the voltage to the lowest sufficient level in all conditions. For EMI reduction DC-DC supports spread spectrum for switching frequency and an external synchronization with dedicated pin. A wide-range adjustable frequency allows the LP886xC-Q1 to avoid disturbance for sensitive frequency band.

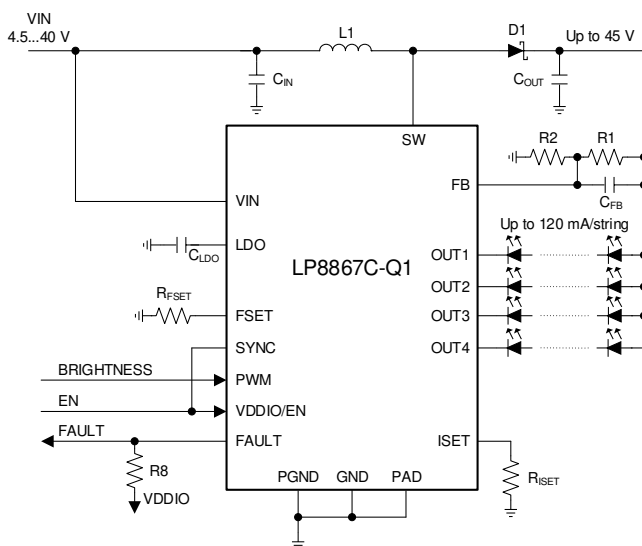
The input voltage range for the LP886xC-Q1 is from 4.5 V to 40 V to support automotive stop, start and load dump condition. The LP886xC-Q1 integrates extensive fault detection features.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8867C-Q1	HTSSOP (20)	6.50 mm × 4.40 mm
LP8869C-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



System Efficiency

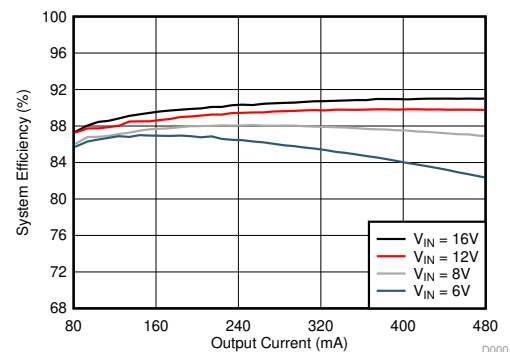


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4 Revision History

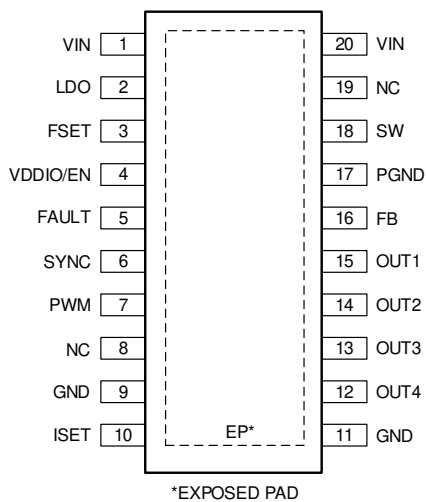
DATE	REVISION	NOTES
August 2019	*	Initial Release

5 Device Comparison Table

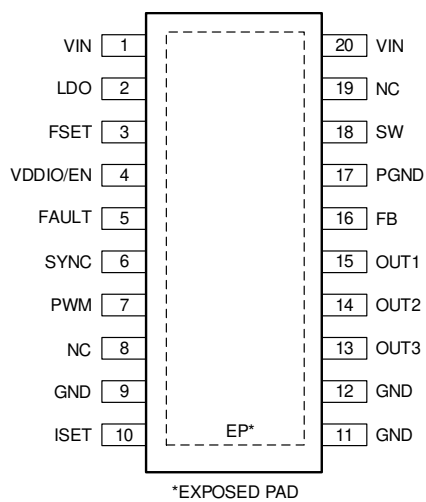
	LP8869-Q1	LP8869C-Q1	LP8867-Q1	LP8867C-Q1
Number of LED channels	3	3	4	4
LED current / channel	120 mA	120 mA	120 mA	120 mA
Power Line FET Control and Automatic Current De-rating Support	Yes	No	Yes	No

6 Pin Configuration and Functions

LP8867C-Q1 PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



LP8869C-Q1 PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	VIN	A	Input power pin and pin for input voltage detection for OVP protection
2	LDO	A	Output of internal LDO; connect a 1- μ F decoupling capacitor between this pin and noise-free GND. Put the capacitor as close to the chip as possible.
3	FSET	A	DC-DC (boost or SEPIC) switching frequency setting resistor; for normal operation, resistor value from 24 k Ω to 219 k Ω must be connected between this pin and ground.
4	VDDIO/EN	I	Enable input for the device as well as supply input (VDDIO) for digital pins.
5	FAULT	OD	Fault signal output. If unused, the pin may be left floating.
6	SYNC	I	Input for synchronizing DC-DC converter. If synchronization is not used, connect this pin to GND to disable spread spectrum or to VDDIO/EN to enable spread spectrum.
7	PWM	I	PWM dimming input.
8	NC	—	No connect
9	GND	G	Ground
10	ISET	A	LED current setting resistor; for normal operation, resistor value from 20 k Ω to 129 k Ω must be connected between this pin and ground.
11	GND	G	Ground.
12	OUT4/GND	A	Current sink output for LP8867C-Q1 This pin must be connected to GND if not used. GND pin for LP8869C-Q1
13	OUT3	A	Current sink output. This pin must be connected to GND if not used.
14	OUT2	A	Current sink output. This pin must be connected to GND if not used.
15	OUT1	A	Current sink output. This pin must be connected to GND if not used.
16	FB	A	DC-DC (boost or SEPIC) feedback input; for normal operation this pin must be connected to the middle of a resistor divider between V_{OUT} and ground using feedback resistor values greater than 5k Ω .
17	PGND	G	DC-DC (boost or SEPIC) power ground.
18	SW	A	DC-DC (boost or SEPIC) switch pin.
19	NC	—	No connect
20	VIN	A	Input power pin and pin for input voltage detection for OVP protection

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Voltage on pins	VIN, SD, SW, FB	–0.3	50	V
	OUT1, OUT2, OUT3, OUT4	–0.3	45	
	LDO, SYNC, FSET, ISET, PWM, VDDIO/EN, FAULT	–0.3	5.5	
Continuous power dissipation ⁽³⁾		Internally Limited		
Ambient temperature, T _A ⁽⁴⁾		–40	125	°C
Junction temperature, T _J ⁽⁴⁾		–40	150	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).
- (4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 150°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} × P_{D-MAX}).

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, all pins ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 10, 11 and 20)	
			All pins	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
Voltage on pins	VIN	4.5	12	45	V
	SW	0		45	
	OUT1, OUT2, OUT3, OUT4	0		40	
	FB, FSET, LDO, ISET, VDDIO/EN, FAULT	0		5.25	
	SYNC, PWM	0		VDDIO/EN	

- (1) All voltages are with respect to the potential at the GND pins.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP886xC-Q1	UNIT
		PWP (HTSSOP)	
		20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	44.2	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	26.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	22.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	22.2	°C/W
R _{θJBot}	Junction-to-case (bottom) thermal resistance	2.5	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.5 Electrical Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _Q	Standby supply current	Device disabled, V _{VDDIO/EN} = 0 V, V _{IN} = 12 V		4.5	20	μA
	Active supply current	V _{IN} = 12 V, V _{OUT} = 26 V, output current 80 mA/channel, converter f _{SW} = 300 kHz		5	12	mA

7.6 Internal LDO Electrical Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{LDO}	Output voltage	V _{IN} = 12 V	4.15	4.3	4.55	V
V _{DR}	Dropout voltage		120	300	430	mV
I _{SHORT}	Short circuit current			50		mA
I _{EXT}	Current for external load				5	mA

7.7 Protection Electrical Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OVP}	VIN OVP threshold voltage		41	42	44	V
V _{UVLO}	VIN UVLO Falling threshold		3.7	3.85	4	V
V _{UVLO_HYST}	VIN UVLO Rising threshold - VIN UVLO Falling threshold			150		mV
V _{FB_OVP}	FB threshold for BST_OVP fault			2.3		V
T _{TSD}	Thermal shutdown Rising threshold		150	165	175	°C
T _{TSD_HYS}	Thermal shutdown Rising threshold - Thermal shutdown Falling threshold			20		°C

7.8 Current Sinks Electrical Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT4, $V_{OUTx} = 45\text{ V}$, $EN = L$		0.1	5	μA
I_{MAX}	Maximum current	OUT1, OUT2, OUT3, OUT4, $R_{ISET} = 20\text{ k}\Omega$		120		mA
I_{OUT}	Output current accuracy	$I_{OUT} = 100\text{ mA}$	-5%		5%	
I_{MATCH}	Output current matching ⁽¹⁾	$I_{OUT} = 100\text{ mA}$, PWM duty = 100%		1%	5%	
V_{LOW_COMP}	Low comparator threshold			0.9		V
V_{MID_COMP}	Mid comparator threshold			1.9		V
V_{HIGH_COMP}	High comparator threshold		5.6	6	7	V

- (1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUTx), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.

7.9 PWM Brightness Control Electrical Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM input frequency		100		20 000	Hz
$t_{ON/OFF}$	Minimum on/off time ⁽¹⁾			0.5		μs

- (1) This specification is not ensured by ATE.

7.10 Boost and SEPIC Converter Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		40	V
V_{OUT}	Output voltage		6		45	
f_{SW_MIN}	Minimum switching frequency	Defined by R_{FSET} resistor		300		kHz
f_{SW_MAX}	Maximum switching frequency	Defined by R_{FSET} resistor		2 200		kHz
t_{OFF}	Minimum switch OFF time ⁽¹⁾	$f_{SW} \geq 1.15\text{ MHz}$			55	ns
I_{SW_MAX}	SW current limit first triggered		3.3	3.7	4.1	A
t_{SW_MAX}	SW current limit first triggered period			1.6		s
I_{SW_LIM}	SW current limit		3	3.35	3.7	A
$R_{DS(on)}$	FET $R_{DS(on)}$			240	400	m Ω
f_{SYNC}	External SYNC frequency		300		2 200	kHz
t_{SYNC_ON}	External SYNC on time ⁽¹⁾		150			ns
t_{SYNC_OFF}	External SYNC off time ⁽¹⁾		150			ns

- (1) This specification is not ensured by ATE.

7.11 Logic Interface Characteristics

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.65			
I_{EN}	Input DC current		-1	5	30	μA
	Input transient current during VDDIO/EN powering up				1.2	mA
LOGIC INPUT SYNC, PWM						

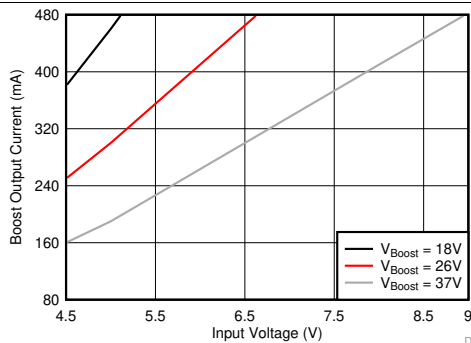
Logic Interface Characteristics (continued)

Limits apply over the full operation temperature range $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, unless otherwise specified, $V_{IN} = 12\text{V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				$0.2 \times V_{DDIO/E}$	V
V_{IH}	Input high level				$0.8 \times V_{DDIO/E}$	
I_I	Input current		-1		1	μA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	Pullup current 3 mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	$V = 5.5\text{ V}$			1	μA

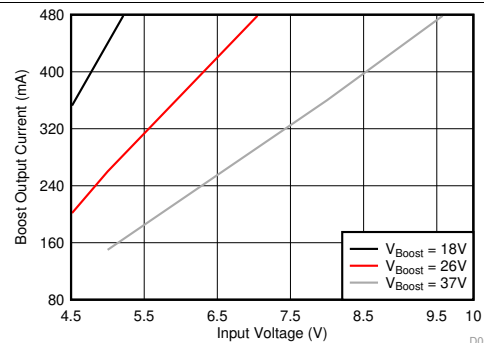
7.12 Typical Characteristics

Unless otherwise specified: D = NRVB460MFS, $T_A = 25^\circ\text{C}$



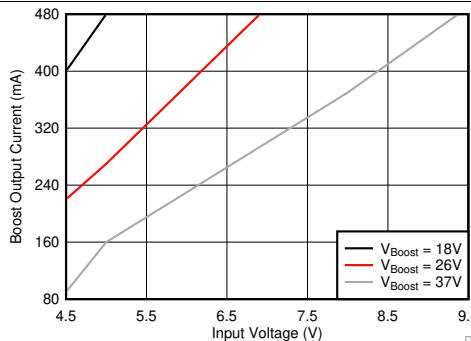
$f_{\text{SW}} = 400 \text{ kHz}$ $L = 33 \mu\text{H}$ DC Load (PWM = 100%)
 C_{IN} and $C_{\text{OUT}} = 33 \mu\text{F} + 2 \times 10 \mu\text{F}$ (ceramic)

Figure 1. Maximum Boost Current



$f_{\text{SW}} = 1.1 \text{ MHz}$ $L = 15 \mu\text{H}$ DC Load (PWM = 100%)
 C_{IN} and $C_{\text{OUT}} = 33 \mu\text{F} + 10 \mu\text{F}$ (ceramic)

Figure 2. Maximum Boost Current



$f_{\text{SW}} = 2.2 \text{ MHz}$ $L = 10 \mu\text{H}$ DC Load (PWM = 100%)
 C_{IN} and $C_{\text{OUT}} = 3 \times 10 \mu\text{F}$ (ceramic)

Figure 3. Maximum Boost Current

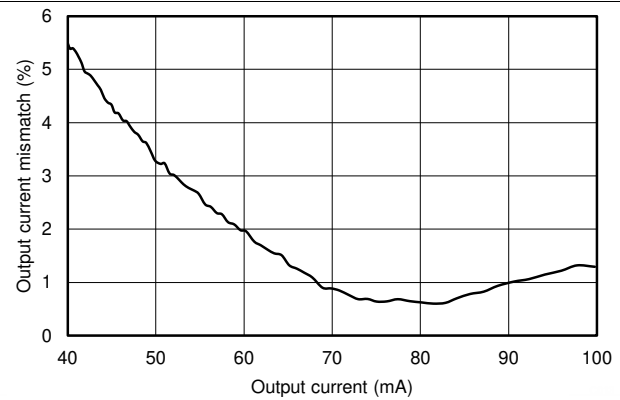
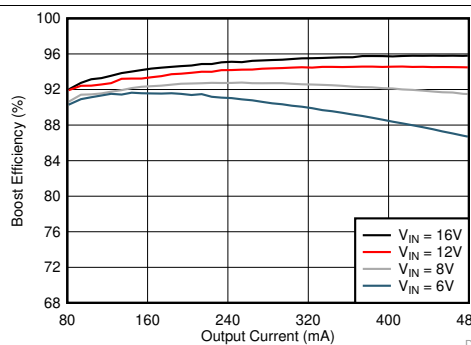
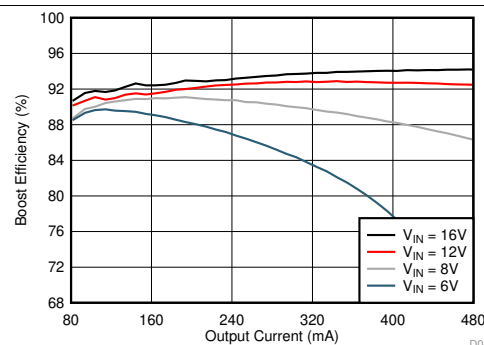


Figure 4. LED Current Sink Matching



$f_{\text{SW}} = 400 \text{ kHz}$ $L = 22 \mu\text{H}$ DC Load (PWM = 100%)
 C_{IN} and $C_{\text{OUT}} = 33 \mu\text{F} + 2 \times 10 \mu\text{F}$ $V_{\text{BOOST}} = 18 \text{ V}$
(ceramic)

Figure 5. Boost Efficiency

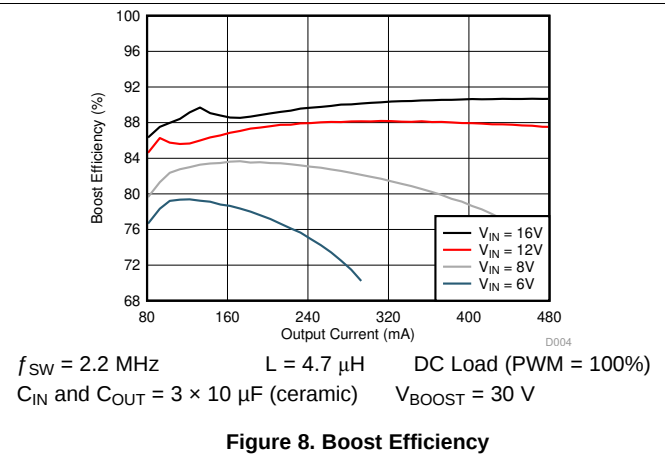
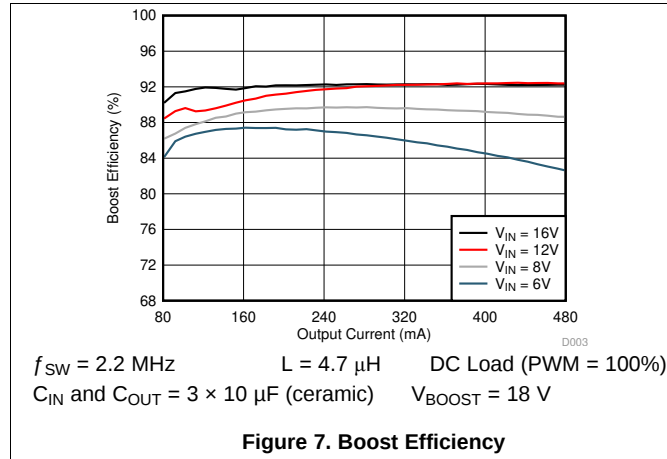


$f_{\text{SW}} = 400 \text{ kHz}$ $L = 22 \mu\text{H}$ DC Load (PWM = 100%)
 C_{IN} and $C_{\text{OUT}} = 33 \mu\text{F} + 2 \times 10 \mu\text{F}$ $V_{\text{BOOST}} = 30 \text{ V}$
(ceramic)

Figure 6. Boost Efficiency

Typical Characteristics (continued)

Unless otherwise specified: D = NRVB460MFS, $T_A = 25^\circ\text{C}$



8 Detailed Description

8.1 Overview

The LP8867C-Q1, LP8869C-Q1 is a highly integrated LED driver for automotive infotainment , cluster and HUD medium-size LCD backlight applications. It includes a DC-DC with an integrated FET, supporting both boost and SEPIC modes, an internal LDO enabling direct connection to battery without need for a pre-regulated supply and 3 or 4 LED current sinks. The VDDIO/EN pin provides the supply voltage for digital IOs (PWM and SYNC inputs) and at the same time enables the device.

The switching frequency on the DC-DC converter is set by a resistor connected to the FSET pin. The maximum voltage of the DC-DC is set by a resistive divider connected to the FB pin. For the best efficiency, the output voltage is adapted automatically to the minimum necessary level needed to drive the LED strings. This is done by monitoring LEDs' cathode voltage in real time. For EMI reduction, two optional features are available:

- Spread spectrum, which reduces EMI noise around the switching frequency and its harmonic frequencies
- DC-DC can be synchronized to an external frequency connected to SYNC pin

The 3 or 4 constant current outputs OUT1, OUT2, OUT3, and OUT4 provide LED current up to 120 mA. Value for the current per OUT pin is set with a resistor connected to ISET pin. Current sinks that are not used must be connected to ground. Grounded current sink is disabled and excluded from boost adaptive voltage detection loop.

Brightness is controlled with the PWM input. Frequency range for the input PWM is from 100 Hz to 20 kHz. LED output PWM behavior follows the input PWM so the output frequency is equal to the input frequency.

LP886xC-Q1 has extensive fault detection features:

- LED open and short detection
- V_{IN} input overvoltage protection
- V_{IN} input undervoltage protection
- V_{Boost} output overvoltage protection
- SW overvoltage protection
- Thermal shutdown in case of chip overheated

Fault condition is indicated through the FAULT output pin.

8.3 Feature Description

8.3.1 Integrated DC-DC Converter

The LP886xC-Q1 DC-DC converter generates supply voltage for the LEDs and can operate in boost mode or in SEPIC mode. The output voltage, switching frequency are all configured by external resistors.

8.3.1.1 DC-DC Converter Parameter Configuration

The LP886xC-Q1 converter is a current-peak mode DC-DC converter, where the switch FET's current and the output voltage feedback are measured and controlled. The block diagram shown in Figure 9

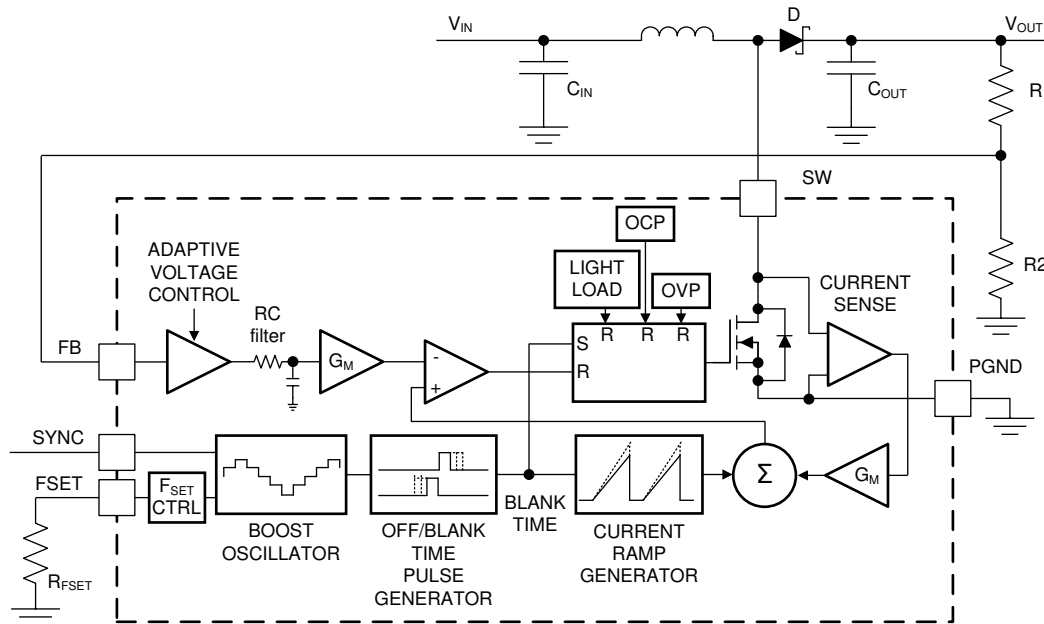


Figure 9. Boost Block Diagram

8.3.1.1.1 Switching Frequency

Switching frequency is adjustable between 300 kHz and 2.2 MHz with R_{FSET} resistor as Equation 1:

$$f_{SW} = 67600 / (R_{FSET} + 6.4)$$

where

- f_{SW} is switching frequency, kHz
- R_{FSET} is frequency setting resistor, kΩ

(1)

For example, if R_{FSET} is set to 163 kΩ, f_{SW} will be 400 kHz.

In most cases, lower switching frequency has higher system efficiency and lower internal temperature increase.

8.3.1.1.2 Spread Spectrum and External SYNC

LP886xC-Q1 has an optional spread spectrum feature ($\pm 3\%$ from central frequency, 1-kHz modulation frequency) which reduces EMI noise at the switching frequency and its harmonic frequencies. If SYNC pin level is low, spread spectrum function is disabled. If SYNC pin level is high, spread spectrum function is enabled.

LP886xC-Q1 DC-DC converter can be driven by an external SYNC signal between 300 kHz and 2.2 MHz. When external synchronization is used, spread spectrum is not available. If the external synchronization input disappears, DC-DC continues operation at the frequency defined by R_{FSET} resistor and spread spectrum function will be enabled/disabled depending on the final SYNC pin level.

External SYNC frequency must be 1.2 to 1.5 times higher than the frequency defined by R_{FSET} resistor. In external SYNC configuration, minimum frequency setting with R_{FSET} could go as low as 250 kHz to support 300-kHz switching with external clock.

Feature Description (continued)

Table 1. DC-DC Synchronization Mode

SYNC PIN INPUT	MODE
Low	Spread spectrum disabled
High	Spread spectrum enabled
300 to 2200 kHz frequency	Spread spectrum disabled, external synchronization mode

8.3.1.1.3 Recommended Component Value and Internal Parameters

The LP886xC-Q1 DC-DC converter has an internal compensation network to ensure the stability. There's no external component needed for compensation. It's strongly recommended that the inductance value and the boost input and output capacitors value follow the requirement of Table 2. Also, the DC-DC internal parameters are chosen automatically according to the selected switching frequency (see Table 2) to ensure stability.

Table 2. Boost Converter Parameters⁽¹⁾

RANGE	FREQUENCY (kHz)	TYPICAL INDUCTANCE (μH)	TYPICAL BOOST INPUT AND OUTPUT CAPACITORS (μF)	MINIMUM SWITCH OFF TIME (ns) ⁽²⁾	BLANK TIME (ns)
1	300 to 480	22 or 33	2 × 10 (cer.) + 33 (electr.)	150	95
2	480 to 1150	15	10 (cer.) + 33 (electr.)	60	95
3	1150 to 1650	10	3 × 10 (cer.)	40	95
4	1650 to 2200	4.7 or 10	3 × 10 (cer.)	40	70

(1) Parameters are for reference only

(2) Due to current sensing comparator delay the actual minimum off time is 6 ns (typical) longer than in the table.

8.3.1.1.4 DC-DC Converter Switching Current Limit

The LP886xC-Q1 DC-DC converter has an internal SW FET inside chip's SW pin. The internal FET current is limited to 3.35 A (typical). The DC-DC converter will sense the internal FET current, and turn off the internal FET cycle-by-cycle when the internal FET current reaches the limit.

To support start transient condition, the current limit could be automatically increased to 3.7 A for a short period of 1.6 seconds when a 3.35-A limit is reached.

NOTE

Application condition where the 3.35-A limit is exceeded continuously is not allowed. In this case the current limit would be 3.35 A for 1.6 seconds followed by 3.7-A limit for 1.6 seconds, and this 3.2-second period repeats.

8.3.1.1.5 DC-DC Converter Light Load Mode

LP886xC-Q1 DC-DC converter will enter into light load mode in below condition:

- V_{IN} voltage is very close to V_{OUT}
- Loading current is very low
- PWM pulse width is very short

When DC-DC converter enters into light load mode, DC-DC converter stops switching occasionally to make sure boost output voltage won't rise up too much. It could also be called as PFM mode, since the DC-DC converter switching frequency will change in this mode.

8.3.1.2 Adaptive Voltage Control

The LP886xC-Q1 DC/DC converter generates the supply voltage for the LEDs. During normal operation, boost output voltage is adjusted automatically based on the LED cathode (OUTx pin) voltages. This is called adaptive boost control. Only the active LED outputs are monitored to control the adaptive boost voltage. Any LED strings with open or short faults are removed from the adaptive voltage control loop. The OUTx pin voltages are periodically monitored by the control loop. The boost voltage is raised if any of the OUTx voltage falls below the

$V_{\text{LOW_COMP}}$ threshold. The boost voltage is also lowered if all OUTx voltages are higher than $V_{\text{LOW_COMP}}$ threshold. The boost voltage keeps unchanged when one of OUTx voltage touches the $V_{\text{LOW_COMP}}$ threshold. In normal operation, the lowest voltage among the OUTx pins is around $V_{\text{LOW_COMP}}$, and boost voltage stays constant. $V_{\text{LOW_COMP}}$ level is the minimum voltage which could guarantee proper LED current sink operation. See Figure 10 for how the boost voltage automatically scales based on the OUT1-4 pin voltage.

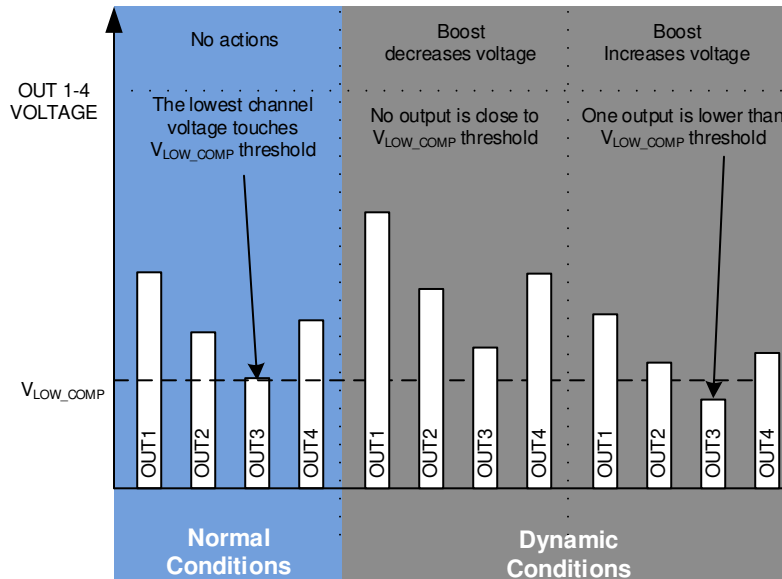


Figure 10. Adaptive Boost Voltage Control Loop Function

8.3.1.2.1 Using Two-Divider

$V_{\text{BOOST_MAX}}$ voltage should be chosen based on the maximum voltage required for LED strings. Recommended maximum voltage is about 3 to 5-V higher than maximum LED string voltage. DC-DC output voltage is adjusted automatically based on LED cathode voltage. The maximum, minimum and initial boost voltages can be calculated with Equation 2:

$$V_{\text{BOOST}} = \left(\frac{V_{\text{BG}}}{R_2} + K \times 0.0387 \right) \times R_1 + V_{\text{BG}}$$

where

- $V_{\text{BG}} = 1.2 \text{ V}$
- R2 recommended value is 10 kΩ to 200 kΩ
- R1/R2 recommended value is 5 to 10 for <1150kHz DC-DC switching frequency
- R1/R2 recommended value is 10 to 20 for >1150kHz DC-DC switching frequency
- $K = 1$ for maximum adaptive boost voltage (typical)
- $K = 0$ for minimum adaptive boost voltage (typical)
- $K = 0.88$ for initial boost voltage (typical)

(2)

For example, if R_1 is set to 750 kΩ and R_2 is set to 130 kΩ, V_{BOOST} will be in the range of 8.1 V to 37.1 V.

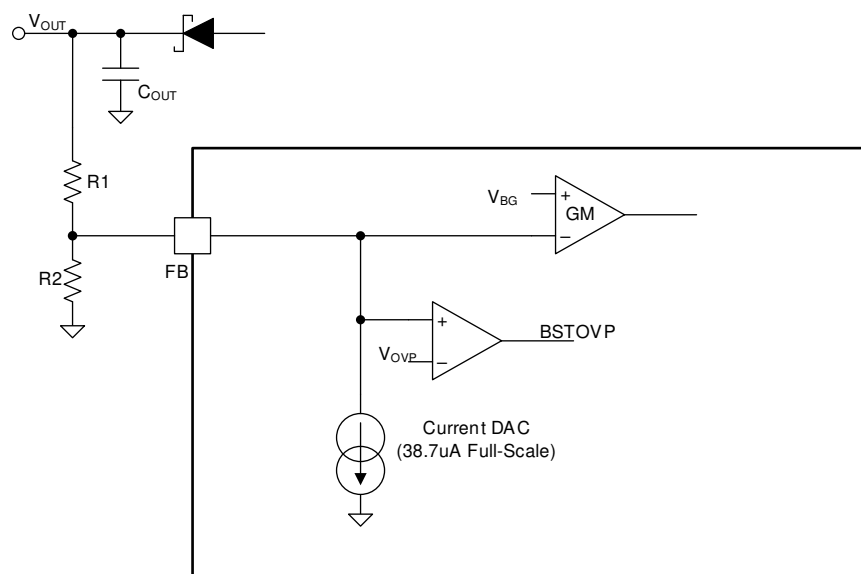


Figure 11. FB External Two-Divider Resistors

8.3.1.2.2 Using T-Divider

Alternatively, a T-divider can be used if resistance less than 100 kΩ is required for the external resistive divider. Then the maximum, minimum and initial boost voltages can be calculated with

$$V_{\text{BOOST}} = \left(\frac{R_1 \times R_3}{R_2} + R_1 + R_3 \right) K \times 0.0387 + \left(\frac{R_1}{R_2} + 1 \right) \times V_{\text{BG}}$$

where

- $V_{\text{BG}} = 1.2 \text{ V}$
- R2 recommended value is 10 kΩ to 200 kΩ
- R1/R2 recommended value is 5 to 10 for <1150kHz DC-DC switching frequency
- R1/R2 recommended value is 10 to 20 for >1150kHz DC-DC switching frequency
- $K = 1$ for maximum adaptive boost voltage (typical)
- $K = 0$ for minimum adaptive boost voltage (typical)
- $K = 0.88$ for initial boost voltage (typical)

(3)

For example, if R_1 is set to 100 kΩ, R_2 is set to 10 kΩ and R_3 is set to 60 kΩ, V_{BOOST} will be in the range of 13.2 V to 42.6 V.

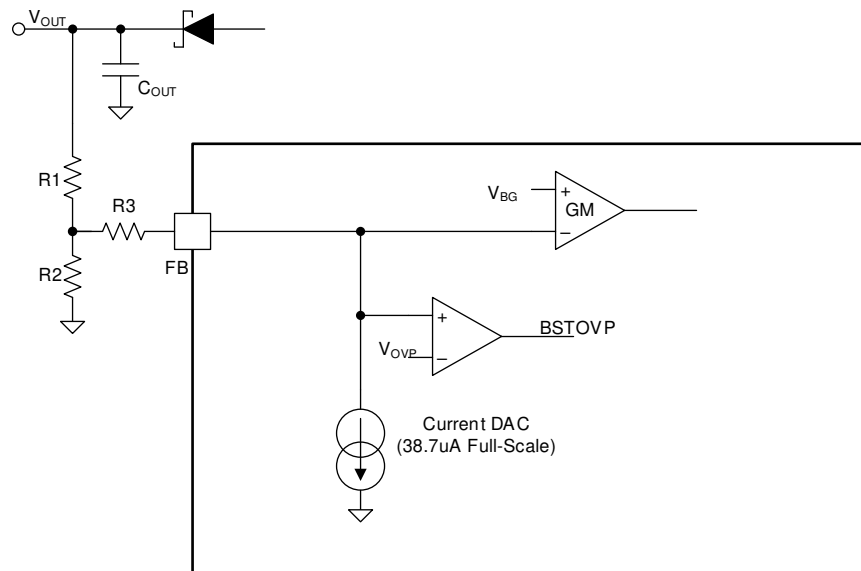


Figure 12. FB external T-divider resistors

8.3.1.2.3 Feedback Capacitor

When operating with no electrolytic capacitor in boost output, which is a typical case when boost frequency is in the 1.15-MHz to 2.2-MHz range, a feedback capacitor needs to be put in parallel with R1 to ensure the loop stability. The value of the capacitor is recommended to be:

$$C_{FB} = \frac{1}{2\pi f_z R_1}$$

where

- $f_z = 20 \text{ kHz}$

(4)

For example, if R_1 is set to 750 k Ω , C_{FB} needs to be around 11 pF.

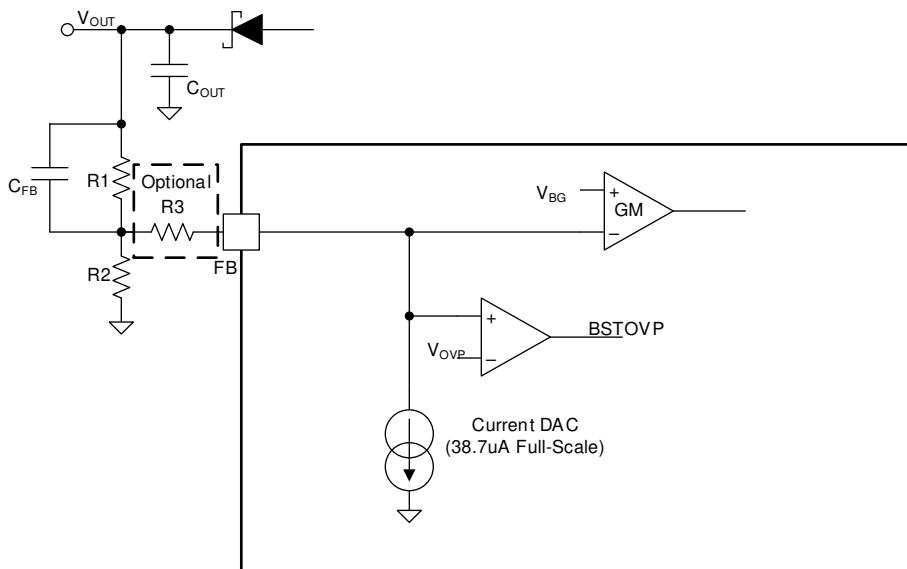


Figure 13. FB External Resistors With Capacitor When Operating With No Electrolytic Capacitor In Boost Output

8.3.2 Internal LDO

The internal LDO regulator converts the input voltage at VIN to a 4.3-V output voltage for internal use. Connect a minimum of 1-μF ceramic capacitor from LDO pin to ground, as close to the LDO pin as possible.

8.3.3 LED Current Sinks

8.3.3.1 LED Output Configuration

LP886xC-Q1 detects LED output configuration during start-up. Any current sink output connected to ground is disabled and excluded from the adaptive voltage control of the DC-DC converter and fault detections.

If more current is needed, LP886xC-Q1's output could also be connected together to support the high current LED.

8.3.3.2 LED Current Setting

The output current of the LED outputs is controlled with external R_{ISSET} resistor. R_{ISSET} value for the target LED current per channel can be calculated using [Equation 5](#):

$$I_{LED} = 2000 \times \frac{V_{BG}}{R_{ISSET}}$$

where

- V_{BG} = 1.2 V
 - R_{ISSET} is current setting resistor, kΩ
 - I_{LED} is output current per OUTx pin, mA
- (5)

For example, if R_{ISSET} is set to 20 kΩ, I_{LED} will be 120 mA per channel.

8.3.3.3 Brightness Control

LP886xC-Q1 controls the brightness of the display with conventional PWM. Output PWM directly follows the input PWM. Input PWM frequency can be in the range of 100 Hz to 20 kHz.

8.3.4 Protection and Fault Detections

The LP886xC-Q1 has fault detection for LED open and short, VIN input overvoltage protection (VIN_OVP), VIN undervoltage protection (VIN_UVLO), Boost output overvoltage protection (BST_OVP), SW overvoltage protection (SW_OVP) and thermal shutdown (TSD).

8.3.4.1 Supply Fault and Protection

8.3.4.1.1 VIN Undervoltage Fault (VIN_UVLO)

The LP886xC-Q1 device supports VIN undervoltage protection. The VIN undervoltage falling threshold is 3.85-V typical and rising threshold is 4-V typical. If during operation of the LP886xC-Q1 device, the VIN pin voltage falls below the VIN undervoltage falling threshold, the boost, LED outputs, and power-line FET will be turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The LP886xC-Q1 will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. VIN_UVLO fault detection is available in SOFT START, BOOST START, and NORMAL state.

8.3.4.1.2 VIN Overvoltage Fault (VIN_OVP)

The LP886xC-Q1 device supports VIN overvoltage protection. The VIN overvoltage threshold is 42-V typical. If during LP886xC-Q1 operation, VIN pin voltage rises above the VIN overvoltage threshold, the boost, LED outputs and the power-line FET will be turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The LP886xC-Q1 will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. VIN_OVP fault detection is available in SOFT START, BOOST START and NORMAL state.

8.3.4.2 Boost Fault and Protection

8.3.4.2.1 Boost Overvoltage Fault (BST_OVP)

The LP886xC-Q1 device supports boost overvoltage protection. If during LP886xC-Q1 operation, the FB pin voltage exceeds the V_{FB_OVP} threshold, which is 2.3-V typical, the boost, LED outputs and the power-line FET will be turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The LP886xC-Q1 will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. BST_OVP fault detection is available in NORMAL state.

Calculating back from FB pin voltage threshold to boost output OVP voltage threshold, the value is not a static threshold, but a dynamic threshold changing with the current target boost adaptive voltage:

$$V_{BOOST_OVP} = V_{BOOST} + \left(\frac{R_1}{R_2} + 1 \right) \times (V_{FB_OVP} - V_{BG})$$

where

- V_{BOOST} is the current target boost adaptive voltage, which in most time is the current largest LED string forward voltage among multiple strings + 0.9 V in steady state
- $V_{FB_OVP} = 2.3 \text{ V}$
- $V_{BG} = 1.2 \text{ V}$
- R_1 and R_2 is the resistor value of FB external network in [Using Two-Divider](#) and [Using T-Divider](#) (6)

For example, if R_1 is set to 750 k Ω and R_2 is set to 130 k Ω , V_{BOOST} will report OVP when the boost voltage is 7.4 V above target boost voltage.

This equation holds true in both two-divider FB external network and T-divider FB external network.

8.3.4.2.2 SW Overvoltage Fault (SW_OVP)

Besides boost overvoltage protection, the LP886xC-Q1 supports SW pin overvoltage protection to further protect the boost system from overvoltage scenario. If during LP886xC-Q1 operation, the SW pin voltage exceeds the V_{SW_OVP} threshold, which is 49-V typical, the boost, LED outputs and the power-line FET are turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The LP886xC-Q1 will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. SW_OVP fault detection is available in SOFT START, BOOST START and NORMAL state.

8.3.4.3 LED Fault and Protection

Every LED current sink has 3 comparators for LED fault detections.

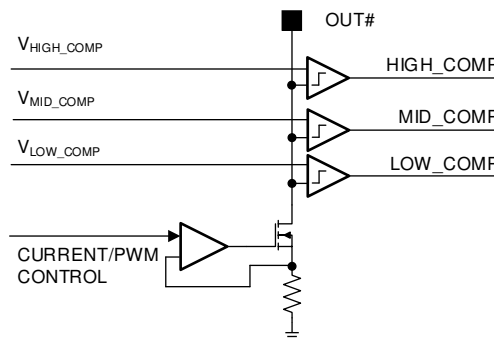


Figure 14. Comparators for LED Fault Detection

Figure 15 shows cases which generates LED faults. Any LED faults will pull the Fault pin low.

8.3.4.3.1 LED Open Fault (LED_OPEN)

During normal operation, boost voltage is raised if any of the used LED outputs falls below the $V_{\text{LOW_COMP}}$ threshold. Open LED fault is detected if boost output voltage has reached the maximum and at least one LED output is still below the threshold. The open string is then disconnected from the boost adaptive control loop and its output is disabled.

8.3.4.3.2 LED Short Fault (LED_SHORT)

Shorted LED fault is detected if one or more LED outputs are above the $V_{\text{HIGH_COMP}}$ threshold (typical 6 V) and at least one LED output is inside the normal operation window (between $V_{\text{LOW_COMP}}$ and $V_{\text{MID_COMP}}$, typical 0.9 V and 1.9 V). The shorted string is disconnected from the boost adaptive control loop and its output is disabled.

LED Open fault detection and LED Short fault detection are available only in NORMAL state.

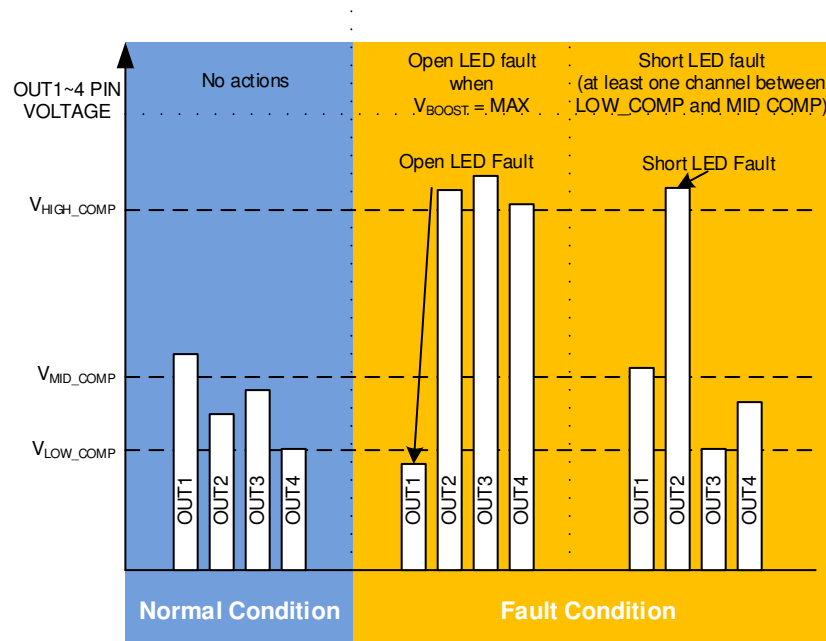


Figure 15. Protection and DC-DC Voltage Adaptation Algorithms

If LED fault is detected, the device continues normal operation and only the faulty string is disabled. The fault is indicated via the FAULT pin which can be released by toggling VDDIO/EN pin low for a short period of 2 μs to 20 μs . LEDs are turned off for this period but the device stays in NORMAL state. If VDDIO/EN is low longer, the device goes to STANDBY and restarts when EN goes high again.

This means if the system doesn't want to simply disable the device because of LED faults. It could clear the LED faults by toggling VDDIO/EN pin low for a short period of 2 μs to 20 μs .

8.3.4.4 Thermal Fault and Protection (TSD)

If the die temperature of LP886xC-Q1 reaches the thermal shutdown threshold T_{TSD} , which is 165°C typical, the boost, power-line FET and LED outputs are turned off to protect the device from damage. The FAULT pin will be pulled low. The LP886xC-Q1 will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. Only if the die temperature drops lower than $T_{\text{TSD}} - T_{\text{TSD_HYS}}$, which is 145°C typical, the device could start-up normally. TSD fault detection is available in SOFT START, BOOST START and NORMAL state.

8.3.4.5 Overview of the Fault and Protection Schemes

A summary of the LP886xC-Q1 fault detection behavior is shown in [Table 3](#). Detected faults (excluding LED open or short) cause device to enter FAULT RECOVERY state. In FAULT_RECOVERY the DC-DC and LED current sinks of the device are disabled, and the FAULT pin is pulled low. The device will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. When recovery is successful and device enters into NORMAL state, the FAULT pin is released high.

Table 3. Fault Detections

FAULT/ PROTECTION	FAULT NAME	CONDITION	FAULT PIN	Enter FAULT_RECOVERY STATE	ACTIVE STATE	ACTION
VIN overvoltage protection	VIN_OVP	VIN > 42 V	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts after 100 ms
VIN undervoltage protection	VIN_UVLO	Effective when VIN < 3.85 V Released when VIN >4 V	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts after 100 ms
Open LED fault	LED_OPEN	Adaptive Voltage is max. and any OUTx voltage < 0.9 V	Yes	No	NORMAL	Open string is removed from the DC-DC voltage control loop and output is disabled. Fault pin low could be released by toggling VDDIO/EN pin, If VDDIO/EN is low for a period of 2 μ s to 20 μ s, LEDs are turned off for this period but device stays in NORMAL.
Shorted LED fault	LED_SHORT	One of OUTx voltage is [0.9 V, 1.9 V] and any OUTx voltage > 6 V	Yes	No	NORMAL	Short string is removed from the DC-DC voltage control loop and output is disabled. Fault pin low could be released by toggling VDDIO/EN pin, If VDDIO/EN is low for a period of 2 μ s to 20 μ s, LEDs are turned off for this period but device stays NORMAL.
Boost overvoltage protection	BST_OVP	V _{FB} > 2.3 V	Yes	Yes	NORMAL	Fault is detected if boost overvoltage condition duration is more than 560 ms Device enters into FAULT RECOVERY state, and restarts after 100 ms
SW overvoltage protection	SW_OVP	V _{SW} > 49 V	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts after 100 ms
Thermal protection	TSD	Effective when T _j > 165 °C Released when T _j < 145 °C	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts until TSD fault is released

8.4 Device Functional Modes

8.4.1 STANDBY State

The LP886xC-Q1 enters STANDBY state when the VIN voltage powers on and voltage is higher than VINUVLO rising threshold, which is 4-V typical. In STANDBY state, the device is able to detect VDDIO/EN signal. When VDDIO/EN is pulled high, the internal LDO wakes up and the device enters into SOFT START state. The device will re-enter the STANDBY state when VDDIO/EN is pulled low for more than 50 μ s.

8.4.2 SOFT START State

In SOFT START state, Power-line FET is enabled, and boost input and output capacitors are charged to VIN level. VIN_OVP, VIN_UVLO, SW_OVP and TSD fault are active. After 65 ms, the device enters into BOOST START state.

8.4.3 BOOST START State

In BOOST START state, DC-DC controller is turned on and boost voltage is ramped to initial boost voltage level with reduced current limit. VIN_OVP, VIN_UVLO, SW_OVP and TSD fault are active in this state. After 50 ms, LED outputs do a one-time detection on grounded outputs. Grounded outputs are disabled and excluded from the adaptive voltage control loop. Then the device enters into NORMAL state.

8.4.4 NORMAL State

In NORMAL state, LED drivers are enabled when PWM signal is high. All faults are active in this state. Fault pin will be released high in the start of NORMAL state if recovering from FAULT RECOVERY state and no fault is available.

8.4.5 FAULT RECOVERY State

Non-LED faults can trigger fault recovery state. LED drivers, boost converter and power-line FET are all disabled. After 100 ms, the device attempts to restart from SOFT START state if VDDIO/EN is still high.

8.4.6 State Diagram and Timing Diagram for Start-up and Shutdown

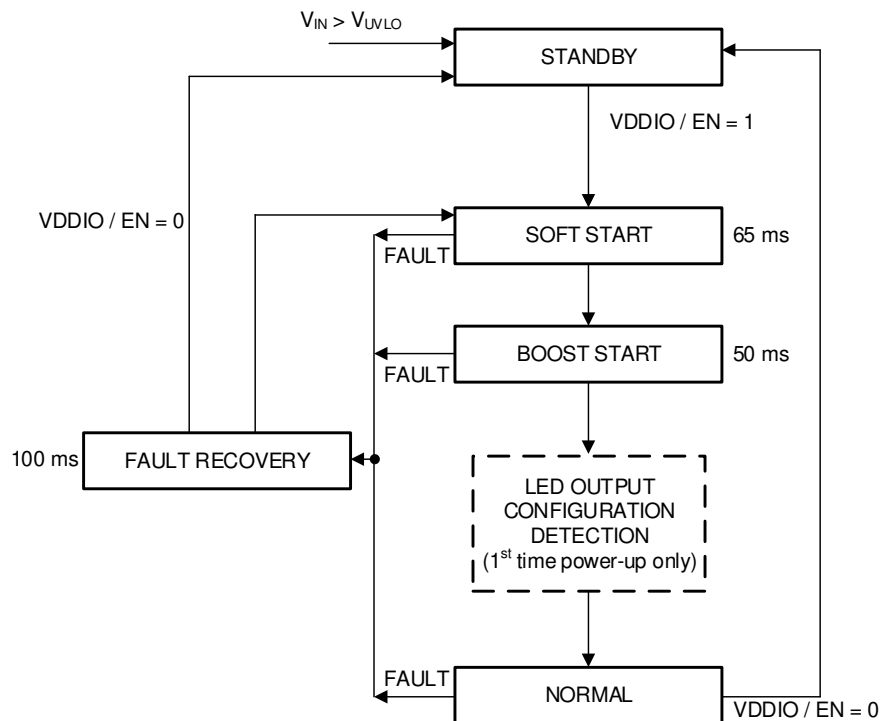


Figure 16. State Diagram

Device Functional Modes (continued)

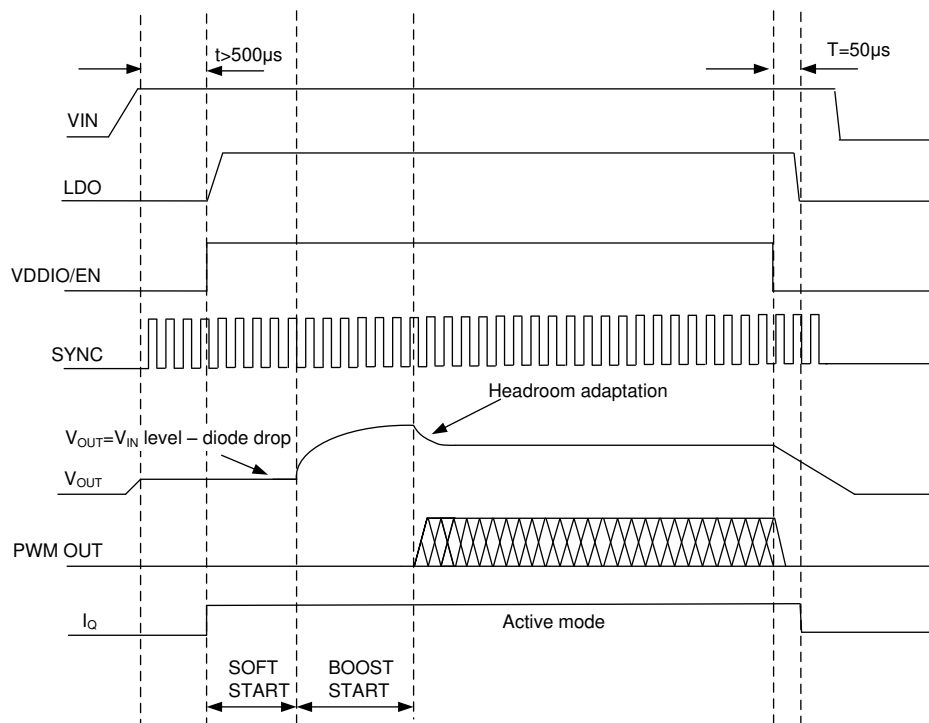


Figure 17. Timing Diagram for the Typical Start-Up and Shutdown

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP886xC-Q1 is designed for automotive applications. The input voltage (V_{IN}) is intended to be connected to the automotive battery, which supports voltage range from 4.5 V to 40 V. Device internal circuitry is powered from the integrated LDO.

The LP886xC-Q1 uses a simple four-wire control:

- VDDIO/EN for enable
- PWM input for brightness control
- SYNC pin for boost synchronisation (optional)
- FAULT output to indicate fault condition (optional)

9.2 Typical Applications

9.2.1 Typical Application for 4 LED Strings

Figure 18 shows the typical application for LP8867-Q1 which supports 4 LED strings, 100 mA per string, with a boost switching frequency of 400 kHz.

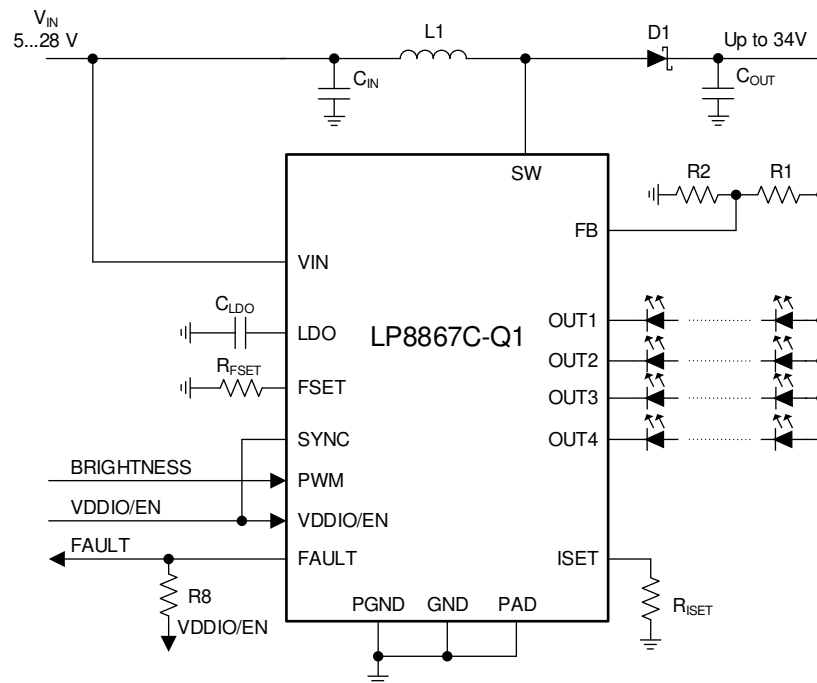


Figure 18. Four Strings 100 mA per String Configuration

Typical Applications (continued)

9.2.1.1 Design Requirements

DESIGN PARAMETER	VALUE
V _{IN} voltage range	5 V – 28 V
LED string	4P8S LEDs (30 V max)
LED string current	100 mA
Maximum boost voltage	34 V
Boost switching frequency	400 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	33 µH
C _{IN}	100 µF, 50 V
C _{IN BOOST}	2 × (10 µF, 50-V ceramic) + 33 µF, 50-V electrolytic
C _{OUT}	2 × (10 µF, 50-V ceramic) + 33 µF, 50-V electrolytic
C _{LDO}	1 µF, 10 V
R _{ISET}	24 kΩ
R _{FSET}	160 kΩ
R1	685 kΩ
R2	130 kΩ
R8	10 kΩ

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferred. The saturation current must be greater than the sum of the maximum load current, and the worst case average-to-peak inductor current. Equation 7 shows the worst case conditions

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE} - peak inductor current
- I_{OUTMAX} - maximum load current
- V_{IN} - minimum input voltage in application
- L - min inductor value including worst case tolerances
- f - minimum switching frequency
- V_{OUT} - output voltage
- D - Duty Cycle for CCM Operation

(7)

As a result, the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. A saturation current rating of at least 4.1 A is recommended for most applications. See Table 2 for recommended inductance value for the different switching frequency ranges. The inductor's resistance should be less than 300 mΩ for good efficiency.

See detailed information in [Understanding Boost Power Stages in Switch Mode Power Supplies](#). [Power Stage Designer Tool](#) can be used for the boost calculation.

9.2.1.2.2 Output Capacitor Selection

A ceramic capacitor with $2 \times V_{MAX_BOOST}$ or more voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. If the selected ceramic capacitors' voltage rating is less than $2 \times V_{MAX_BOOST}$, an alternative way is to increase the number of ceramic capacitors. Capacitance recommendations for different switching frequencies are shown in [Table 2](#). To minimize audible noise of ceramic capacitors their physical size should typically be minimized.

9.2.1.2.3 Input Capacitor Selection

A ceramic capacitor with $2 \times V_{IN_MAX}$ or more voltage rating is recommended for the input capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. If the selected ceramic capacitors' voltage rating is less than $2 \times V_{MAX_BOOST}$, an alternative way is to increase the number of ceramic capacitors. Capacitance recommendations for different boost switching frequencies are shown in [Table 2](#).

9.2.1.2.4 LDO Output Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 1-μF capacitor is sufficient.

9.2.1.2.5 Diode

A Schottky diode should be used for the boost output diode. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times degrade the efficiency and the load regulation. Diode rating for peak repetitive current should be greater than inductor peak current (up to 4.1 A) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage. The junction capacitance of Schottky diodes are also very important. Big junction capacitance leads to huge reverse current and big noise when boost is switching. A <500-pF junction capacitance at $V_R = 0.1$ V Schottky diode is recommended.

9.2.1.3 Application Curves

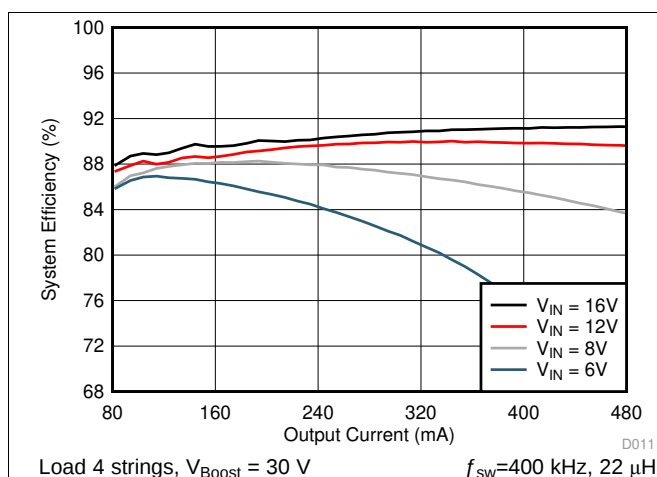


Figure 19. System Efficiency

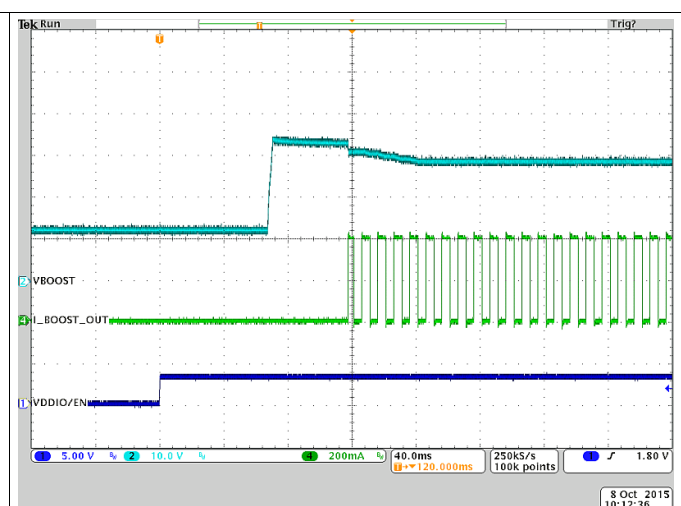


Figure 20. Typical Start-Up

9.2.2 SEPIC Mode Application

When LED string voltage can be above or below V_{IN} voltage, SEPIC configuration can be used. In this example, two separate coils or coupled coil could both be used for SEPIC. Separate coils can enable lower height external components to be used, compared to a coupled coil solution. On the other hand, coupled coil typically maximizes the efficiency. Also, in this example, an external clock is used to synchronize SEPIC switching frequency. External clock input can be modulated to spread switching frequency spectrum.

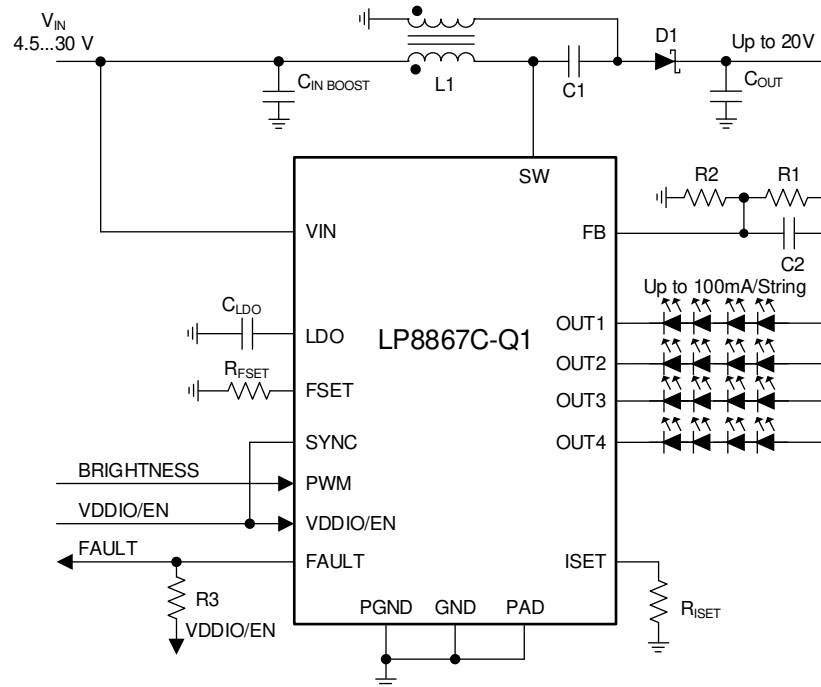


Figure 21. SEPIC Mode, 4 Strings 100 mA and String Configuration

9.2.2.1 Design Requirements

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5 V – 30 V
LED string	4P4S LEDs (15 V max)
LED string current	100 mA
Maximum output voltage	20 V
SEPIC switching frequency	2.2 MHz
External sync for SEPIC	used
Spread spectrum	Internal spread spectrum disabled (external sync used)
L1, L2	4.7 μ H
C_{IN}	10 μ F 50 V
C_{IN} SEPIC	2 $\times$ 10 μ F, 50-V ceramic + 33 μ F, 50-V electrolytic
C1	10- μ F 50-V ceramic
C2	30 pF
C_{OUT}	2 $\times$ 10 μ F, 50-V ceramic + 33 μ F, 50-V electrolytic
C_{LDO}	1 μ F, 10 V
R_{ISET}	24 k Ω
R_{FSET}	24 k Ω
R1	265 k Ω
R2	37 k Ω
R3	10 k Ω

9.2.2.2 Detailed Design Procedure

In SEPIC mode the maximum voltage at the SW pin is equal to the sum of the input voltage and the output voltage. Because of this, the maximum sum of input and output voltage must be limited below 49 V. See the [Detailed Design Procedure](#) section for general external component guidelines. Main differences of SEPIC compared to boost are described below.

[Power Stage Designer™ Tool](#) can be used for modeling SEPIC behavior. For detailed explanation on SEPIC see Texas Instruments Analog Applications Journal [Designing DC/DC Converters Based on SEPIC Topology](#).

9.2.2.2.1 Inductor

In SEPIC mode, currents flowing through the coupled inductors or the two separate inductors L1 and L2 are the input current and output current, respectively. Values can be calculated using [Power Stage Designer™ Tool](#) or using equations in [Designing DC/DC Converters Based on SEPIC Topology](#).

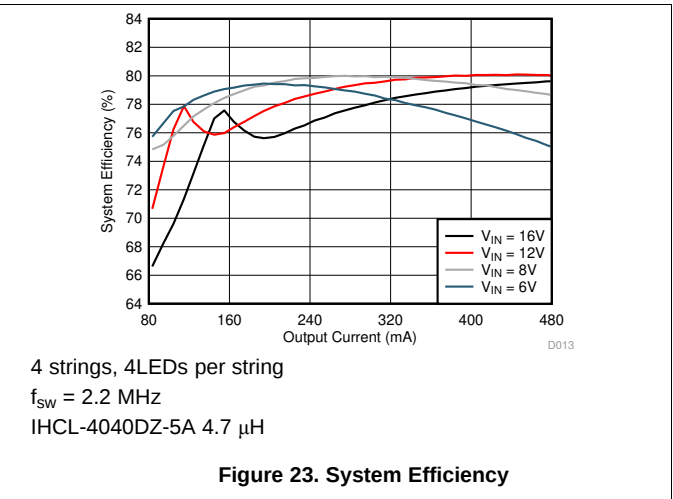
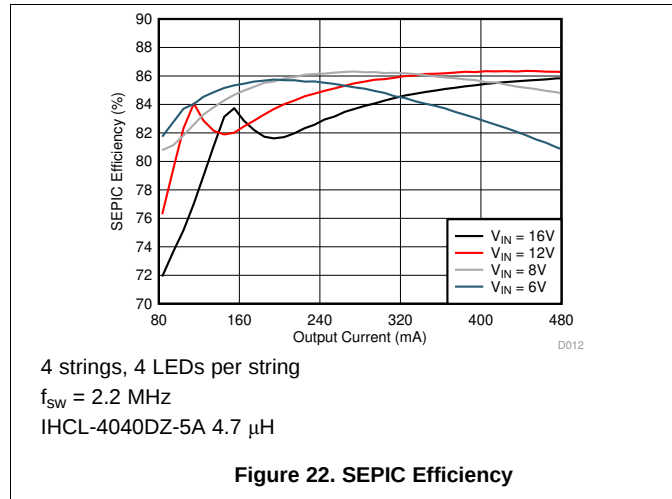
9.2.2.2.2 Diode

In SEPIC mode diode peak current is equal to the sum of input and output currents. Diode rating for peak repetitive current should be greater than SW pin current limit (up to 4.1 A for transients) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Diode voltage rating must be higher than sum of input and output voltages.

9.2.2.2.3 Capacitor C1

TI recommends a ceramic capacitor with low ESR. Capacitor voltage rating must be higher than maximum input voltage.

9.2.2.3 Application Curves



10 Power Supply Recommendations

The device is designed to operate from an automotive battery. Device should be protected from reversal voltage and voltage dump over 50 V. The resistance of the input supply rail must be low enough so that the input current transient does not cause a high drop at LP886xC-Q1 VIN pin. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to the ceramic bypass capacitors in the VIN line.

11 Layout

11.1 Layout Guidelines

Figure 24 is a layout recommendation for LP886xV-Q1 used to demonstrate the principles of a good layout. This layout can be adapted to the actual application layout if or where possible. It is important that all boost components are close to the chip, and the high current traces must be wide enough. By placing boost components on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. Bypass LDO capacitor must be placed as close as possible to the device.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
 - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to the SW and PGND pins. Input and output capacitor grounds must be close to each other to minimize current loop size.
 - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High-frequency return currents find a route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the **positive** current route in the ground plane, if the ground plane is intact under the route. To minimize the current loop for high frequencies:
 - Inductor's pin in SW node needs to be as near as possible to chip's SW pin
 - Put a small capacitor as near as possible to the diode's pin in boost output node and arrange vias to PGND plane close to the capacitor's GND pin.
- Use separate power and noise-free grounds. PGND is used for boost converter return current and noise-free ground is used for more sensitive signals, such as LDO bypass capacitor grounding as well as grounding the GND pin of the device.
- Boost output feedback voltage to LEDs must be taken out *after* the output capacitors, not straight from the diode cathode.
- Place LDO 1- μ F bypass capacitor as close as possible to the LDO pin.
- Input and output capacitors require strong grounding (wide traces, many vias to GND plane).

11.2 Layout Example

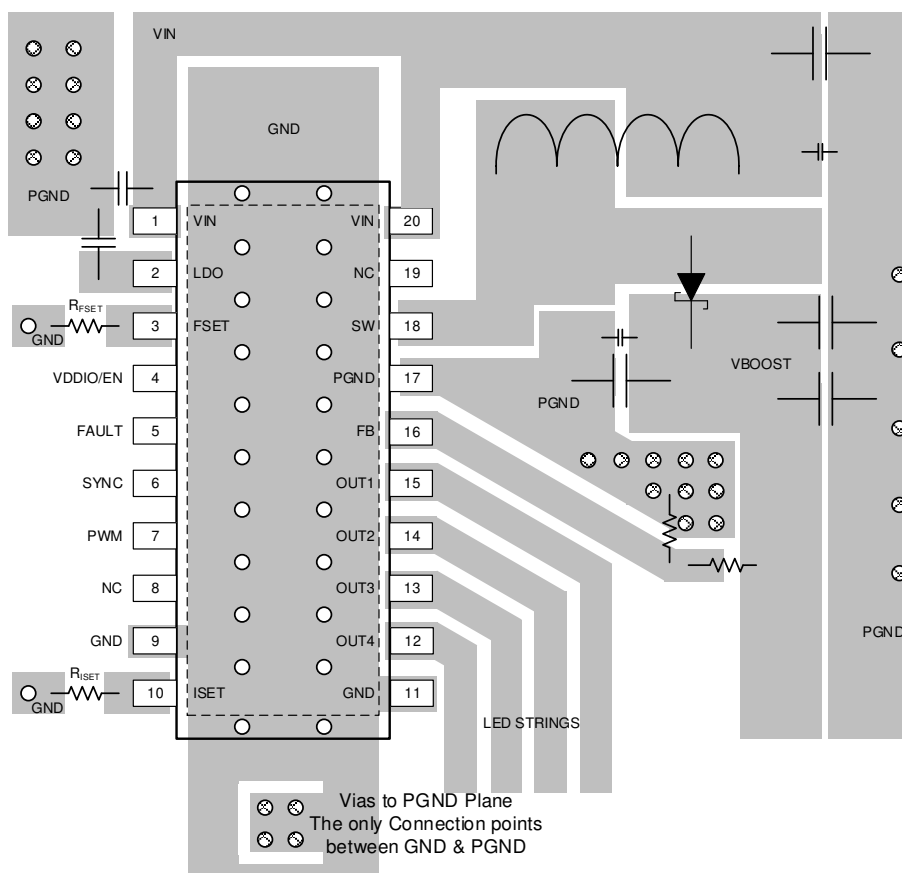


Figure 24. LP886xC-Q1 Boost Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Power Stage Designer™ Tool can be used for both boost and SEPIC: <http://www.ti.com/tool/powerstage-designer>

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- [PowerPAD™ Thermally Enhanced Package](#)
- [Understanding Boost Power Stages in Switch Mode Power Supplies](#)
- [Designing DC-DC Converters Based on SEPIC Topology](#)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

Power Stage Designer, E2E are trademarks of Texas Instruments.
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12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP8867CQPWPRQ1	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8867CQ
LP8869CQPWPRQ1	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8869CQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

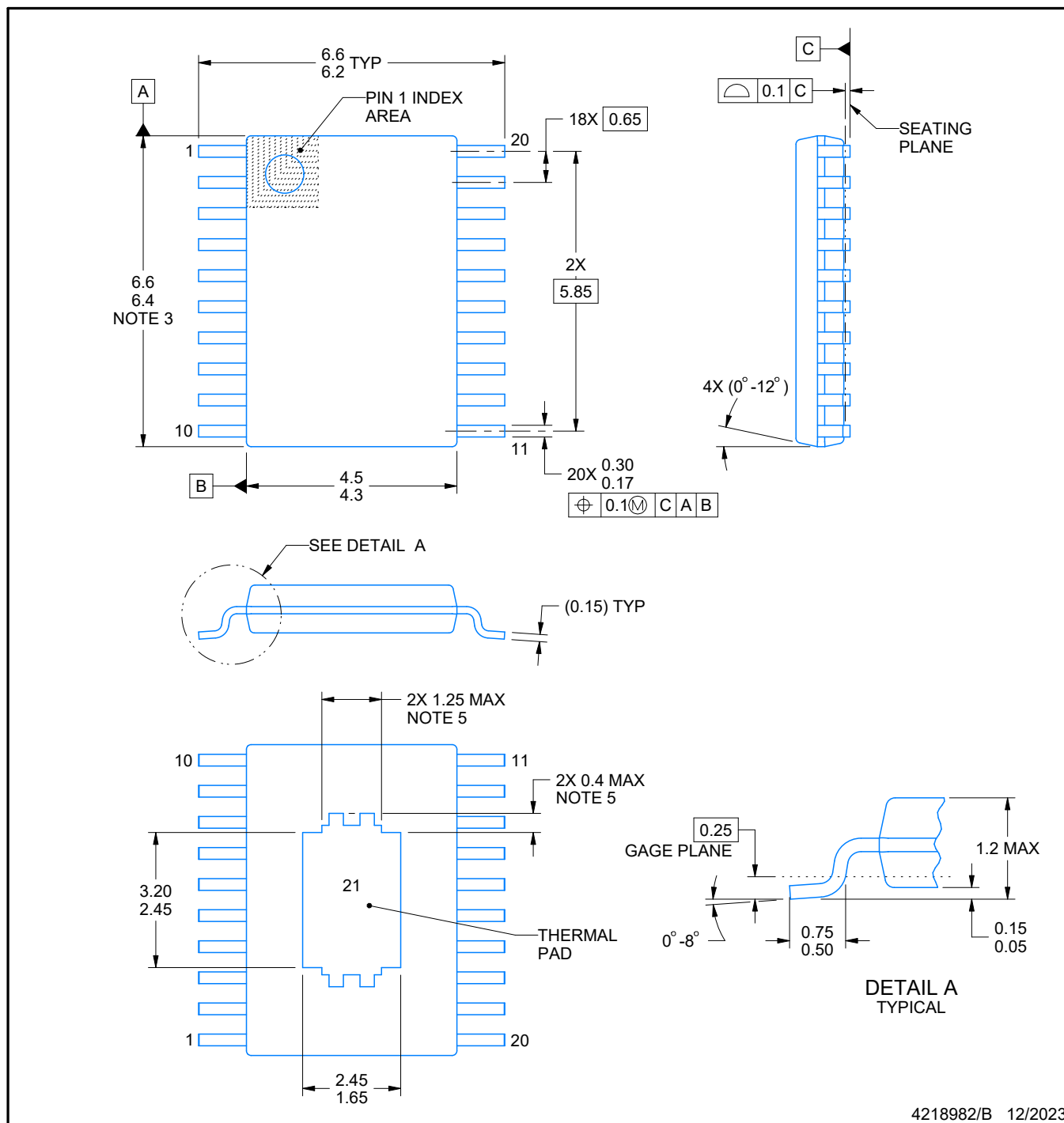
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8867CQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LP8867CQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LP8869CQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LP8869CQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8867CQPWPRQ1	HTSSOP	PWP	20	2000	356.0	356.0	35.0
LP8867CQPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
LP8869CQPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
LP8869CQPWPRQ1	HTSSOP	PWP	20	2000	356.0	356.0	35.0



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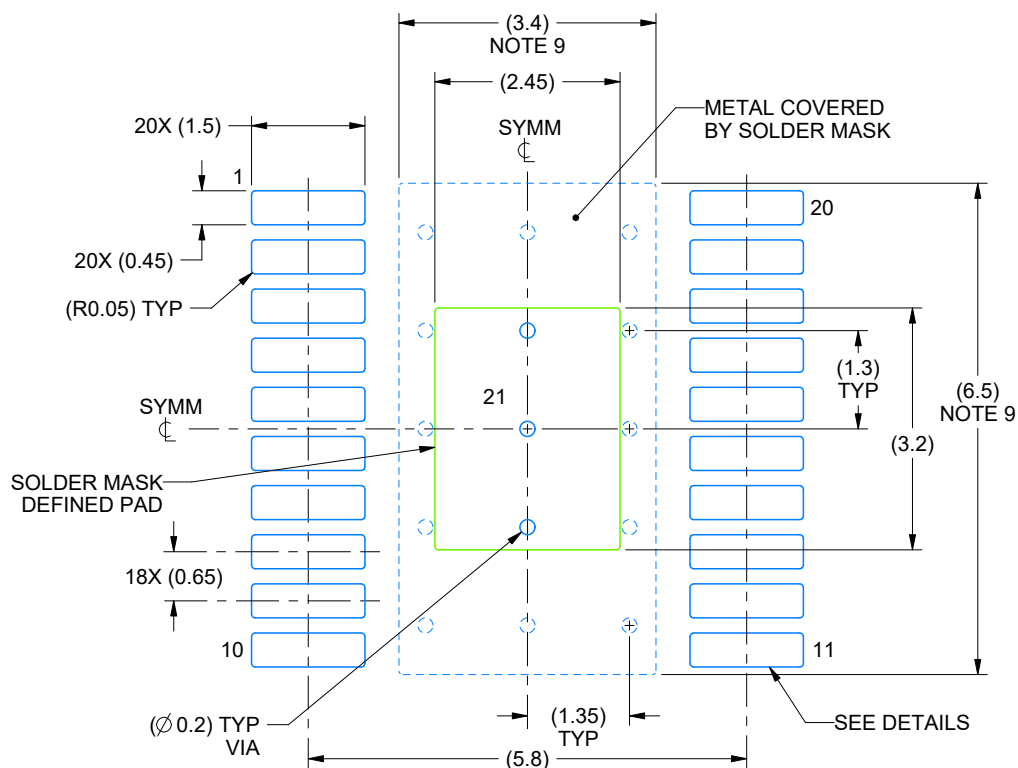
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

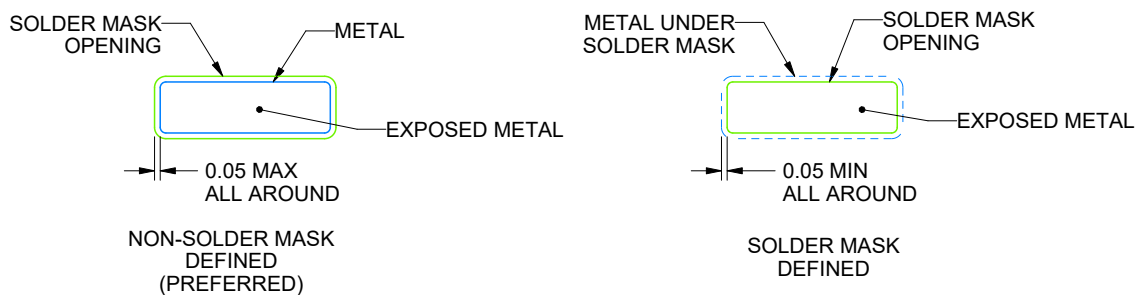
PWP0020N

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4218982/B 12/2023

NOTES: (continued)

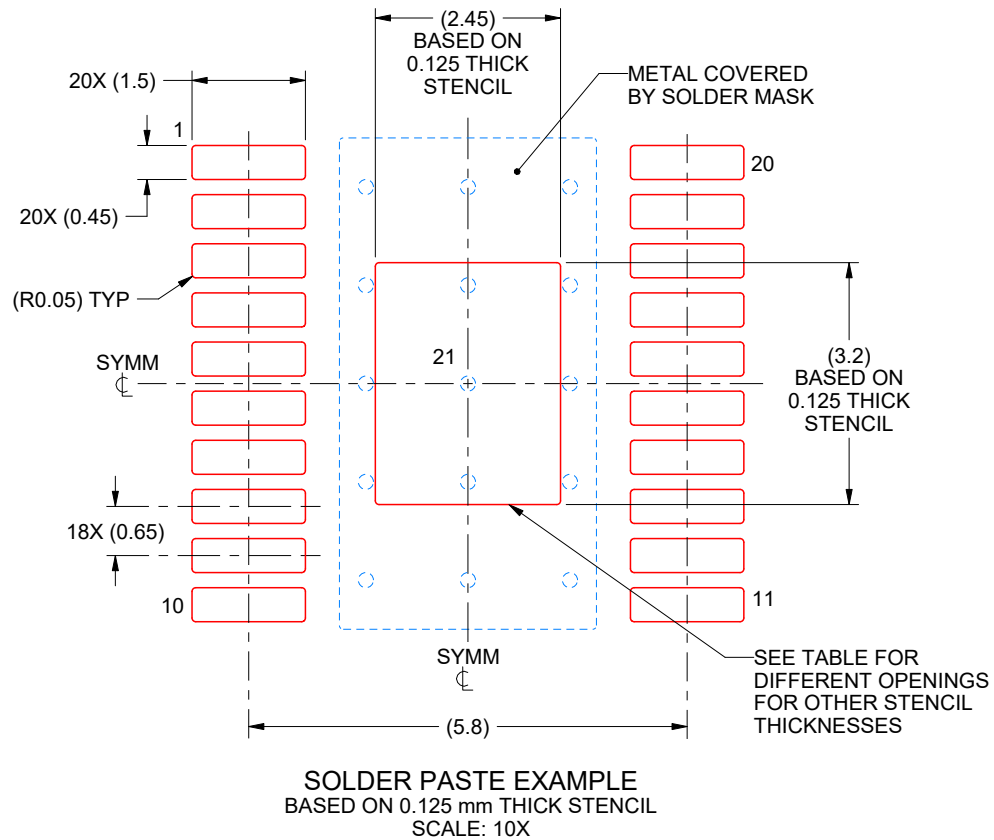
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0020N

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

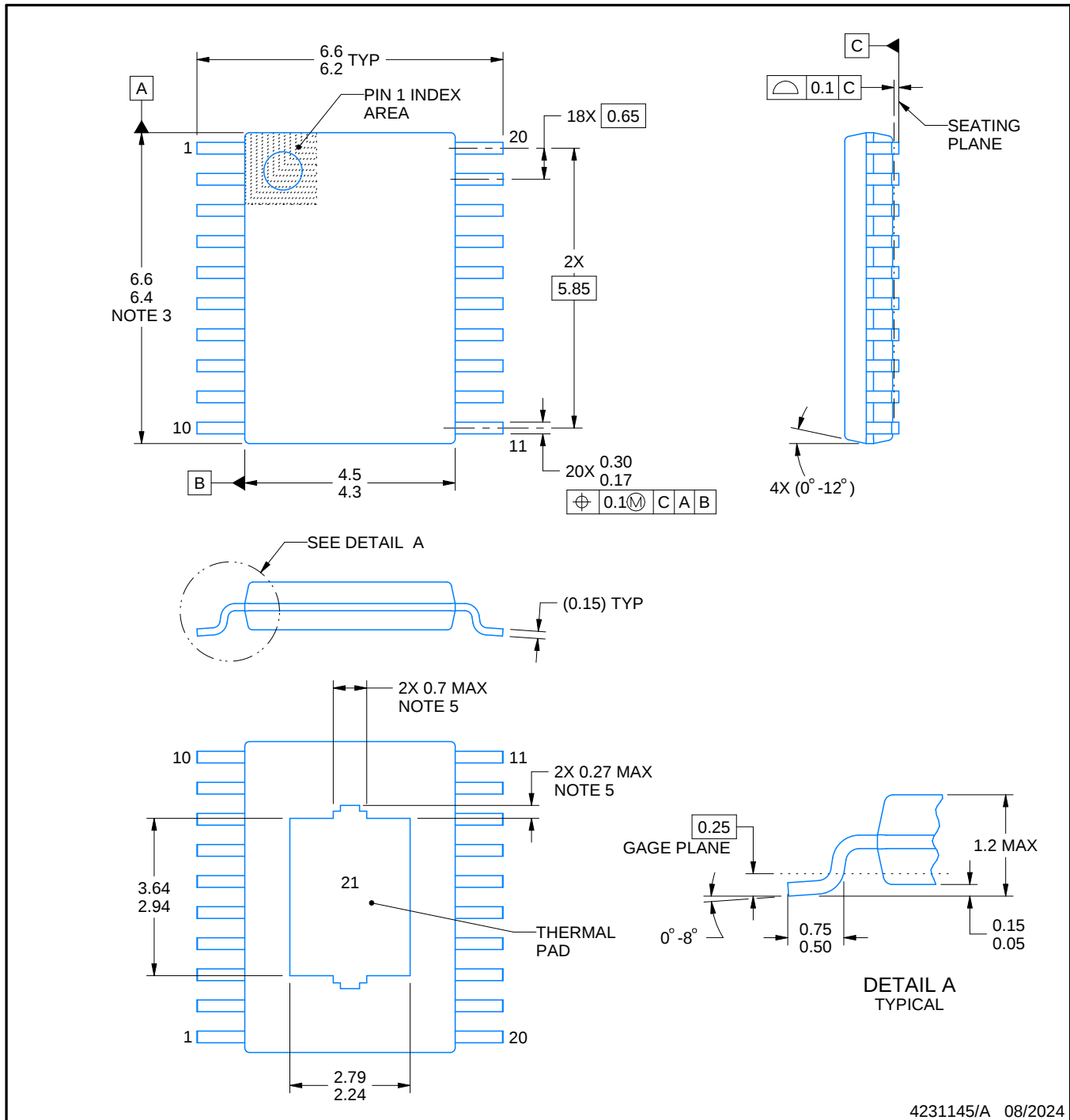
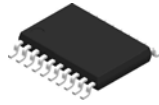


STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.74 X 3.58
0.125	2.5 X 3.2 (SHOWN)
0.15	2.24 X 2.92
0.175	2.07 X 2.70

4218982/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



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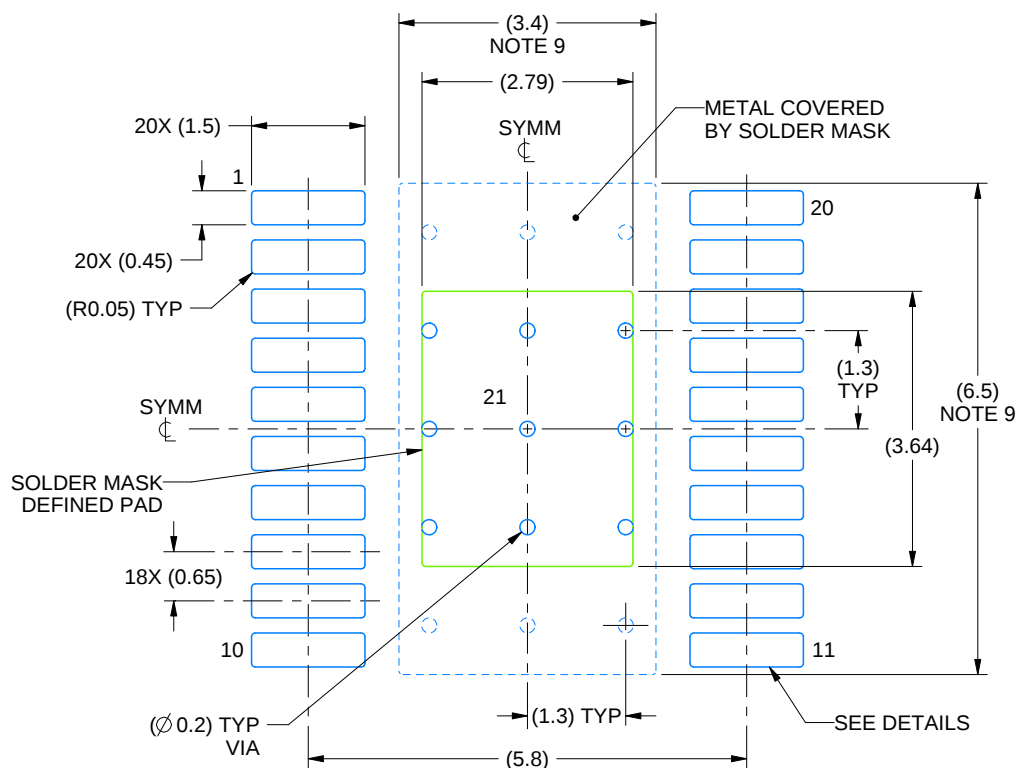
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

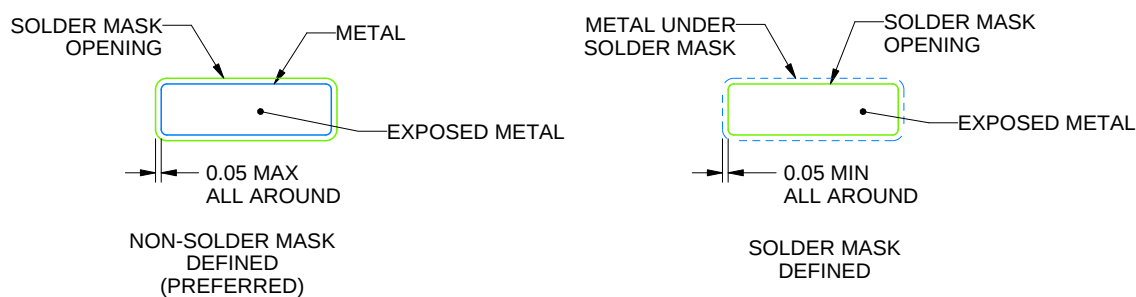
PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

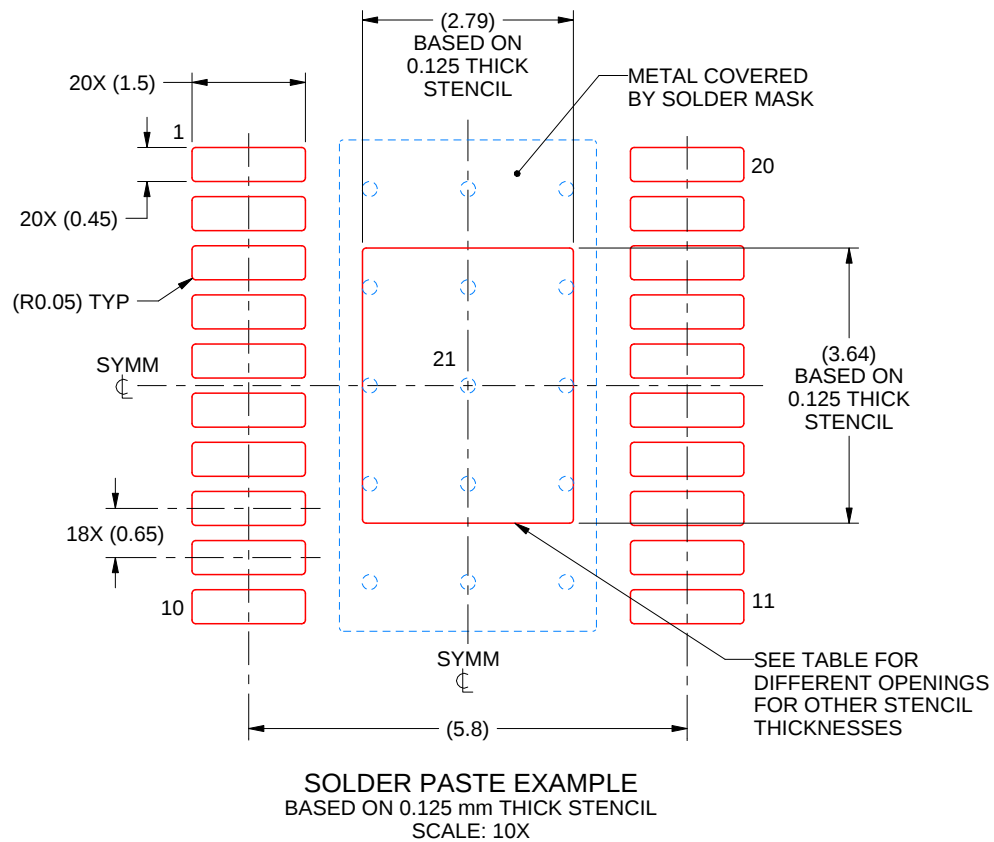
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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