

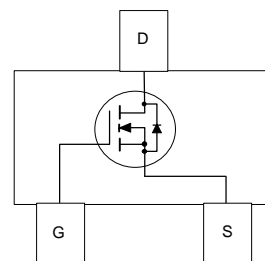
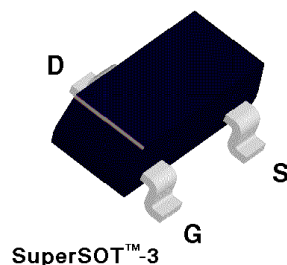
## NDS335N N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

These N -Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 1.7 A, 20 V.  $R_{DS(ON)} = 0.14 \Omega$  @  $V_{GS} = 2.7$  V  
 $R_{DS(ON)} = 0.11 \Omega$  @  $V_{GS} = 4.5$  V.
- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.



### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	NDS335N	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage - Continuous	8	V
$I_D$	Maximum Drain Current - Continuous (Note 1a)	1.7	A
	- Pulsed	10	
$P_D$	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$

# Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V T <sub>J</sub> =125°C			1 10	μA μA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA T <sub>J</sub> =125°C	0.5 0.3	0.7 0.5	1 0.8	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 2.7 V, I <sub>D</sub> = 1.7 A T <sub>J</sub> =125°C V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.7 A		0.084 0.13 0.065	0.14 0.25 0.11	Ω
I <sub>D(ON)</sub>	On-State Drain Current	V <sub>GS</sub> = 2.7 V, V <sub>DS</sub> = 5 V V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V	5 10			A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 1.7 A,		6		S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		240		pF
C <sub>oss</sub>	Output Capacitance			130		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
t <sub>d(on)</sub>	Turn - On Delay Time	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 4.5 V, R <sub>Gen</sub> = 6 Ω		8	20	ns
t <sub>r</sub>	Turn - On Rise Time			29	45	ns
t <sub>d(off)</sub>	Turn - Off Delay Time			28	40	ns
t <sub>f</sub>	Turn - Off Fall Time			8	20	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.7 A, V <sub>GS</sub> = 4.5 V		6.4	9	nC
Q <sub>gs</sub>	Gate-Source Charge			0.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			2		nC

# Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				10	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.42 A (Note 2)		0.8	1.2	V

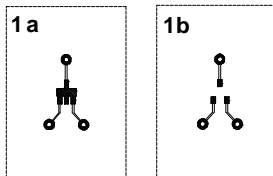
Notes:

1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJA</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta J} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{rJ}$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 250°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- b. 270°C/W when mounted on a 0.001 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

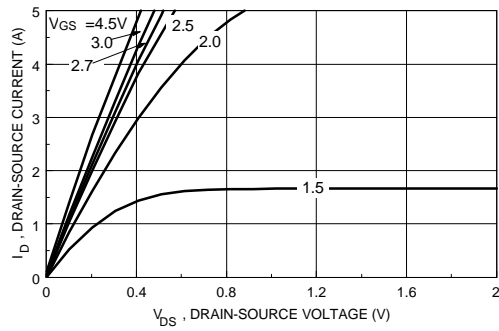


Figure 1. On-Region Characteristics.

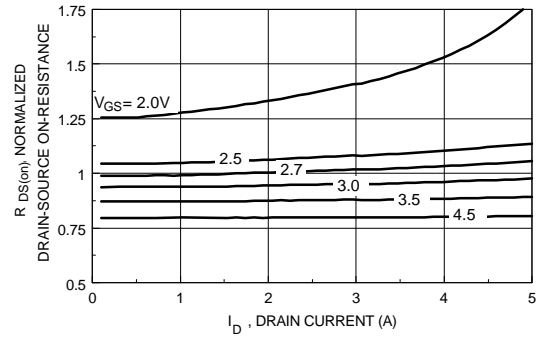


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

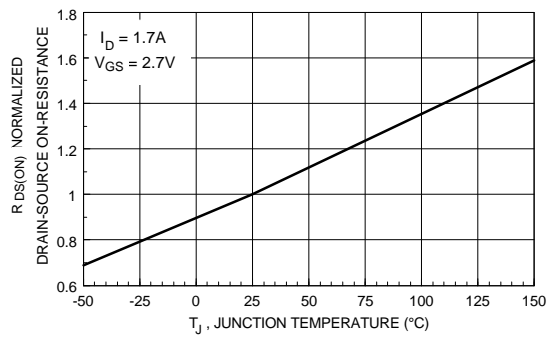


Figure 3. On-Resistance Variation with Temperature.

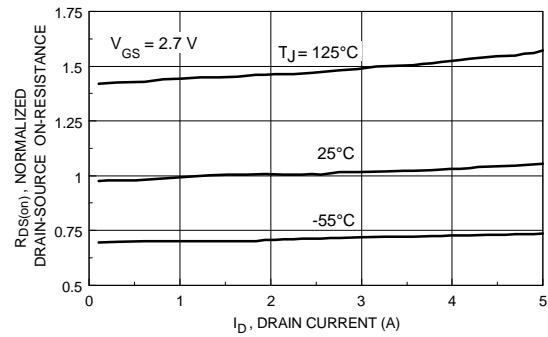


Figure 4. On-Resistance Variation with Drain Current and Temperature.

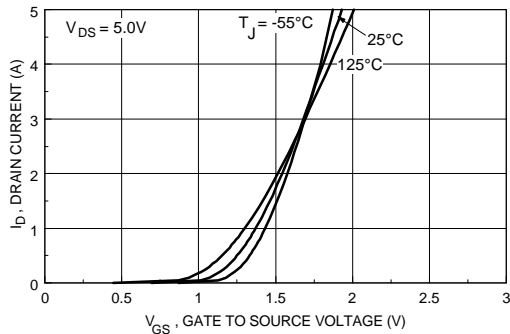


Figure 5. Transfer Characteristics.

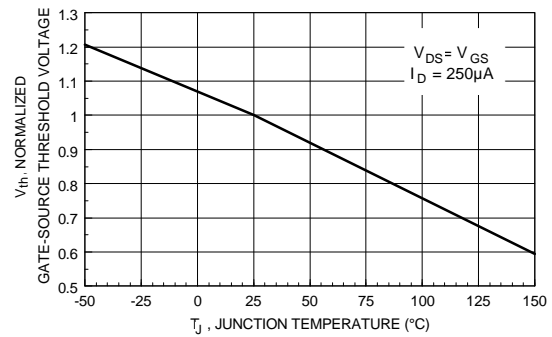
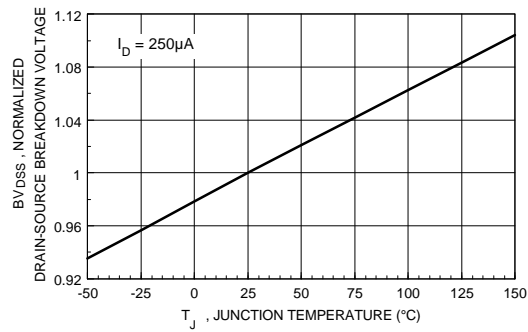
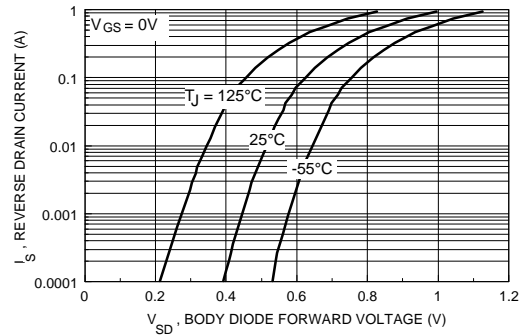


Figure 6. Gate Threshold Variation with Temperature.

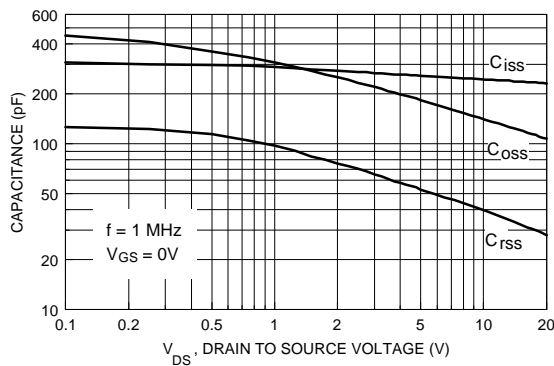
## Typical Electrical Characteristics (continued)



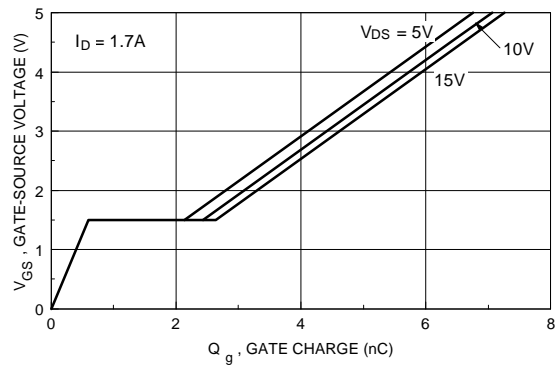
**Figure 7. Breakdown Voltage Variation with Temperature.**



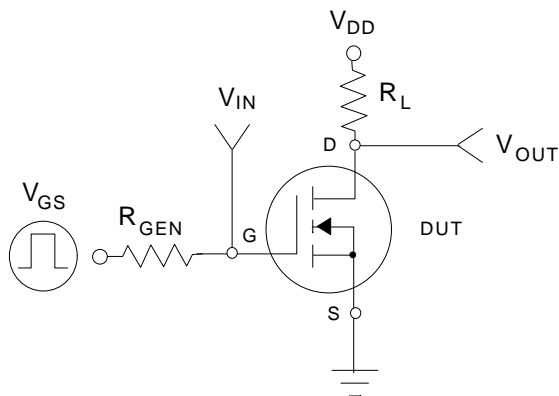
**Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.**



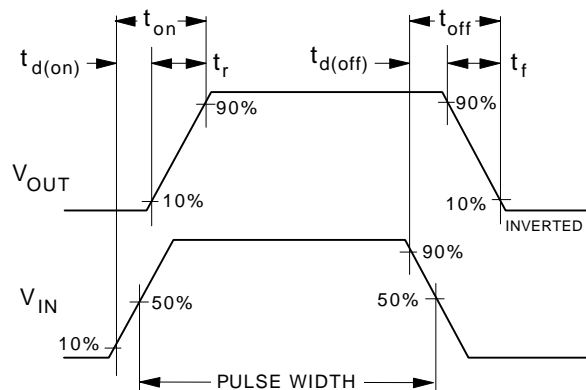
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**

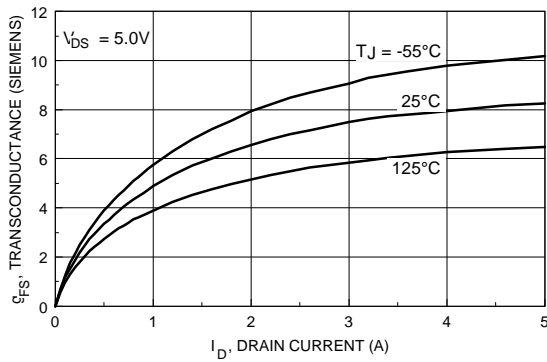


**Figure 11. Switching Test Circuit.**

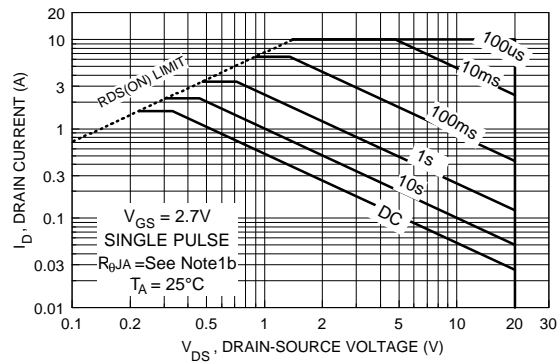


**Figure 12. Switching Waveforms.**

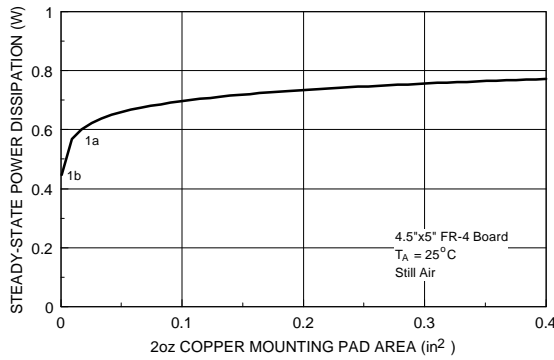
## Typical Electrical Characteristics (continued)



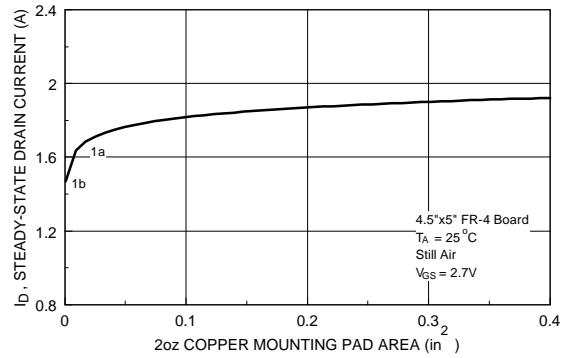
**Figure 13. Transconductance Variation with Drain Current and Temperature.**



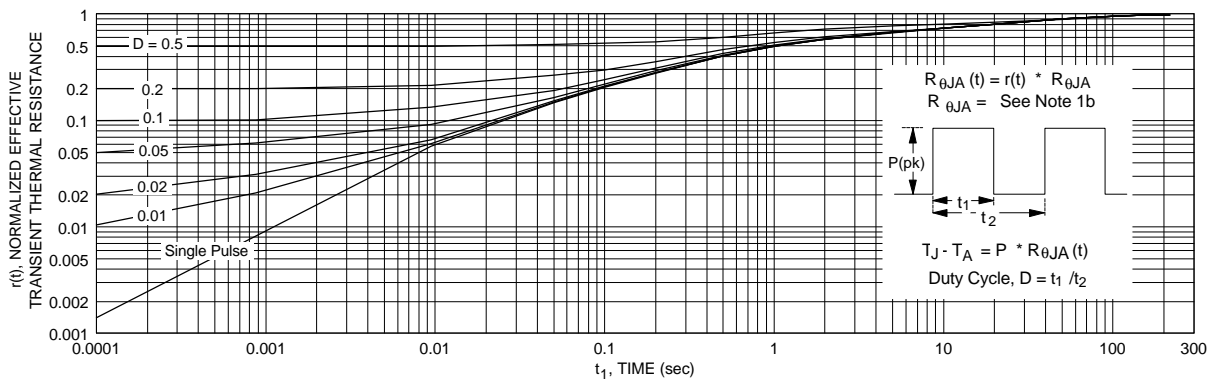
**Figure 14. Maximum Safe Operating Area**



**Figure 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 17. Transient Thermal Response Curve.**

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

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