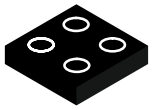
MOSFET – Power, N-Channel, Dual EFCP

12 V, 6 A, 29.5 mΩ

EFC4627R



CSP4 1.01x1.01
CASE 568AK

Features

- 2.5 V Drive
- Protection Diode In
- Common−Drain Type
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- Lithium−ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Value	Unit
Source to Source Voltage	V_{SSS}		12	V
Gate to Source Voltage	V_{GSS}		±10	V
Source Current (DC)	I_S		6	A
Source Current (Pulse)	I_{SP}	PW ≤ 10 μs, Duty Cycle ≤1%	60	A
Total Dissipation	P_T	When mounted on ceramic substrate (5000 mm^2 x 0.8 mm)	1.4	W
Junction Temperature	T_J		150	°C
Storage Temperature	T_{stg}		− 55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

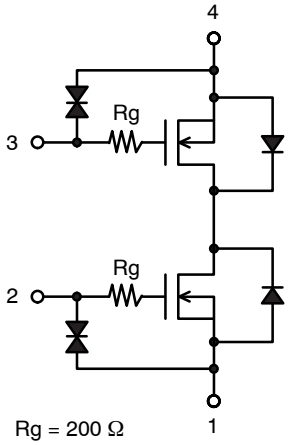
Parameter	Symbol	Value	Unit
Junction to Ambient When mounted on ceramic substrate (5000 mm^2 x 0.8 mm)	$R_{\theta JA}$	84	V

MARKING DIAGRAM



C = Specific Device Code
Y = Year of Production
M = Assembly Operation Month
ZZ = Assembly Lot Number

ELECTRICAL CONNECTION



Rg = 200 Ω

ORDERING INFORMATION

Device	Package	Shipping†
EFC4627R−TR	CSP4 (Pb−Free and Halogen Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V	Test Circuit 1	12	–	–	V
Zero–Gate Voltage Source Current	I_{SSS}	V_{SS} = 10 V, V_{GS} = 0 V	Test Circuit 1	–	–	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V	Test Circuit 2	–	–	±1	μA
Gate Threshold Voltage	V_{GS}(th)	V_{SS} = 6 V, I_S = 1 mA	Test Circuit 3	0.5	–	1.3	V
Forward Transconductance	g_{FS}	V_{SS} = 6 V, I_S = 2 A	Test Circuit 4	–	4.8	–	S
Static Source to Source On–State Resistance	R_{SS}(on)1	I_S = 2 A, V_{GS} = 4.5 V	Test Circuit 5	18.5	23.9	29.5	mΩ
	R_{SS}(on)2	I_S = 2 A, V_{GS} = 4.0 V	Test Circuit 5	19.7	25.4	31.3	mΩ
	R_{SS}(on)3	I_S = 2 A, V_{GS} = 3.8 V	Test Circuit 5	20.3	26.1	32.3	mΩ
	R_{SS}(on)4	I_S = 2 A, V_{GS} = 3.1 V	Test Circuit 5	23.5	30.3	39.0	mΩ
	R_{SS}(on)5	I_S = 2 A, V_{GS} = 2.5 V	Test Circuit 5	29.3	37.7	50.5	mΩ
Turn–On Delay Time	t_d(on)	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 2 A	Test Circuit 6	–	75	–	ns
Rise Time	t_r			–	740	–	ns
Turn–Off Delay Time	t_d(off)			–	2340	–	ns
Fall Time	t_f			–	2320	–	ns
Total Gate Charge	Qg	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 6 A	Test Circuit 7	–	13.4	–	nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V	Test Circuit 8	–	0.76	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test Circuits are Example of Measuring FET1 Side.

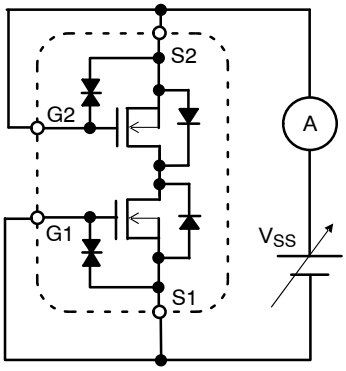
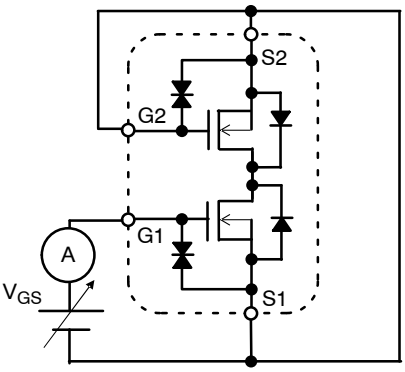


Figure 1. Test Circuit 1 – I_{SSS}



When FET1 is measured, Gate and Source of FET2 are short–circuited.

Figure 2. Test Circuit 2 – I_{GSS}

When FET1 is measured, Gate and Source of FET2 are short–circuited.

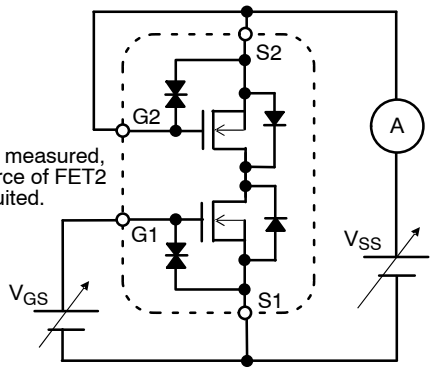
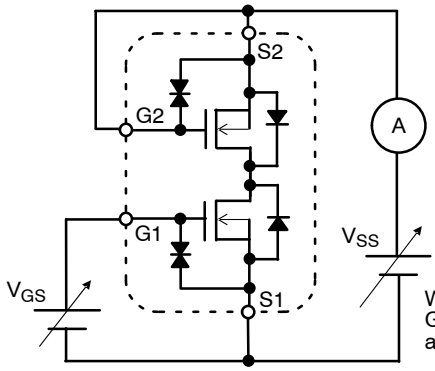


Figure 3. Test Circuit 3 – V_{GS}(th)



When FET1 is measured, Gate and Source of FET2 are short–circuited.

Figure 4. Test Circuit 4 – g_{FS}

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TEST CIRCUITS (continued)

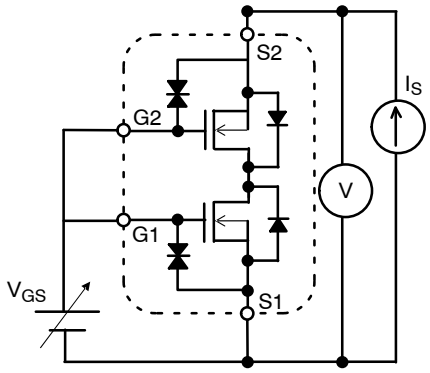
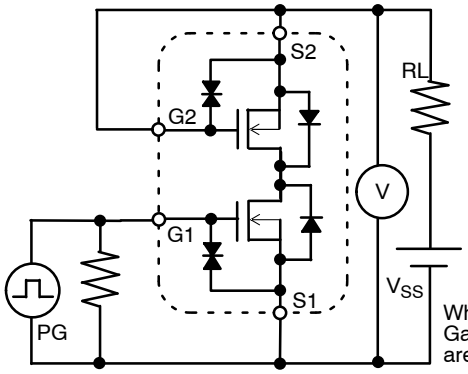


Figure 5. Test Circuit 5 – R_{SS}(on)



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 6. Test Circuit 6 – t_d(on), t_r, t_d(off), t_f

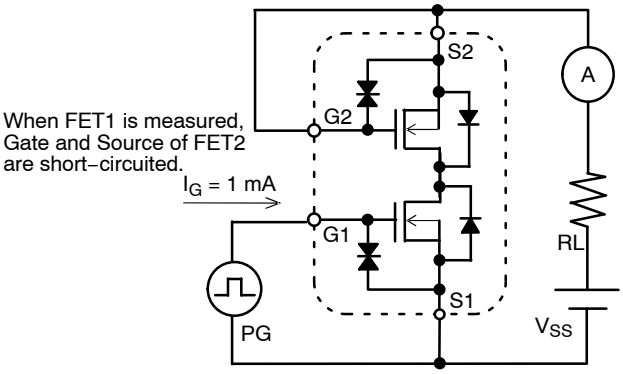
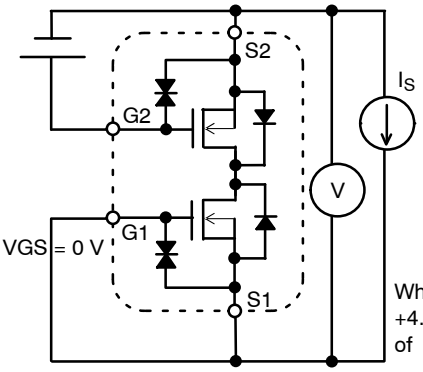


Figure 7. Test Circuit 7 – Qg



When FET1 is measured, +4.5 V is added to V_{GS} of FET2.

Figure 8. Test Circuit 8 – $V_{F(S-S)}$

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

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TYPICAL CHARACTERISTICS

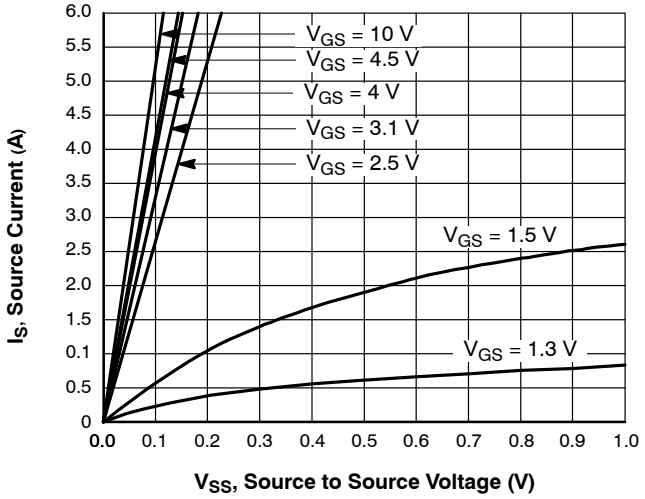


Figure 9. I_S – V_{SS}

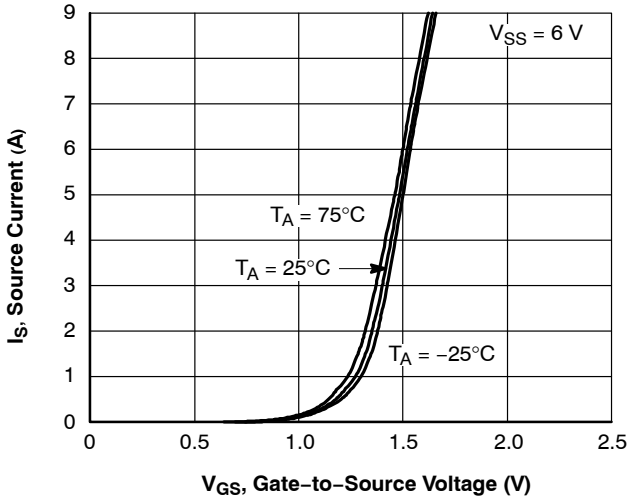


Figure 10. I_S – V_{GS}(th)

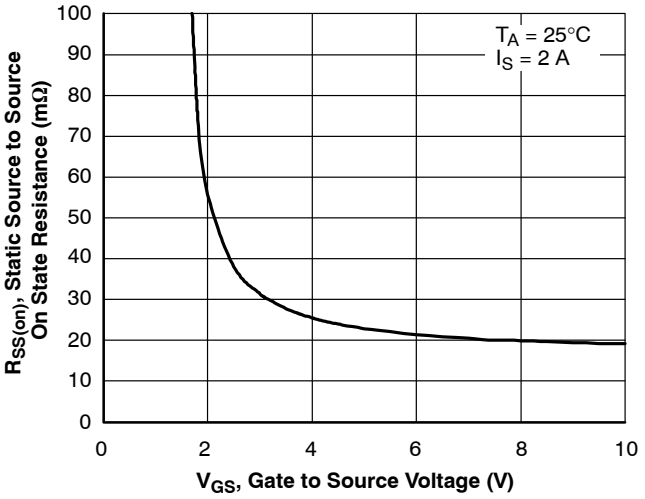


Figure 11. R_{SS}(on) – V_{GS}

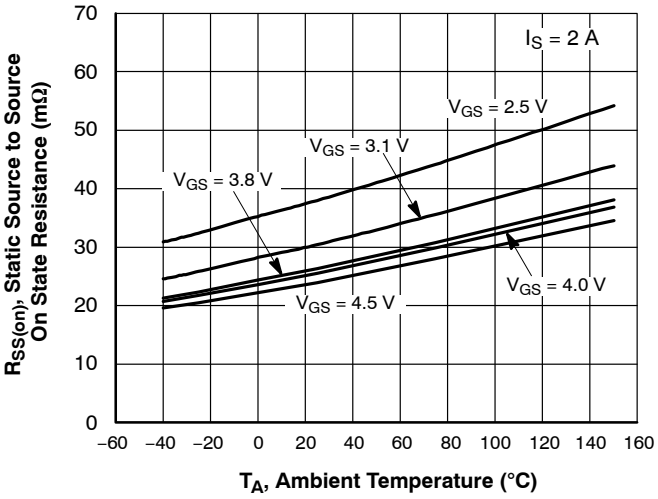


Figure 12. R_{SS}(on) – T_A

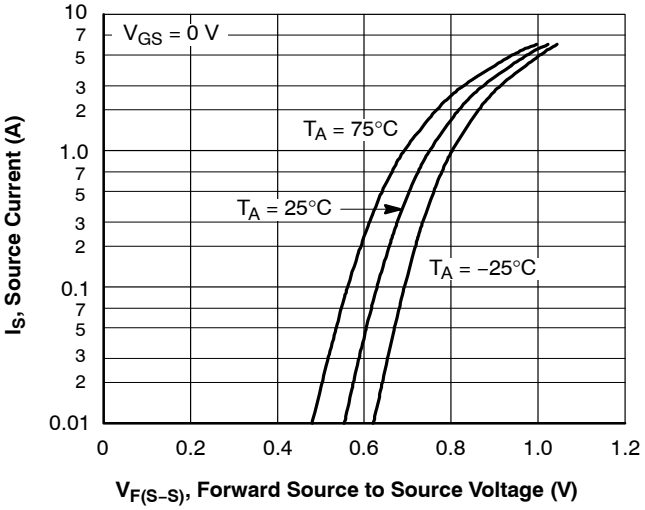


Figure 13. I_S – $V_{F(S-S)}$

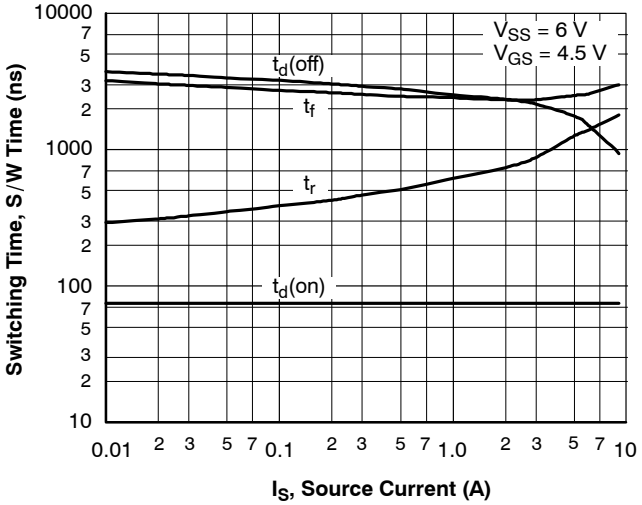


Figure 14. S/W Time – I_S

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TYPICAL CHARACTERISTICS (continued)

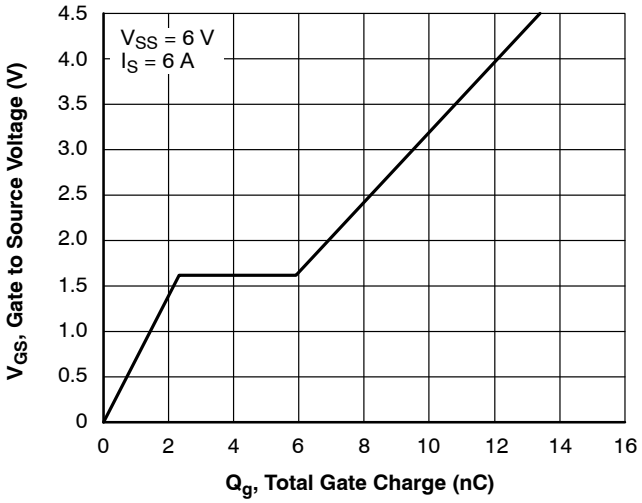


Figure 15. V_{GS} – Q_g

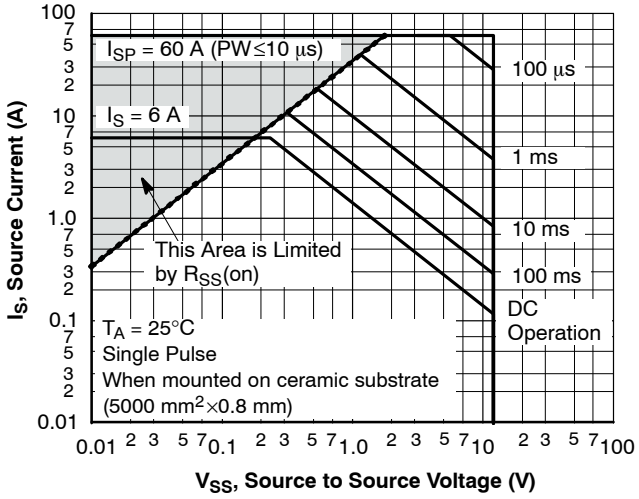


Figure 16. SOA

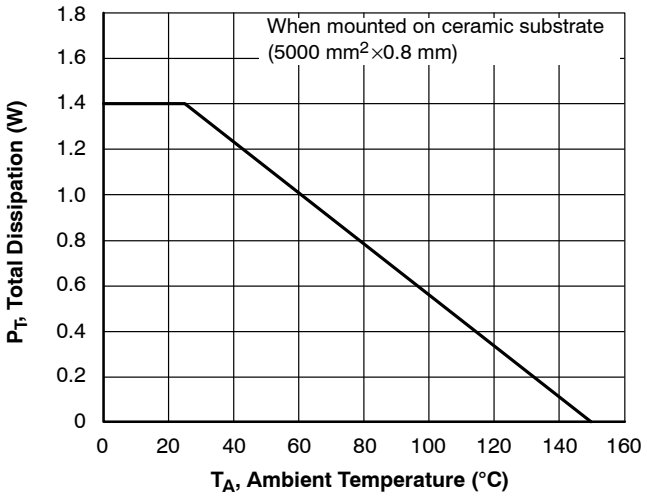


Figure 17. P_T – T_A

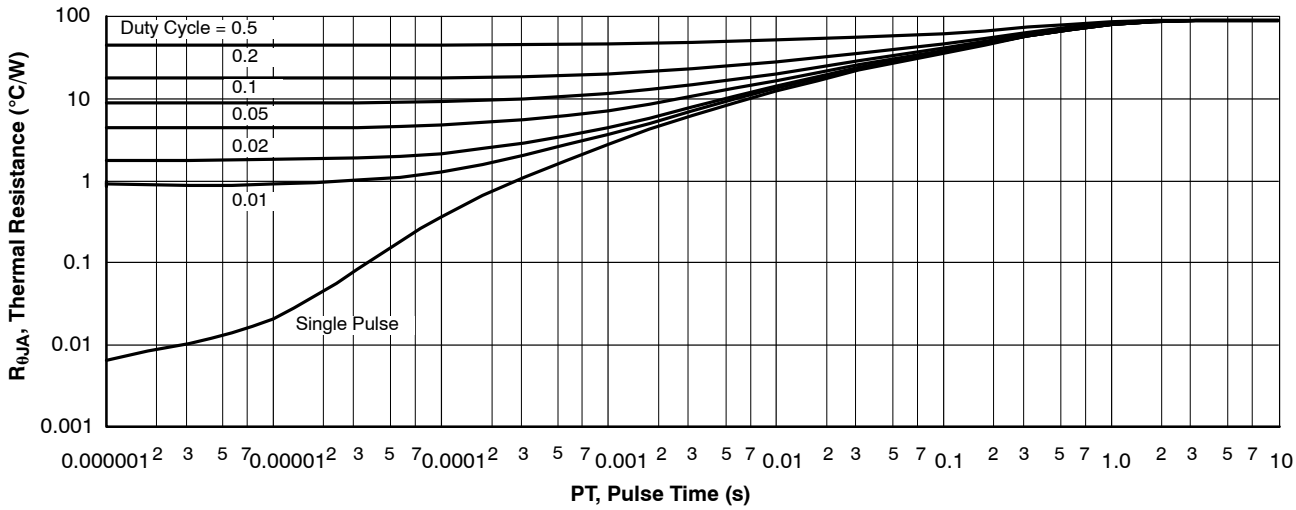


Figure 18. $R_{\theta JA}$ – Pulse Time

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PACKAGE DIMENSION

EFC4627R−TR

(Unit: mm)

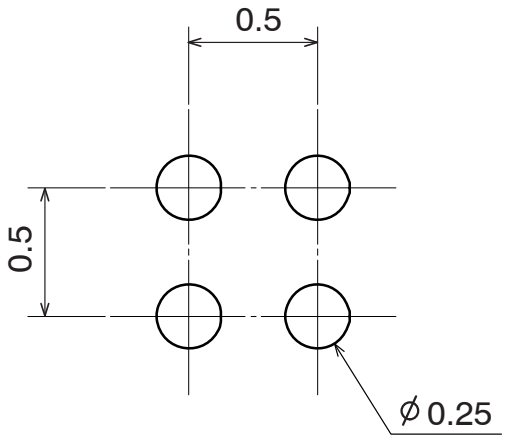


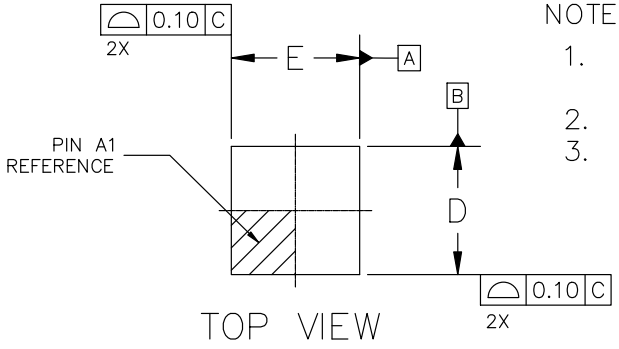
Figure 19. Recommended Soldering Footprint

Note on usage: Since the EFC4627R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

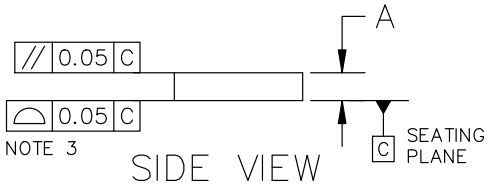
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WLCSP4, 1.01x1.01x0.20, 0.50P
CASE 568AK
ISSUE C

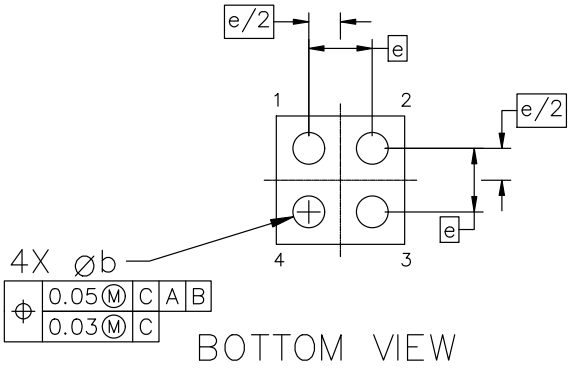
DATE 05 NOV 2024



TOP VIEW



SIDE VIEW

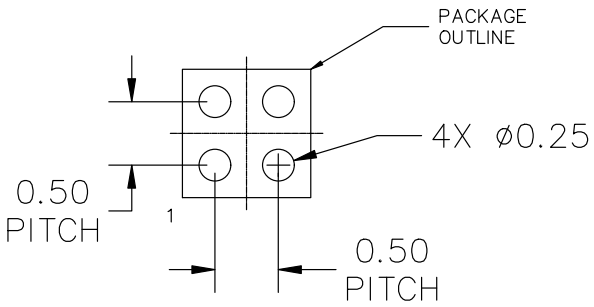


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.18	0.20	0.22
b	0.22	0.25	0.28
D	0.99	1.01	1.11
E	0.99	1.01	1.11
e	0.50 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques References manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP4, 1.01x1.01x0.20, 0.50P**	**PAGE 1 OF 1**

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