AW-NM288SM

IEEE 802.11 b/g/n Wireless LAN Stamp Module

Datasheet

Version 0.5

Revision History

Document release	Date	Modification	Initials	Approved
Version 0.1	2016/04/22	Initial Version	N.C. Chen	Chihhao Liao
Version 0.2	2016/06/06	Update 1-4. Specifications Table	N.C. Chen	Chihhao Liao
Version 0.3	2016/08/08	Update 1-4. Specifications Table Electrical Specifications	N.C. Chen	Chihhao Liao
Version 0.4	2016/08/26	Update SDIO Host Interface SPECIFICATION Remove gSPI description	N.C. Chen	Chihhao Liao
Version 0.5	2016/07/18	Update IC P/N from CYW43362 to CYW43362	N.C. Chen	Chihhao Liao

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1.General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the advanced **IEEE 802.11 b/g/n WLAN** module - **AW-NM288SM.** The module is targeted to mobile and embedded devices which need small footprint package, low power consumption, and multiple OS support. The module supports **2.4GHz** IEEE 802.11n MAC/baseband/radio. It also features an integrated Power Management Unit (PMU), Power Amplifiers (PAs), and a Low Noise Amplifier (LNA) to address the needs of mobile devices that require minimal power consumption and compact size.

By using AW-NM288SM, the customers can easily enable the Wi-Fi embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.** Specified in the IEEE 802.11 standard minimize the system power requirements by using AW-NM288SM. In addition to the support of **WPA/WPA2 (personal)** and **WEP** encryption, the AW-NM288SM also supports the IEEE 802.11i security standard through **AES** and **TKIP** acceleration hardware for faster data encryption. For the video, voice and multimedia applications the AW-NM288SM support 802.11e Quality of Service (QoS). The host interface is **SDIO v2.0** interface.

1-2. Key Features

1-2-1. General

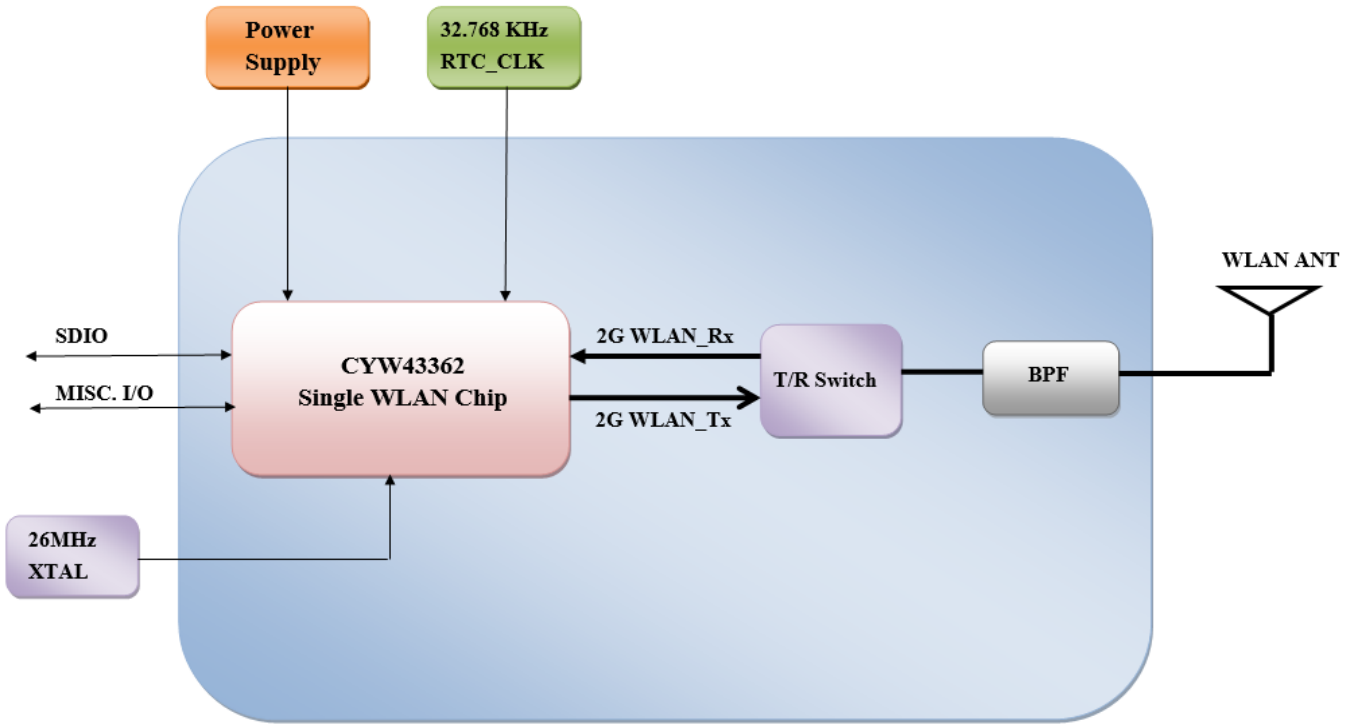
- **Integrates Cypress solutions of AW-NM288SM single-band 2.4GHz IEEE 802.11 b/g/n SoC**
- **SDIO v2.0 interfaces support for WLAN**
- **Lead-free / Halogen Free Design**
- **12.0mm(L) x 12.0mm(W) x 1.5 mm(H) 44 pin LGA package**
- **Without Crystal(XTAL)**

1-2-2. WLAN Section

- **Integrated WLAN CMOS power amplifier with internal power detector**
- **Support internal fractional-N PLL enables the use of a wide range of reference clock frequencies.**
- **Supports antenna diversity**
- **Supports IEEE 802.11d, h, i, j,**
- **Security–WPA/WPA2 (personal), AES (HW), TKIP (HW), CKIP (SW).**
- **WMM, QoS, WMM-PS**
- **Proprietary protocol –CCXv2/CCXv3/CCXv4/CCXv5, WFAEC**
- **Integrated CPU with on-chip memory for a complete WLAN subsystem minimizing the need to wake up the applications processor**

1-3. Block Diagram

A simplified block diagram of the AW-NM288SM module is depicted in the figure below.



AW-NM288SM BLOCK DIAGRAM

1-4. Specifications Table

Model Name	AW-NM288SM
Product Description	**IEEE 802.11 b/g/n Wireless LAN Stamp Module**
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant
Host Interface	WLAN: SDIO v2.0
Major Chipset	CYW43362
Dimension	12.0mm(L) x 12.0mm(W) x 1.5 mm(H)
Weight	TBD
Package	44 pin Stamp Module
Operating Conditions	
Voltage	Input supply voltage for VBAT: 2.3 ~4.8V Input supply for host I/O : 1.71 ~3.63V
Temperature	Operating: -30~85 °C ; Storage: -40~85 °C
Relative Humidity	< 60 % (storage) <85% (operation)
Electrical Specifications	
Frequency Range	WLAN: 2.4 GHz Band
Number of Channels	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 Japan – 1 ~ 14 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13 802.11n: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13
Modulation	WLAN: DSSS, OFDM, BPSK(9/6Mbps), QPSK(18/12Mbps), DBPSK(1Mbps), DQPSK(2Mbps), CCK(11/5.5Mbps), 16-QAM(36/24Mbps), 64-QAM (72.2/54/48Mbps)
Output Power	WLAN: 11b: 16 dBm (± 2dBm) @EVM<35% 11g: 15 dBm (± 2dBm) @EVM≦ -25 dB 11n_HT20: 14 dBm (± 2dBm) @EVM≦ -28 dB
Receive Sensitivity	WLAN: 11b (11Mbps): -82 dBm (Typical) 11g (54Mbps): -70 dBm (Typical) 11n (HT20 MCS7): -67 dBm (Typical)

Data Rates	**WLAN:** **802.11b: 1, 2, 5.5, 11Mbps** **802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps** **802.11n:MCS 0~7 HT20**
Operating Range	**TBD**
Security	◆ **WPA™- and WPA2™- (Personal) support for powerful encryption and authentication** ◆ **AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility** ◆ **Cisco® Compatible Extension- (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX5.0) certified** ◆ **Wi-Fi Protected Setup (WPS)** ◆ **WEP** ◆ **WMM / WMM-SA** ◆ **CKIP(Software)**
ESD test condition	**ESD:HBM +/-1.25KV** **CDM+/-175V** **MM +/- 50V**
Operating System Compatibility	

2. Electrical Characteristics

2-1. Recommended Operating Conditions

Symbol	Parameter	Type	Min	Typ	Max	Units
VBAT	Power supply for Internal Regulators and FEM	Input	2.3	3.3	4.8	V

2-2. DC Characteristics for Host I/O

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SDIO Interface I/O pins						
V_{IH}	Input high voltage (V_{DDIO})	VDDIO_SD=3.3V	2.0	-	3.3	
V_{IL}	Input low voltage (V_{DDIO})	VDDIO_SD=3.3V	-	-	0.8	
V_{OH}	Output High Voltage @ 2mA	VDDIO_SD=3.3V	VDDIO-0.4V	-	-	
V_{OL}	Output Low Voltage @ 2mA	VDDIO_SD=3.3V	-	-	0.4	
Other Digital I/O pins						
V_{IH}	Input high voltage (V_{DDIO})	VDDIO=3.3V	2.0	-	VDDIO	
V_{IL}	Input low voltage (V_{DDIO})	VDDIO=3.3V	-	-	0.8	
V_{OH}	Output High Voltage @ 2mA	VDDIO=3.3V	VDDIO-0.4V	-	-	
V_{OL}	Output Low Voltage @ 2mA	VDDIO=3.3V	-	-	0.4	

2-3. WLAN Interface Specification

2-3-1. SDIO 2.0

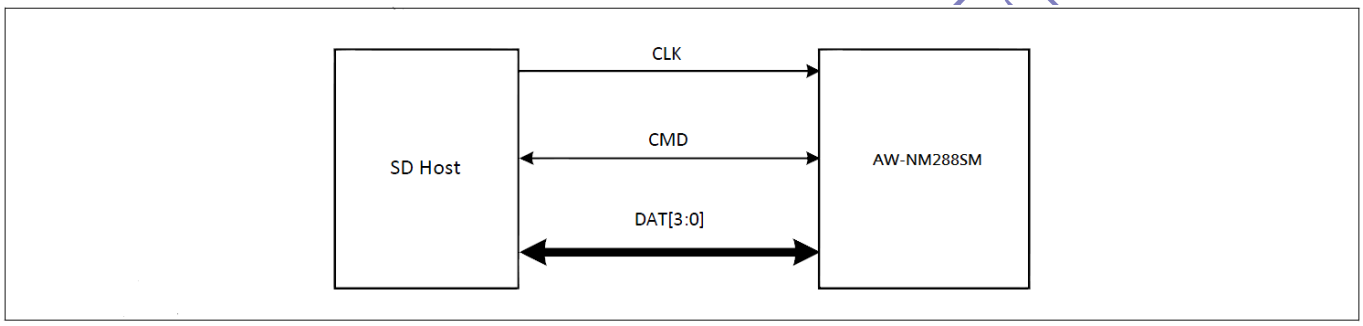
The AW-NM288SM WLAN section supports SDIO version 2.0 for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks — 200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided. SDIO mode is enabled using the strapping option pins. See Table 10 on page 56 for details.

Three functions are supported:

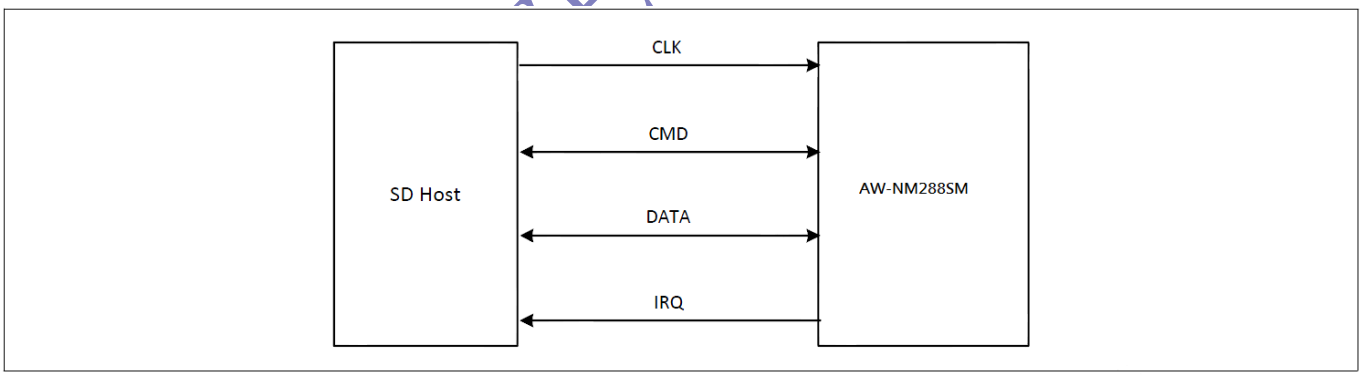
- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used
DATA3	Data line 3	NC	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

SDIO Pin Descriptions



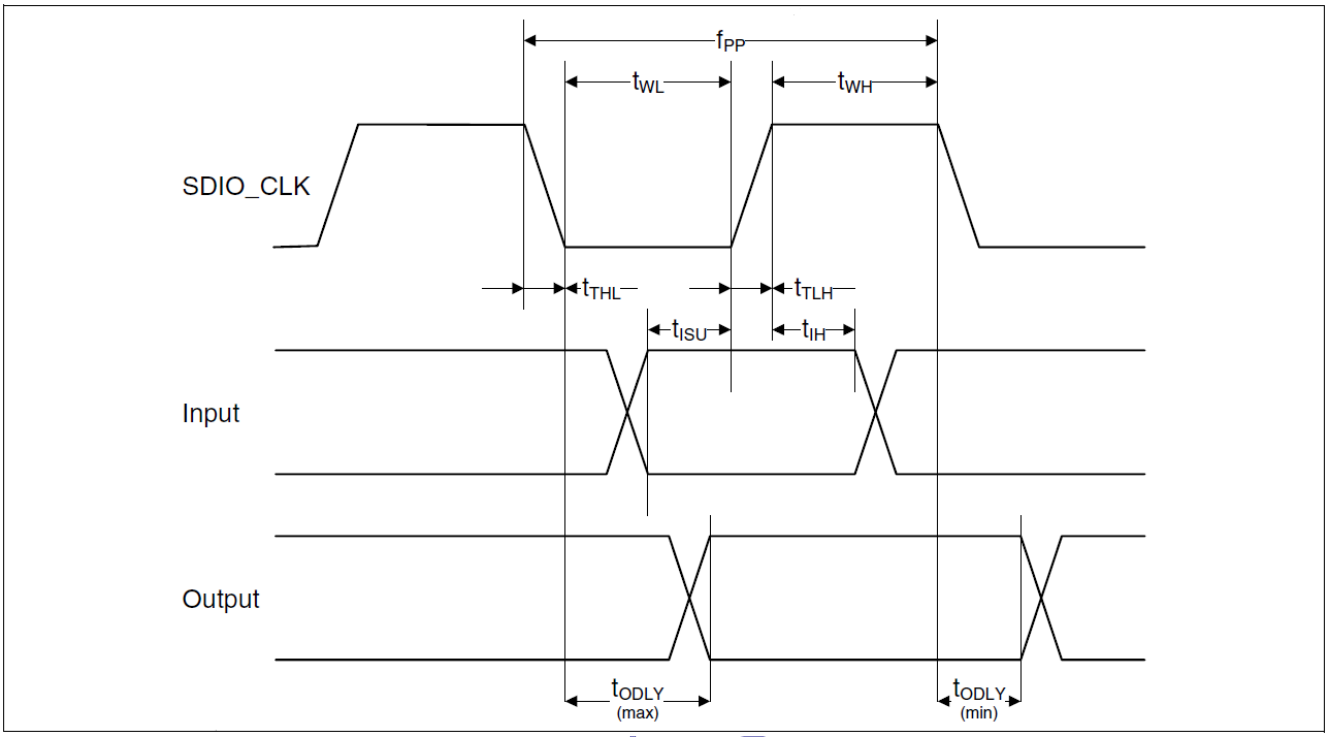
Single Connections to SDIO Host (SD 4-Bit Mode)



Signal Connections to SDIO Host (SD 1-Bit Mode)

2-4. Interface Timing

SDIO Default Mode Timing

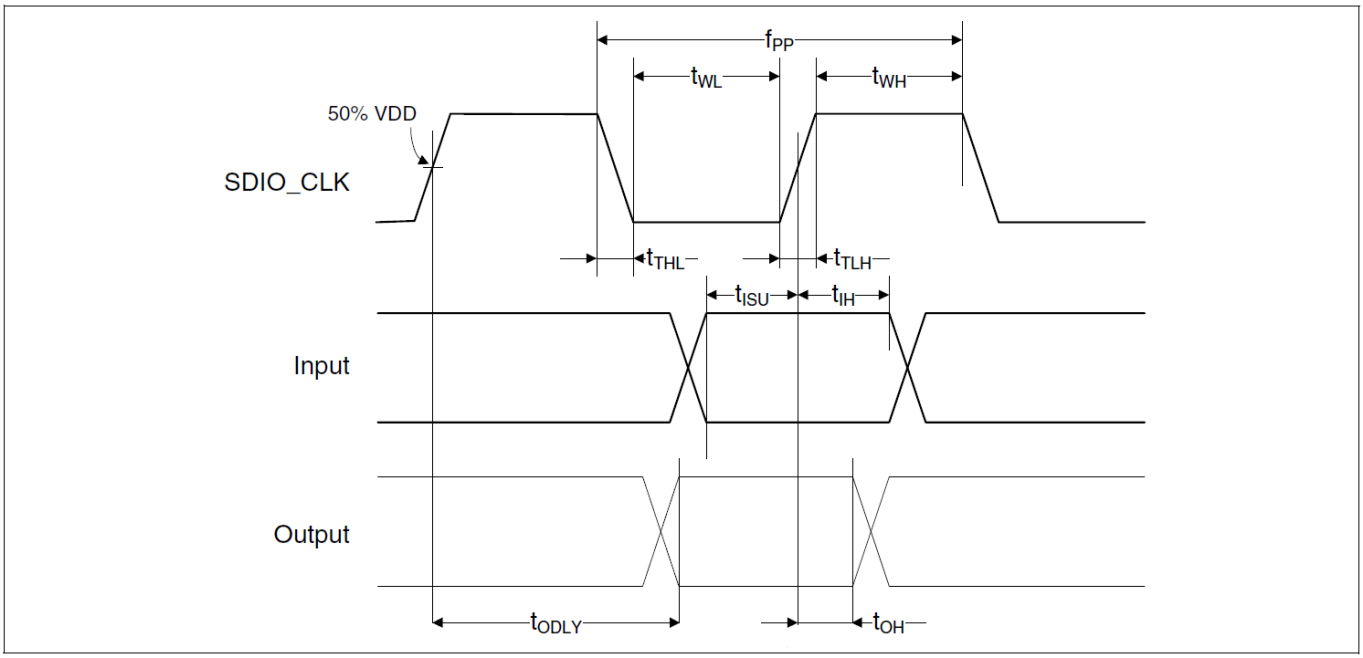


SDIO Bus Timing (Default Mode)

SDIO Bus Timing Parameters (Default Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency — Data Transfer mode	fPP	0	–	25	MHz
Frequency — Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock fall time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time — Data Transfer mode	tODLY	0		14	ns
Output delay time — Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.



SDIO Bus Timing (High-Speed Mode)

SDIO Bus Timing Parameters (High-Speed Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

2-5. Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

External 32.768KHz Low-Power Oscillator

The AW-NM288SM uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 3.

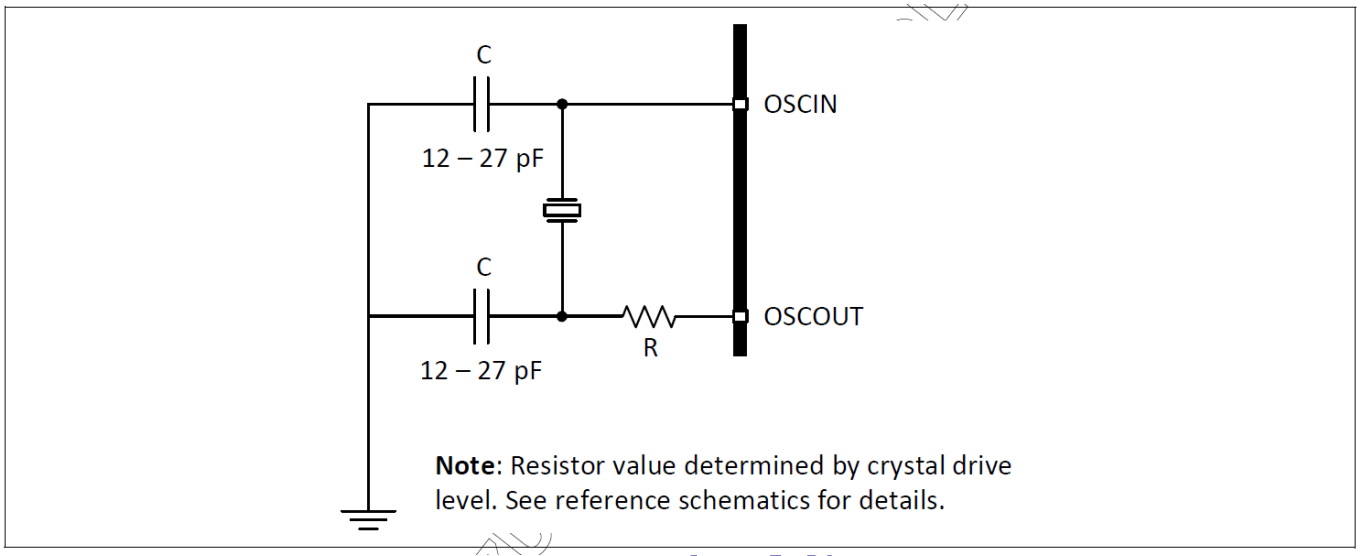
Note: The AW-NM288SM will auto-detect the LPO clock. If it senses a clock on the EXT_SLEEP_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT_SLEEP_CLK to ground. Do not leave this pin floating.
- To use an external LPO: Connect the external 32.768 kHz clock to EXT_SLEEP_CLK.

			Specification			
Symbol	***Parameter***	***Condition/Notes***	***Minimum***	***Typical***	***Maximum***	***Units***
Fr	Frequency	–	–	32768	–	Hz
Δf/fr	Frequency tolerance	At 25°C	−30	–	+30	ppm
		−20°C <Ta< +70°C	−150	–	+40	
		−30°C <Ta< +85°C	−220	–	+40	
Duty cycle	–	–	30	–	70	%
Vol	Output low voltage	–	0	–	0.2	V
Voh	Output high voltage	–	0.7 Vio	–	Vio	V
Tr/Tf	Rise and fall time	–	–	–	100	ns
–	Signal type	Digital	–	–	–	–
–	Clock jitter	Integrated over 300 Hz to 15 kHz	–	–	30	ns
–	Input impedance	Resistive	10	–	–	MΩ
		Capacitive	–	–	2	pF
–	Input amplitude	Fail safe, 3.3V digital I/O	–	–	3.63	V

Crystal Interface and Clock Generation

The AW-NM288SM can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 4. Consult the reference schematics for the latest configuration.



The AW-NM288SM uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing. This enables it to operate using numerous frequency references. This may either be an external source such as a crystal interfaced directly to the AW-NM288SM.

The default frequency reference setting is a 26 MHz crystal. The signal requirements and characteristics for the crystal interface are shown on page 17.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min	Typ	Max	Min	Typ	Max	
Frequency	–		26 MHz					
Crystal load capacitance	–	–	12	–				pF
ESR	–	–	–	60				Ω
Input Impedance (OSCIN)[b]	Resistive				30k	100k	–	Ω
	Capacitive				–	–	7.5	pF
Input Impedance (WRF_TCXO_IN)	Resistive				30k	100k	–	Ω
	Capacitive				–	–	4	pF
OSCIN input voltage	AC-coupled analog signal				400	–	1200	mV_{p-p}
OSCIN input low level	DC-coupled digital signal				0	–	0.2	V
OSCIN input high level	DC-coupled digital signal				1.0	–	1.36	V
WRF_TCXO_IN input voltage	DC-coupled analog signal[c]				400	–	TCXO VDD[d]	mV_{p-p}
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm
Duty cycle	26 MHz clock				40	50	60	%
Phase Noise[e, f] (IEEE 802.11 b/g)	26 MHz clock at 1 kHz offset				–	–	–119	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	–129	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	–134	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	–139	dBc/Hz
Phase Noise[e, f] (IEEE 802.11n, 2.4 GHz)	26 MHz clock at 1 kHz offset				–	–	–124	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	–134	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	–139	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	–144	dBc/Hz

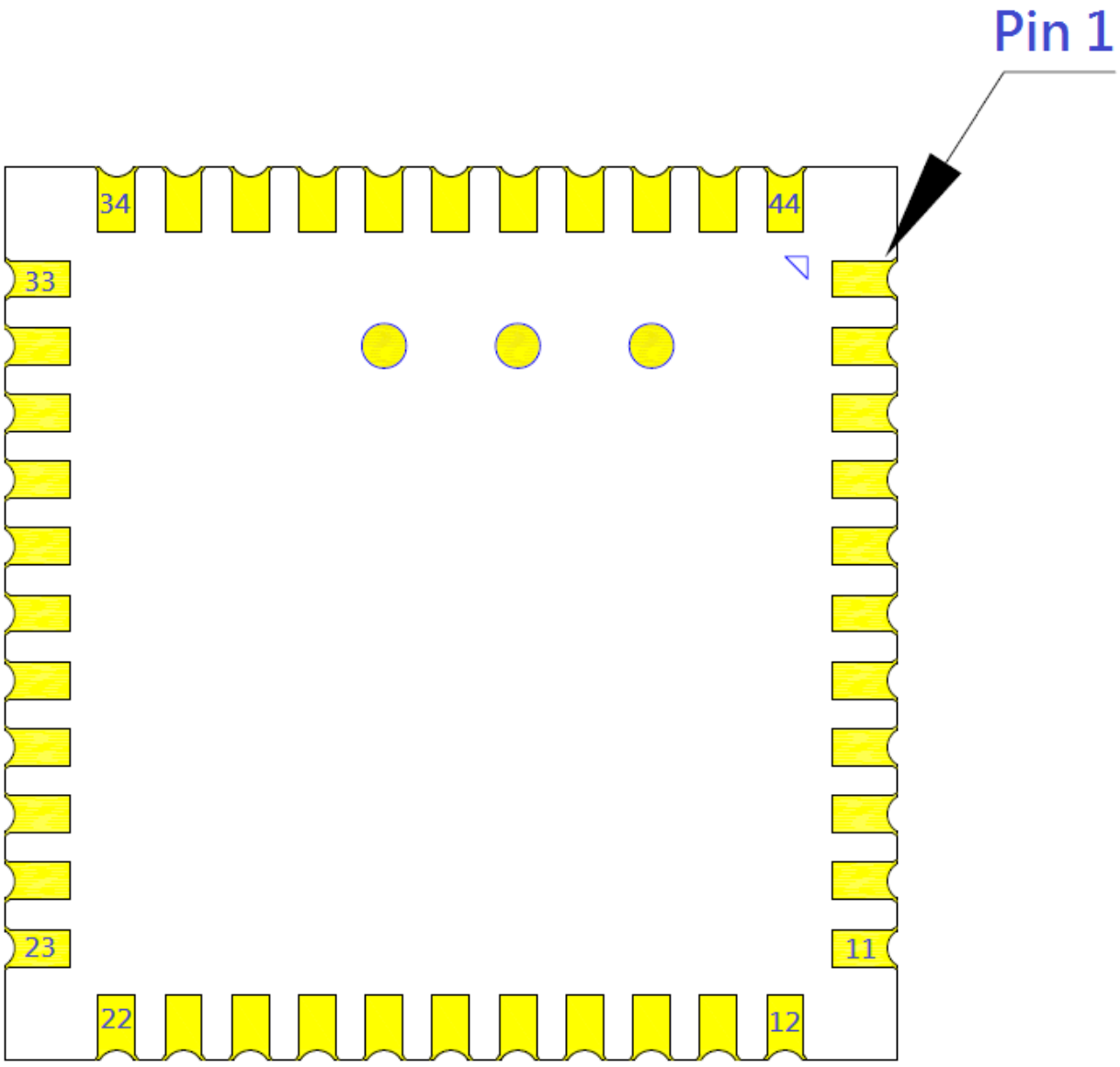
3. Pin Definition

Note: The pin name and direction are defined on module side.

Pin No	Definition	Basic Description	Type
1	GND	Ground.	GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.	I/O
3	GND	Ground.	GND
4	NC	Floating Pin, No connect to anything.	Floating
5	NC	Floating Pin, No connect to anything.	Floating
6	NC	Floating Pin, No connect to anything.	Floating
7	NC	Floating Pin, No connect to anything.	Floating
8	NC	Floating Pin, No connect to anything.	Floating
9	VBAT	3.3V power pin	VCC
10	XTAL_IN	Crystal Input	I
11	XTAL_OUT	Crystal Output	O
12	WL_DIS#	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	I
13	WL_DEV_WAKE_HOST	WL Host Wake	O
14	SDIO_D2	SDIO Data Line 2	I/O
15	SDIO_D3	SDIO Data Line 3	I/O
16	SDIO_CMD	SDIO Command Input	I/O
17	SDIO_CLK	SDIO Clock Input	I
18	SDIO_D0	SDIO Data Line 0	I/O
19	SDIO_D1	SDIO Data Line 1	I/O
20	GND	Ground.	GND
21	VIN_LDO_OUT	Internal Buck 1.2V voltage generation pin	VCC
22	VDDIO	1.8V-3.3V VDDIO supply for WLAN and BT	VCC
23	VIN_LDO	Internal Buck 1.2V voltage generation pin	VCC
24	SUSCLK_IN	External 32K or RTC clock	I
25	NC	Floating Pin, No connect to anything.	Floating
26	NC	Floating Pin, No connect to anything.	Floating

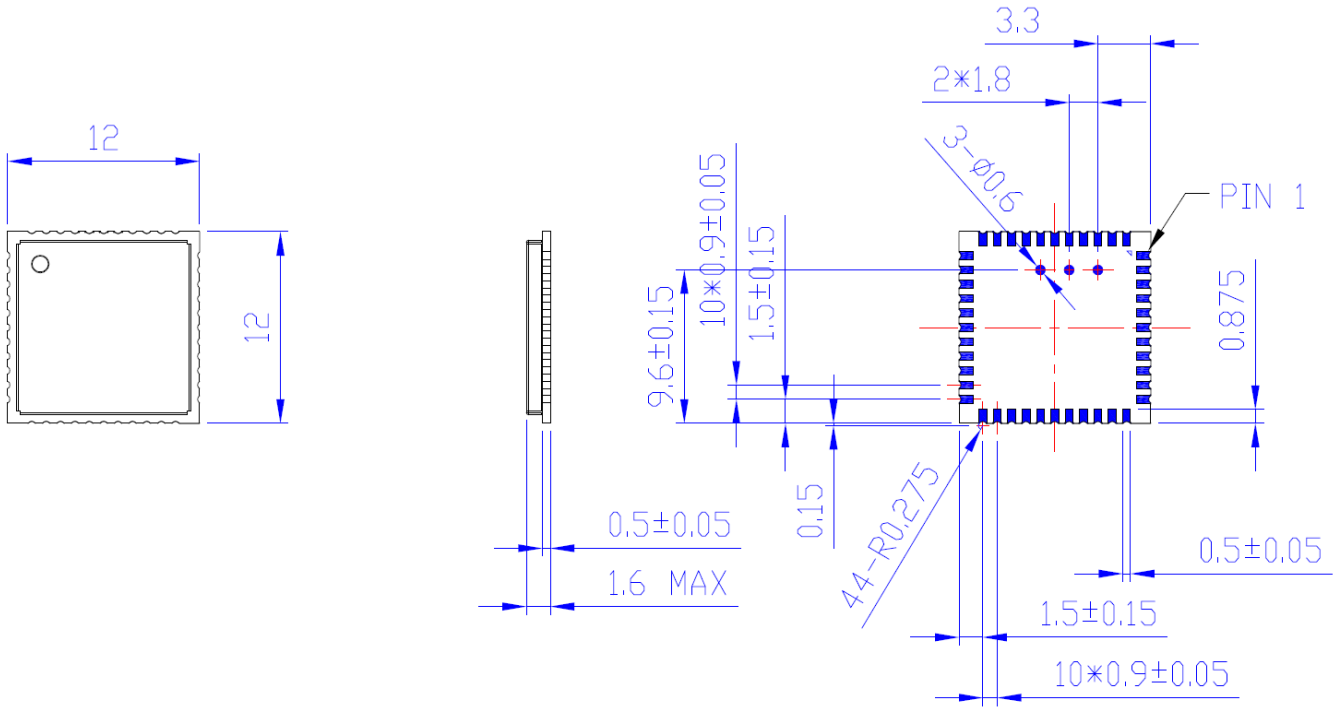
27	NC	Floating Pin, No connect to anything.	Floating
28	NC	Floating Pin, No connect to anything.	Floating
29	NC	Floating Pin, No connect to anything.	Floating
30	NC	Floating Pin, No connect to anything.	Floating
31	GND	Ground.	GND
32	NC	Floating Pin, No connect to anything.	Floating
33	GND	Ground.	GND
34	NC	Floating Pin, No connect to anything.	Floating
35	NC	Floating Pin, No connect to anything.	Floating
36	GND	Ground.	GND
37	NC	Floating Pin, No connect to anything.	Floating
38	NC	Floating Pin, No connect to anything.	Floating
39	NC	Floating Pin, No connect to anything.	Floating
40	NC	Floating Pin, No connect to anything.	Floating
41	NC	Floating Pin, No connect to anything.	Floating
42	NC	Floating Pin, No connect to anything.	Floating
43	NC	Floating Pin, No connect to anything.	Floating
44	NC	Floating Pin, No connect to anything.	Floating
45	TP3(NC)	Floating Pin, No connect to anything.	Floating
46	TP3(NC)	Floating Pin, No connect to anything.	Floating
47	TP3(NC)	Floating Pin, No connect to anything.	Floating

3-1. Pin Map



AW-NM288SM Bottom View Pin Map

4. Mechanical Information



Tolerances unless otherwise specified : ±0.15mm