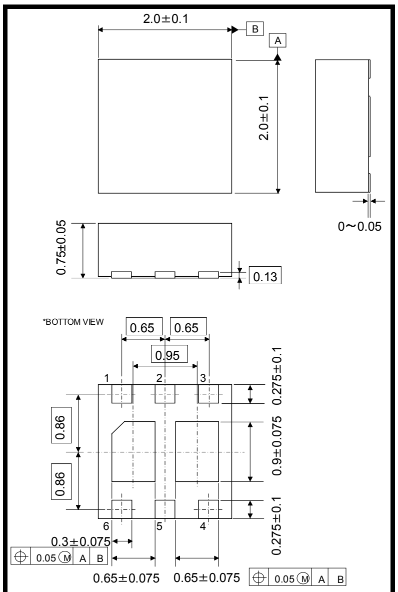
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOS VI)

SSM6P47NU

Power Management Switch Applications

Unit: mm



1. Source1
2. Gate1
3. Drain2
4. Source2
5. Gate2
6. Drain1

UDFN6	
JEDEC	―
JEITA	―
TOSHIBA	2-2Y1A

Weight: 8.5 mg (typ.)

- 1.5V drive
- Low ON-resistance: $R_{DS(on)}$ = 242 mΩ (max) (@V_{GS} = -1.5 V)
  $R_{DS(on)}$ = 170 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(on)}$ = 125 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(on)}$ = 95 mΩ (max) (@V_{GS} = -4.5 V)

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

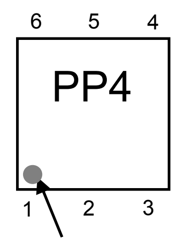
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	−20	V
Gate-Source voltage		V_{GSS}	±8	V
Drain current	DC	I_D	−4.0	A
	Pulse	I_{DP} (Note 1)	−8.0	
Power dissipation (Note 2)		P_D	1	W
		t < 10s	2	
Channel temperature		Tch	150	°C
Storage temperature		T_{stg}	−55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150 °C during use.

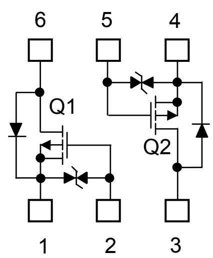
Note 2: Total rating
Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking(Top View)

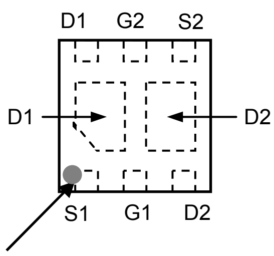


Polarity marking

Equivalent Circuit(Top View)



Pin Condition(Top View)



Polarity marking (on the top)
*Electrodes : on the bottom

Start of commercial production
2010-06

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

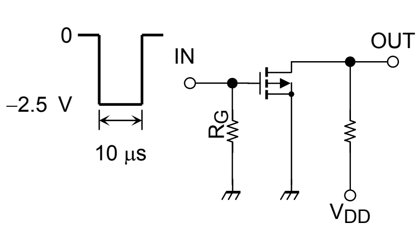
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	$V_{(BR)\ DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
	$V_{(BR)\ DSX}$	I_D = -1 mA, V_{GS} = 5 V (Note 4)	-15	—	—	
Drain cut-off current	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	μA
Gate leakage current	I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage	V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -1.0 A (Note 3)	2.8	5.6	—	S
Drain–source ON-resistance	$R_{DS\ (ON)}$	I_D = -1.5 A, V_{GS} = -4.5 V (Note 3)	—	80.5	95	mΩ
		I_D = -1.0 A, V_{GS} = -2.5 V (Note 3)	—	99.5	125	
		I_D = -0.5 A, V_{GS} = -1.8 V (Note 3)	—	122	170	
		I_D = -0.25 A, V_{GS} = -1.5 V (Note 3)	—	143	242	
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	290	—	pF
Output capacitance	C_{oss}		—	44	—	
Reverse transfer capacitance	C_{rss}		—	32	—	
Total Gate Charge	Q_g	V_{DD} = –10 V, I_D = –3.5 A, V_{GS} = –4.5 V	—	4.6	—	nC
Gate-Source Charge	Q_{gs1}		—	0.5	—	
Gate-Drain Charge	Q_{gd}		—	1.2	—	
Switching time: Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -0.5 A, V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω	—	12.0	—	ns
Switching time: Turn-off time	t_{off}		—	46.2	—	
Drain-Source forward voltage	V_{DSF}	I_D = 4.0 A, V_{GS} = 0 V (Note 3)	—	0.9	1.2	V

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

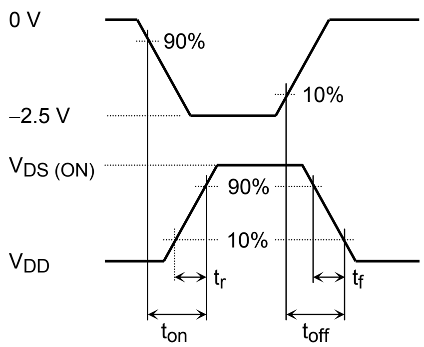
(a) Test circuit



V_{DD} = –10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Notice on Usage

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM6P47NU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

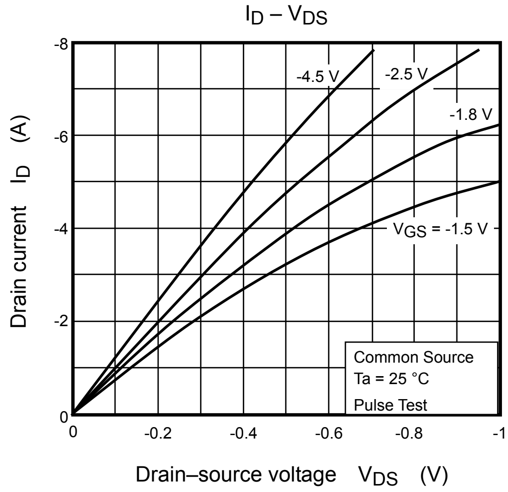
Take this into consideration when using the device.

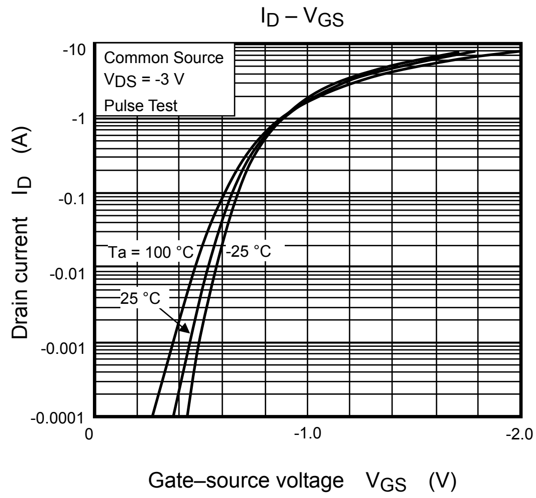
Handling Precaution

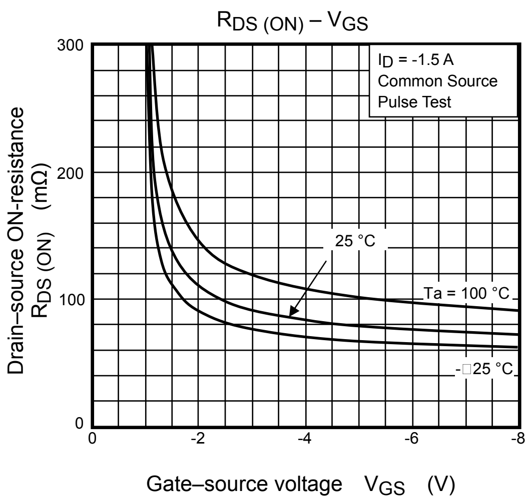
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

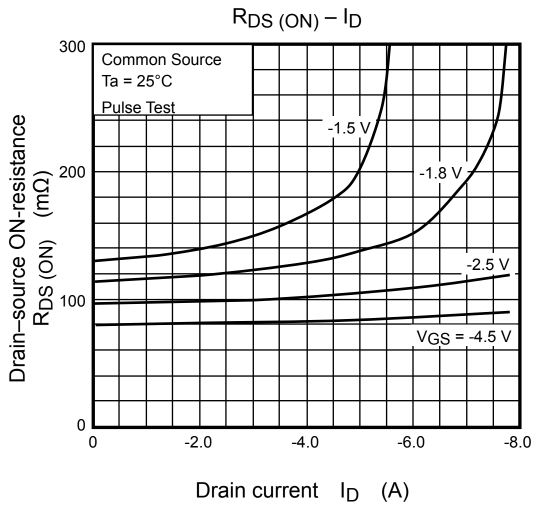
Thermal resistance $R_{th\ (ch\text{-}a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

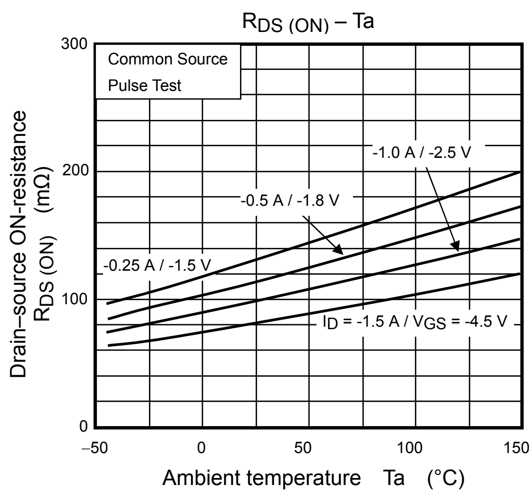
(Q1, Q2 Common)

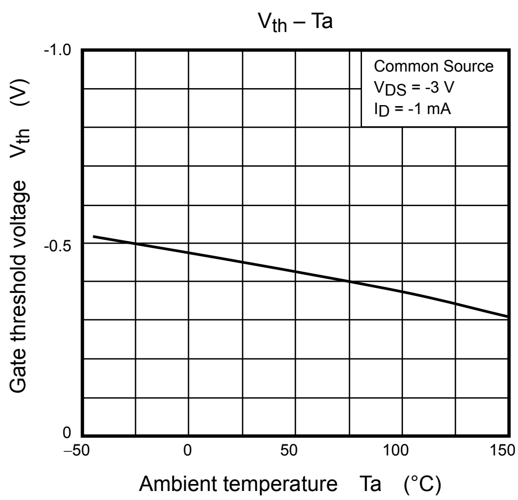

I_D – V_{DS}
Drain current I_D (A)
Drain–source voltage V_{DS} (V)
-8
-6
-4
-2
0
-0.2
-0.4
-0.6
-0.8
-1
-4.5 V
-2.5 V
-1.8 V
V_{GS} = -1.5 V
Common Source
Ta = 25 °C
Pulse Test


I_D – V_{GS}
Drain current I_D (A)
Gate–source voltage V_{GS} (V)
-10
-1
-0.1
-0.01
-0.001
-0.0001
0
-1.0
-2.0
Common Source
V_{DS} = -3 V
Pulse Test
Ta = 100 °C
-25 °C
25 °C

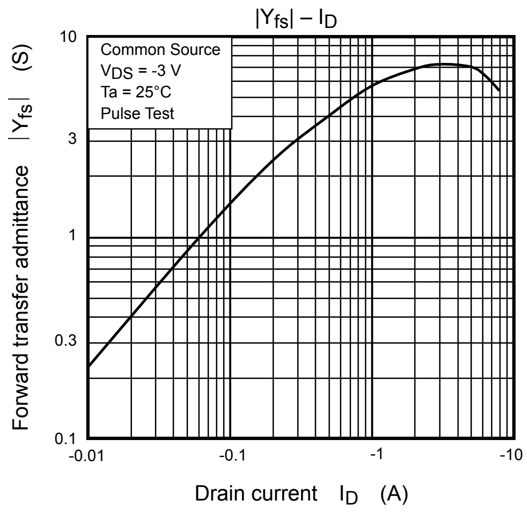

$R_{DS (ON)}$ – V_{GS}
Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)
Gate–source voltage V_{GS} (V)
300
200
100
0
-2
-4
-6
-8
I_D = -1.5 A
Common Source
Pulse Test
25 °C
Ta = 100 °C
-25 °C

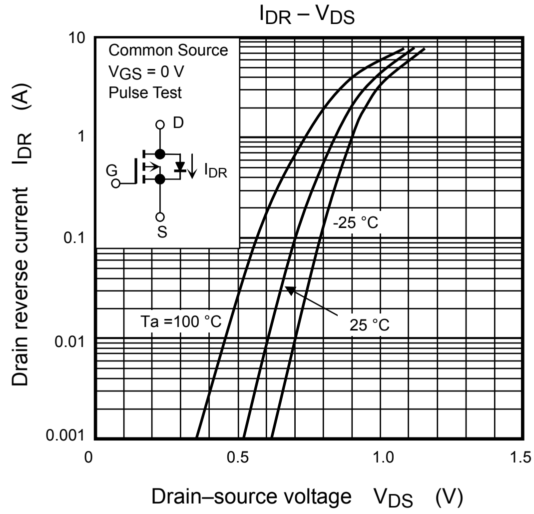

$R_{DS (ON)}$ – I_D
Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)
Drain current I_D (A)
300
200
100
0
-2.0
-4.0
-6.0
-8.0
Common Source
Ta = 25°C
Pulse Test
-1.5 V
-1.8 V
-2.5 V
V_{GS} = -4.5 V

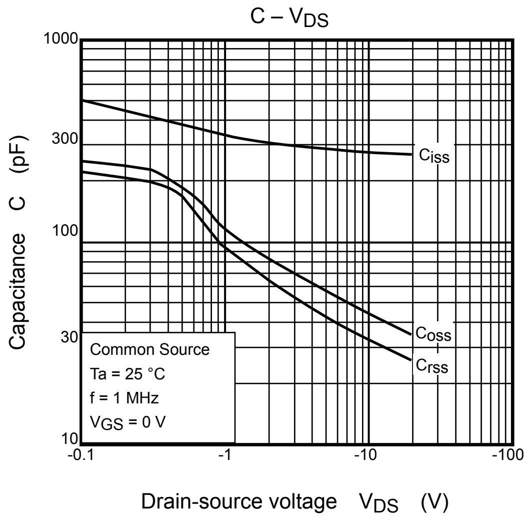

$R_{DS (ON)}$ – Ta
Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)
Ambient temperature Ta (°C)
300
200
100
0
–50
50
100
150
Common Source
Pulse Test
-1.0 A / -2.5 V
-0.5 A / -1.8 V
-0.25 A / -1.5 V
I_D = -1.5 A / V_{GS} = -4.5 V

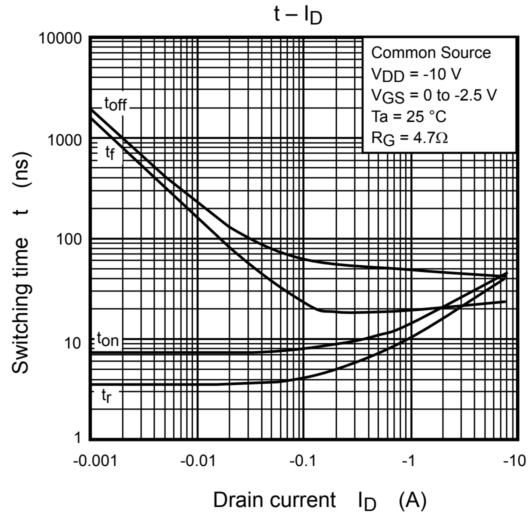

V_{th} – Ta
Gate threshold voltage V_{th} (V)
Ambient temperature Ta (°C)
-1.0
-0.5
0
–50
50
100
150
Common Source
V_{DS} = -3 V
I_D = -1 mA

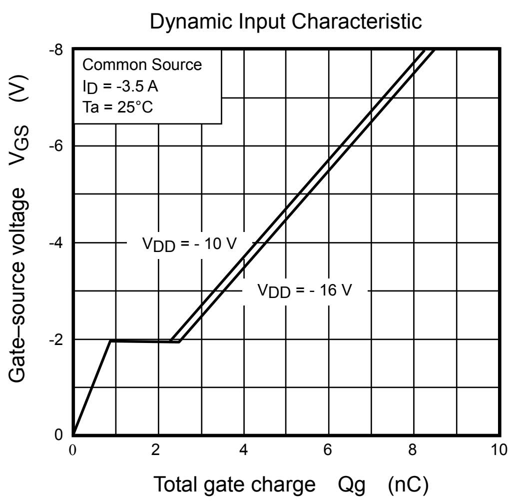
(Q1, Q2 Common)

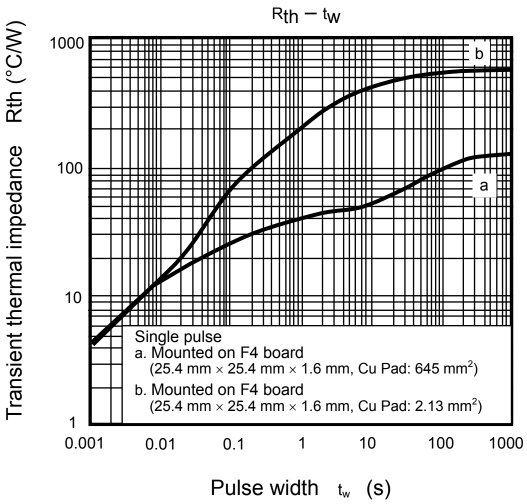

|Yfs| – ID
Common Source
VDS = -3 V
Ta = 25°C
Pulse Test
Forward transfer admittance |Yfs| (S)
10
3
1
0.3
0.1
-0.01
-0.1
-1
-10
Drain current ID (A)

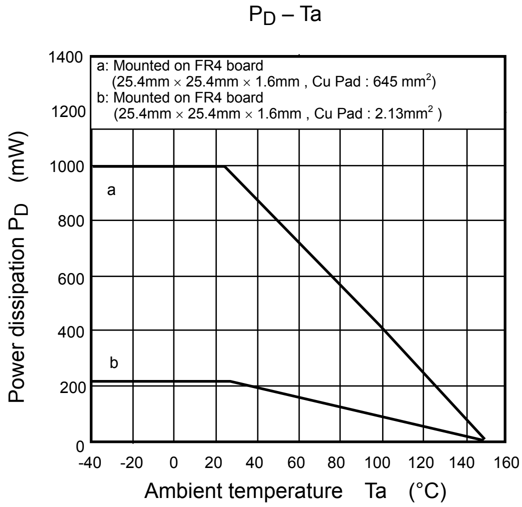

IDR – VDS
Common Source
VGS = 0 V
Pulse Test
D
G
S
IDR
-25 °C
25 °C
Ta =100 °C
Drain reverse current IDR (A)
10
1
0.1
0.01
0.001
0
0.5
1.0
1.5
Drain–source voltage VDS (V)


C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25 °C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
1000
300
100
30
10
-0.1
-1
-10
-100
Drain-source voltage VDS (V)


t – ID
Common Source
VDD = -10 V
VGS = 0 to -2.5 V
Ta = 25 °C
RG = 4.7Ω
toff
tf
ton
tr
Switching time t (ns)
10000
1000
100
10
1
-0.001
-0.01
-0.1
-1
-10
Drain current ID (A)


Dynamic Input Characteristic
Common Source
ID = -3.5 A
Ta = 25°C
VDD = - 10 V
VDD = - 16 V
Gate–source voltage VGS (V)
-8
-6
-4
-2
0
0
2
4
6
8
10
Total gate charge Qg (nC)


Rth – tw
Transient thermal impedance Rth (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
b
a
Single pulse
a. Mounted on F4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm2)
b. Mounted on F4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 2.13 mm2)


PD – Ta
Power dissipation PD (mW)
1400
1200
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 645 mm2)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 2.13mm2)
a
b

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