

MOSFET - Dual P-Channel, POWERTRENCH®

NDC7003P

General Description

These dual P-Channel Enhancement Mode Power Field Effect Transistors are produced using onsemi's proprietary Trench Technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- $-0.34\text{ A}, -60\text{ V}$ $R_{DS(ON)} = 5\text{ }\Omega$ @ $V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 7\text{ }\Omega$ @ $V_{GS} = -4.5\text{ V}$
- Low Gate Charge
- Fast Switching Speed
- High Performance Trench Technology for Low $R_{DS(ON)}$
- SUPERSOT™ -6 Package: Small Footprint (72% smaller than standard SO-8); Low Profile (1 mm Thick)
- This is a Pb-Free Device

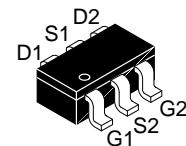
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|----------------|---|--------------------|------|
| V_{DSS} | Drain-Source Voltage | -60 | V |
| V_{GSS} | Gate-Source Voltage | ± 20 | V |
| I_D | Drain Current - Continuous (Note 1a) - Pulsed | -0.34 -1 | A |
| P_D | Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c) | 0.96 0.9 0.7 | W |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | °C |

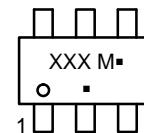
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|-----------------|---|---------|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 130 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 60 | |

TSOT23 6-Lead
CASE 419BL

MARKING DIAGRAM



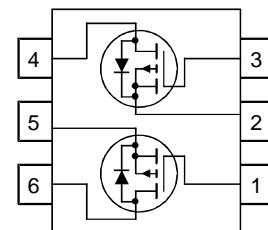
XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT



SOT-6 (SUPERSOT™ -6)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------|------------------------|-----------------------|
| NDC7003P | TSOT-23-6 (Pb-free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NDC7003P

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|--|-----|-----------|------|----------------------------|
| OFF CHARACTERISTICS | | | | | | |
| BV_{DSS} | Drain–Source Breakdown Voltage | $I_D = -250 \mu\text{A}$, $V_{\text{GS}} = 0 \text{ V}$ | -60 | | | V |
| $\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250 \mu\text{A}$, Referenced to 25°C | | -57 | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{\text{DS}} = -48 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$ | | -1 | | μA |
| I_{GSS} | Gate–Body Leakage, Forward | $V_{\text{GS}} = \pm 20 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$ | | ± 100 | | nA |
| ON CHARACTERISTICS (Note 2) | | | | | | |
| $V_{\text{GS}(\text{th})}$ | Gate Threshold Voltage | $V_{\text{DS}} = V_{\text{GS}}$, $I_D = -250 \mu\text{A}$ | -1 | -1.9 | -3.5 | V |
| $\frac{\Delta V_{\text{GS}(\text{th})}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = -250 \mu\text{A}$, Referenced to 25°C | | 3.2 | | $\text{mV/}^\circ\text{C}$ |
| $R_{\text{DS}(\text{ON})}$ | Static Drain–Source On–Resistance | $V_{\text{GS}} = -10 \text{ V}$, $I_D = -0.34 \text{ A}$ | | 1.2 | 5 | Ω |
| | | $V_{\text{GS}} = -4.5 \text{ V}$, $I_D = -0.25 \text{ A}$ | | 1.5 | 7.5 | |
| | | $V_{\text{GS}} = -10 \text{ V}$, $I_D = 0.34 \text{ A}$, $T_J = 125^\circ\text{C}$ | | 1.9 | 10 | |
| $I_{\text{D}(\text{on})}$ | On–State Drain Current | $V_{\text{GS}} = -10 \text{ V}$, $V_{\text{DS}} = -10 \text{ V}$ | -1 | | | A |
| g_{FS} | Forward Transconductance | $V_{\text{DS}} = -10 \text{ V}$, $I_D = -0.34 \text{ A}$ | | 700 | | mS |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C_{iss} | Input Capacitance | $V_{\text{DS}} = -25 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$ | | 66 | | pF |
| C_{oss} | Output Capacitance | | | 13 | | |
| C_{rss} | Reverse Transfer Capacitance | | | 6 | | |
| R_{G} | Gate Resistance | $V_{\text{GS}} = 15 \text{ mV}$, $f = 1.0 \text{ MHz}$ | | 11.2 | | Ω |
| SWITCHING CHARACTERISTICS (Note 2) | | | | | | |
| $t_{\text{d}(\text{on})}$ | Turn–On Delay Time | $V_{\text{DD}} = -25 \text{ V}$, $I_D = -1 \text{ A}$, $V_{\text{GS}} = -10 \text{ V}$, $R_{\text{GEN}} = 6 \Omega$ | | 3.2 | 6.4 | ns |
| t_r | Turn–On Rise Time | | | 10 | 20 | |
| $t_{\text{d}(\text{off})}$ | Turn–Off Delay Time | | | 8 | 16 | |
| t_f | Turn–Off Fall Time | | | 1 | 2 | |
| Q_g | Total Gate Charge | $V_{\text{DS}} = -25 \text{ V}$, $I_D = -0.34 \text{ A}$, $V_{\text{GS}} = -10 \text{ V}$ | | 1.6 | 2.2 | nC |
| Q_{gs} | Gate–Source Charge | | | 0.3 | | |
| Q_{gd} | Gate–Drain Charge | | | 0.3 | | |

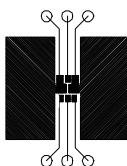
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

| | | | | | | |
|-----------------|---|--|--|-------|------|---|
| I_S | Maximum Continuous Drain–Source Diode Forward Current | | | -0.34 | A | |
| V_{SD} | Drain–Source Diode Forward Voltage | $V_{\text{GS}} = 0 \text{ V}$, $I_S = -0.34 \text{ A}$ (Note 2) | | -0.8 | -1.4 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

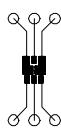
1. $R_{\theta\text{JA}}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta\text{JC}}$ is guaranteed by design while $R_{\theta\text{CA}}$ is determined by the user's board design.

1a



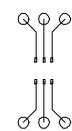
a) 130°C/W when mounted on a 0.125 in^2 pad of 2oz copper.

1b



b) 140°C/W when mounted on a 0.005 in^2 pad of 2oz copper.

1c



c) 180°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width $< 300 \mu\text{s}$, Duty cycle $< 2.0 \%$.

TYPICAL CHARACTERISTICS

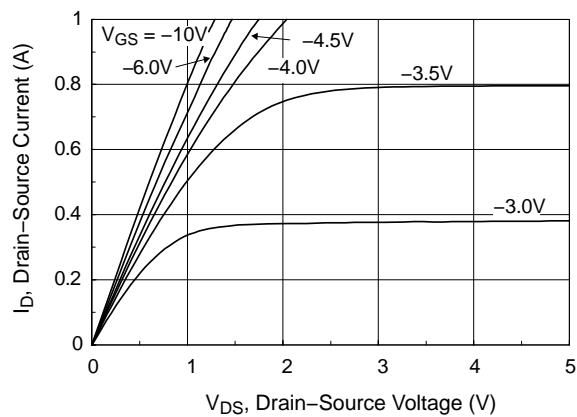


Figure 1. On-Region Characteristics

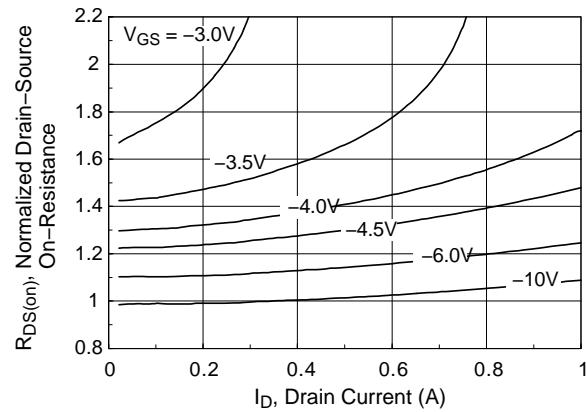


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

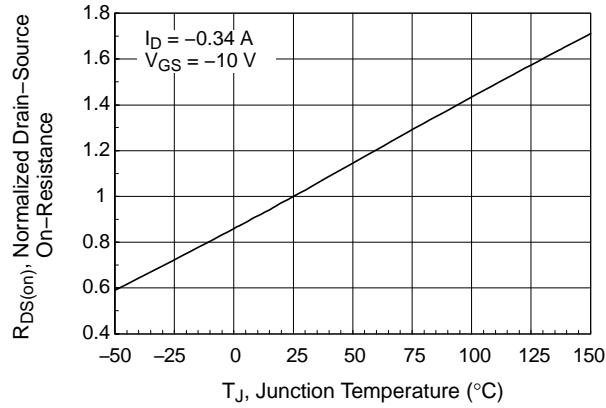


Figure 3. On-Resistance Variation with Temperature

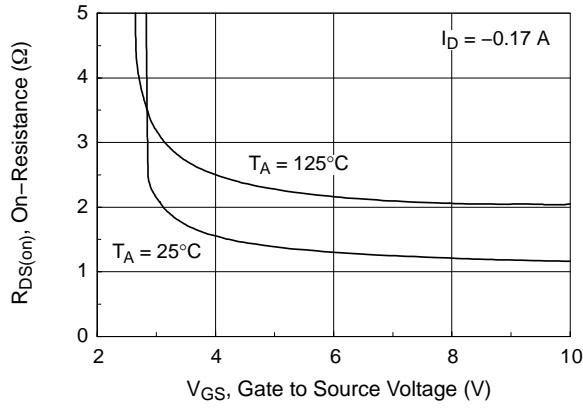


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

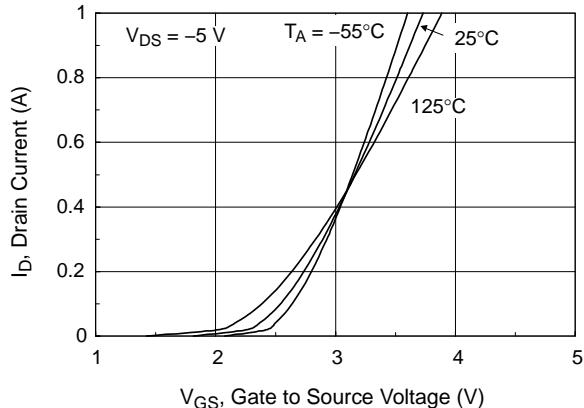


Figure 5. Transfer Characteristics

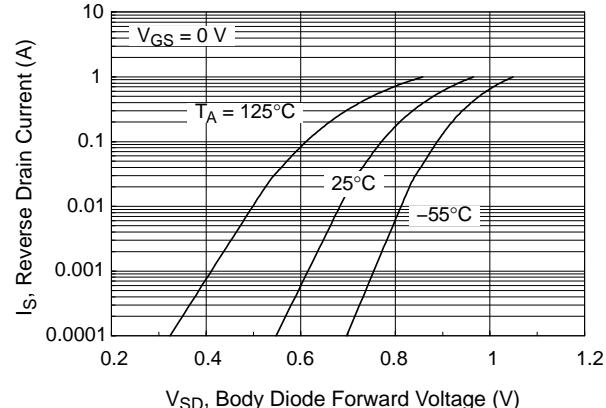


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS

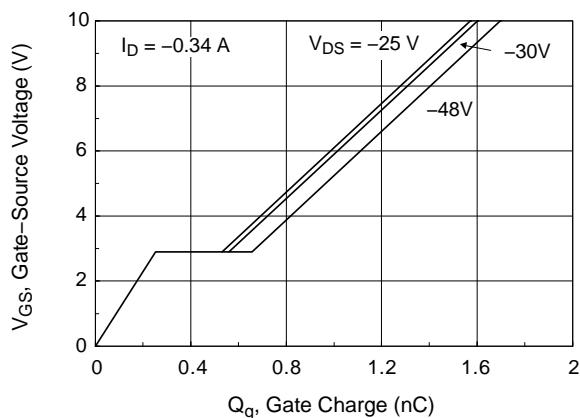


Figure 7. Gate Charge Characteristics

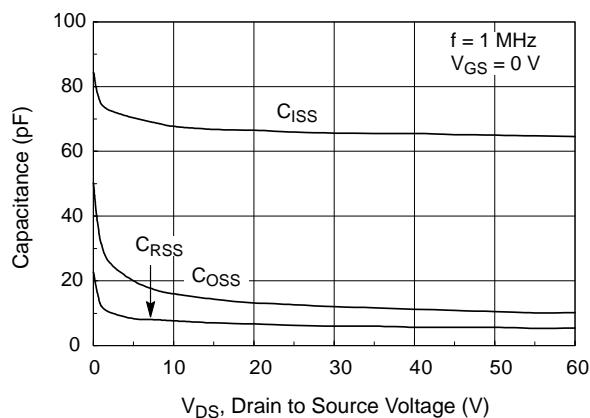


Figure 8. Capacitance Characteristics

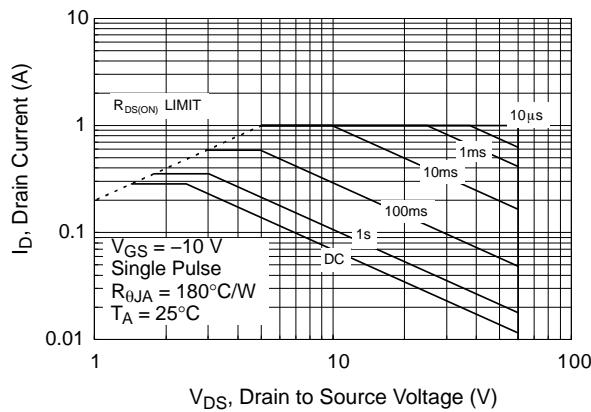


Figure 9. Maximum Safe Operating Area

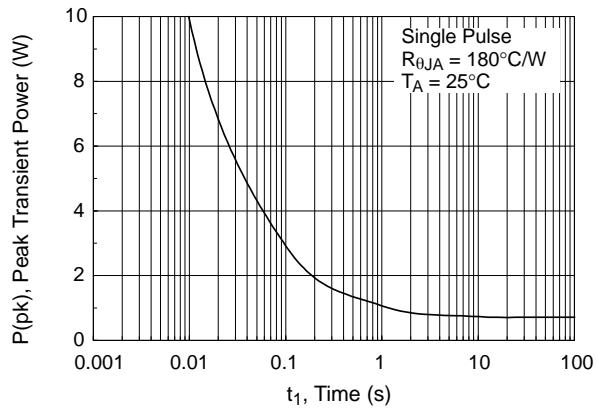


Figure 10. Single Pulse Maximum Power Dissipation

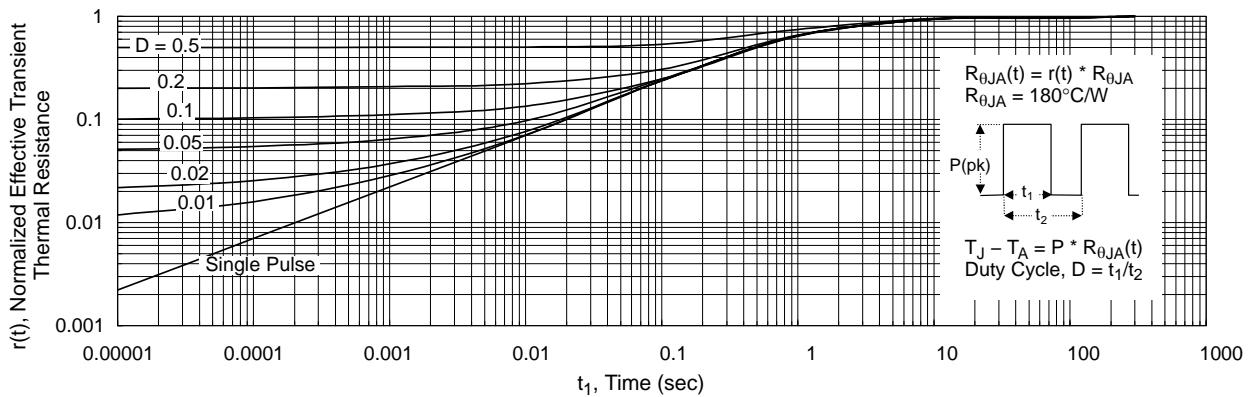


Figure 11. Transient Thermal Response Curve

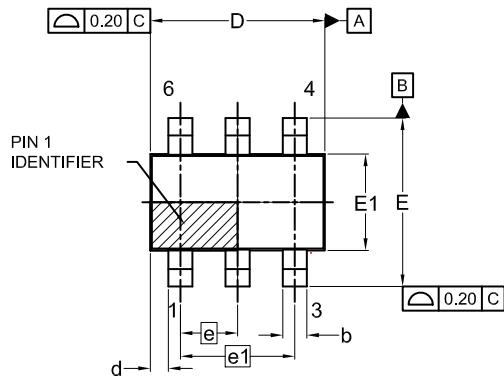
(Note: Thermal characterization performed using the conditions described in Note 1c.)

Transient thermal response will change depending on the circuit board design.)

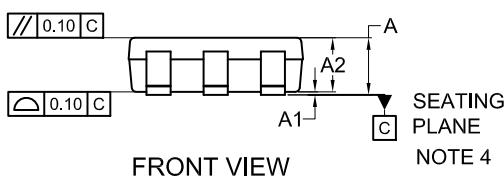
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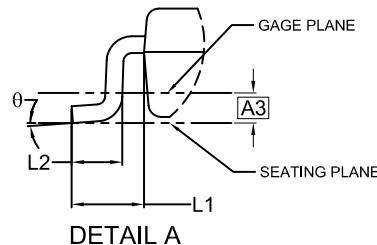
SCALE 2:1



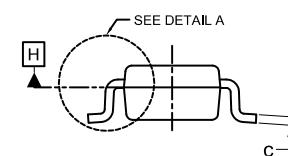
TOP VIEW



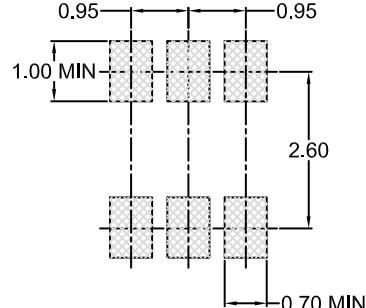
FRONT VIEW



DETAIL A



SIDE VIEW

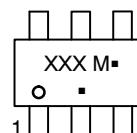
LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 0.70 | 0.85 | 1.00 |
| A3 | 0.25 BSC | | |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.80 | 2.95 | 3.10 |
| d | 0.30 REF | | |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | 0.95 BSC | | |
| e1 | 1.90 BSC | | |
| L1 | 0.60 REF | | |
| L2 | 0.20 | 0.40 | 0.60 |
| Θ | 0° | -- | 10° |

GENERIC
MARKING DIAGRAM*

XXX = Specific Device Code

M = Date Code

- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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| DESCRIPTION: | TSOT23 6-Lead | PAGE 1 OF 1 |

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