High-Speed CAN Transceiver with Partial Networking

ATA6574

Description

The ATA6574 is a stand-alone, high-speed CAN transceiver with partial networking that interfaces a Controller Area Network (CAN) protocol controller and a physical two-wire CAN bus designed for high-speed CAN applications in the automotive environment.

The ATA6574 provides local and enhanced remote wake-up capabilities and is available in a 14-lead SOIC package. It has a very low-power consumption in Standby and Sleep mode. Besides local wake-up via the WAKE pin and remote wake-up pattern according to ISO 11898-2:2024, the ATA6574 additionally supports ISO 11898-2:2024 compliant CAN partial networking. A CAN frame decoder evaluates the bus traffic and checks for a matching frame that has been configured into registers via the SPI. The device is able to keep the complete Automotive Electronic Control Unit (ECU) in a low-power mode, even when bus traffic is present, until a valid wake-up frame has been received. It also features a watchdog (by default off) and a Serial Peripheral Interface (SPI).

The ATA6574 is a CAN FD device. However, selective wake-up is only possible using classical CAN frames. In Sleep mode, the device can be configured to either ignore CAN FD frames or to treat CAN FD frames as frames with errors and increment the internal error counter.

The VIO pin allows the automatic adjustment of the I/O levels to the I/O level of the connected microcontroller.

The SPI interface controls the device and provides status and diagnosis information to the host MCU.

All these features make the ATA6574 an excellent choice for high-speed CAN networks, especially in applications where nodes are always connected to the battery but are only activated when they are really needed in the application.

Features

CAN FD Transceiver

- High-Speed CAN Transceiver Fully Compliant to ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5
- Autonomous Bus Biasing According to ISO 11898-2:2024
- Standard CAN Data-Rate up to 1 Mbit/s and CAN FD Data-Rate up to 5 Mbit/s (CAN FD)
- Differential Bus Receiver with Wide Common-Mode Range
- Transceiver Disengages from the Bus In Overtemperature and Low-Power Supply Mode
- Battery Supply and CAN Bus Pins Protected Against Transients According to ISO 7637
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Short-Circuit Protected to GND and VCC
- RXD Recessive Clamping Detection
- Transmit Data (TXD) Dominant Time-out Function
- Remote Wake-up Pattern According to ISO 11898-2:2024
- Remote Wake-up Frame According to ISO 11898-2:2024 (Selective Wake-up)

Functional Safety Support

- ISO 26262:2018 Functional Safety Ready up to ASIL B

- IEC 61508:2010 Functional Safety Ready up to SIL 2

Misc

- 4 Mbit/s SPI Interface
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Very Low Current Consumption in Sleep and Standby Mode with Full Wake-up Capability
- Power-Down of the Complete Node via the INH-Output (Switching Off External Voltage Regulator(s))
- Local Wake-up via the WAKE Pin
- Host Wake-up via SPI
- Wake-up Source Recognition
- Undervoltage Detection on VS, VCC and VIO Pins
- Overtemperature Protection
- 3.3V to 5V Microcontrollers can be Interfaced Directly via the VIO Pin
- VS Operating Voltage up to 28V, VS DC Supply Voltage up to 40V

Watchdog

- Watchdog with Independent Clock Source
- Watchdog can be Operated in Window and Time-out Mode:
  - Optional cyclic wake-up in Watchdog Time-out mode
  - Watchdog automatically re-enabled when wake-up event captured
  - Watchdog period-selectable
  - Watchdog Reset period-selectable

Automotive Qualification

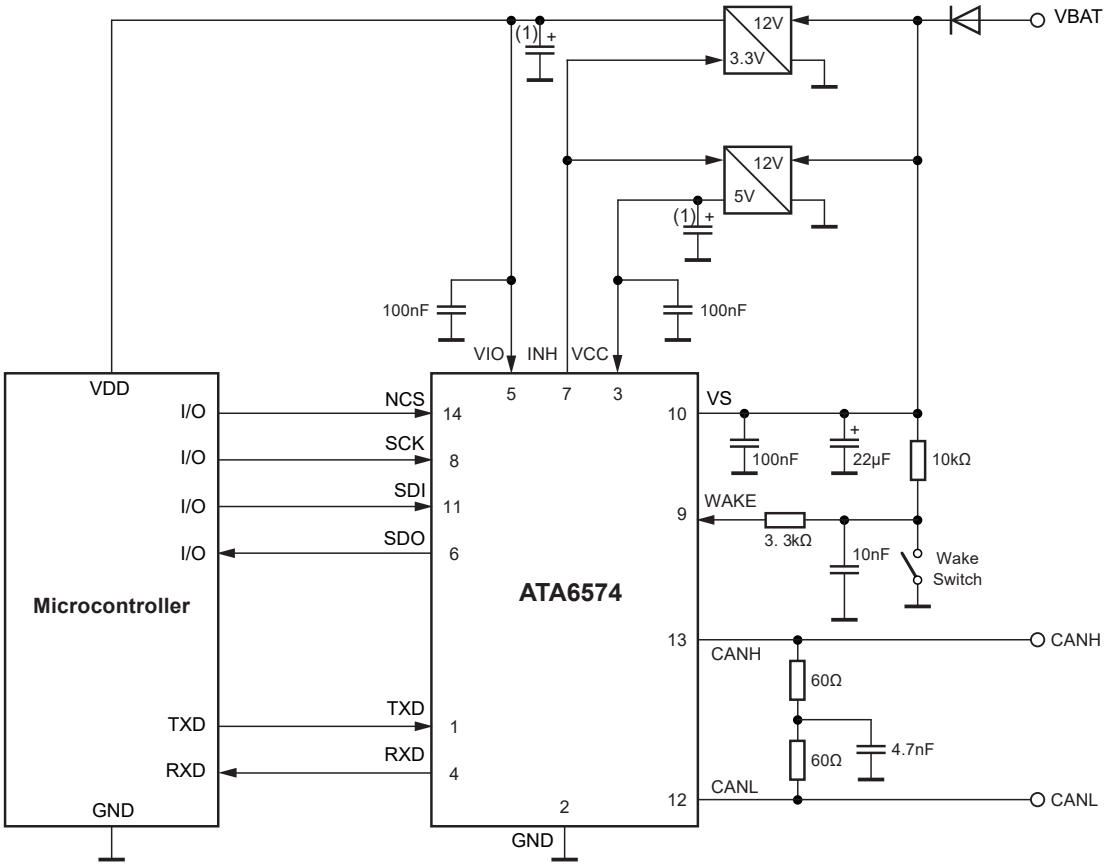
- AEC-Q100 Qualified Rev. J
- Two Ambient Temperature Grades Available:
  - ATA6574-GNQW1-VAO up to T_{amb} = +125°C
  - ATA6574-GNQW0-VAO up to T_{amb} = +150°C
- Fulfills the OEM *"Hardware Requirements for CAN Interfaces in Automotive Applications"*, Rev. 1.3
- Fulfills the OEM *"Requirements for Partial Networking"*, Rev. 2.2
- CAN FD Transceiver Fully Compliant to SAE J2962-2_202402
- ESD According to IBEE CAN EMC Test Specification Following IEC 62228-3:2019, IEC61000-4-2: (330Ω/150 pF) - Pins VS, WAKE ± 8 kV
- ESD According to IBEE CAN EMC Test Specification Following IEC 62228-3:2019, IEC61000-4-2: (330Ω/150 pF) - Pins CANH, CANL ± 6 kV
- 14-Lead SOIC Package (Moisture Sensitivity Level 1)

Applications

- Body Electronics and Lighting
- Automotive Infotainment
- Powertrain Systems
- Advanced Driver Assistance Systems (ADAS)

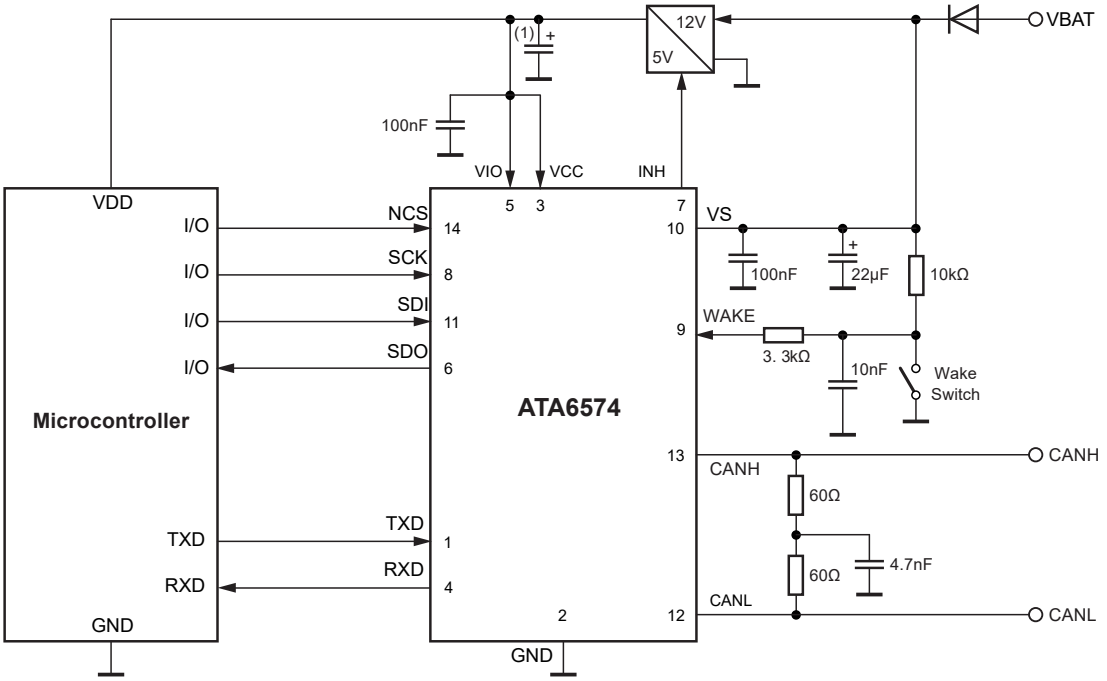
1. Typical Application Circuits

Figure 1-1. Typical Application Circuit ATA6574



Note:
1. The value of these capacitors depends on the external voltage regulators used.

Figure 1-2. Typical Application Circuit 5V Only



Note:
1. The value of this capacitor depends on the external voltage regulator used.

2. Product Family

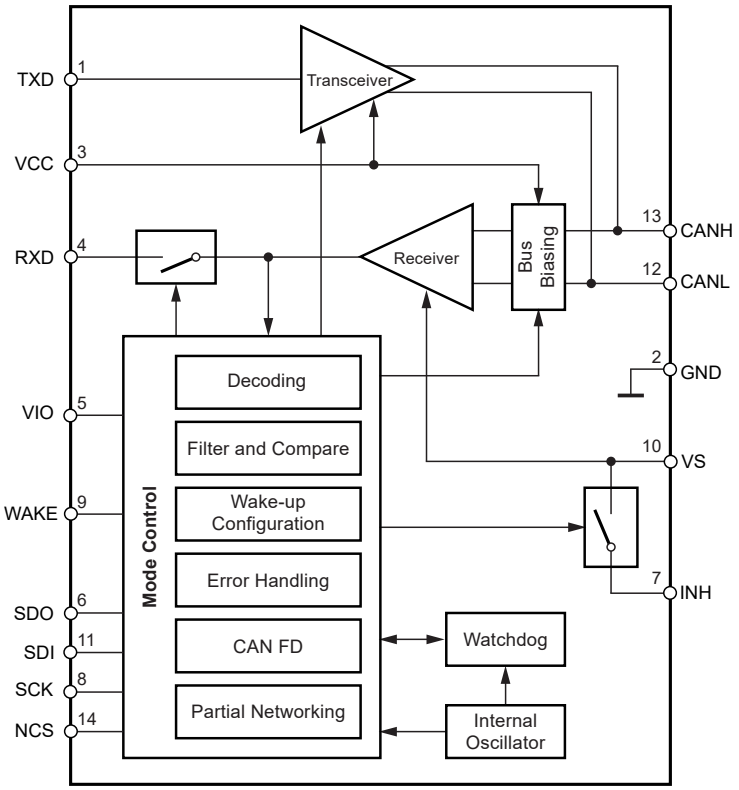
The device names, features, and package types of each device are listed in the following table. All devices integrate a high-speed CAN FD transceiver.

Table 2-1. ATA6574 Family Members

Device	Grade 0	Grade 1	Package
ATA6574-GNQW1-VAO		x	SOIC14
ATA6574-GNQW0-VAO	x		SOIC14

3. Block Diagram

Figure 3-1. Simplified Block Diagram



4. Pin Configuration

Figure 4-1. Pin Configuration

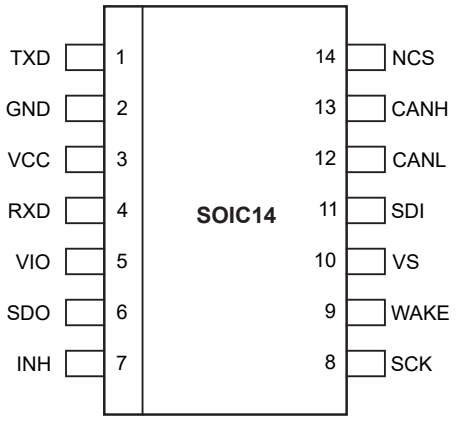


Table 4-1. Pin Description

Pin SOIC14	Symbol	Function
1	TXD	Transmit Data Input
2	GND	Ground
3	VCC	5V CAN Transceiver Supply Voltage
4	RXD	Receive Data Output, reads out data from the CAN bus
5	VIO	Supply Voltage for I/O Level Adapter
6	SDO	SPI Serial Data Output
7	INH	High-Side Output for Switching External Voltage Regulators
8	SCK	SPI Clock
9	WAKE	High-Voltage Input for Local Wake-up
10	VS	Battery Supply Voltage
11	SDI	SPI Serial Data Input
12	CANL	Low-Level CAN Bus Line
13	CANH	High-Level CAN Bus Line
14	NCS	SPI Chip Select Input

4.1 Supply Pin (VS)

The VS supply pin is the power supply pin for the ATA6574 device. In an application, this pin is usually connected to the battery via a serial diode for reverse battery protection. This pin withstands standard automotive conditions, such as 40V during a load dump.

An undervoltage detection circuit is implemented to avoid malfunctions or false bus messages. After switching on VS, the device starts in Standby mode and the INH output is switched on.

4.2 Ground Pin (GND)

The device does not affect the CAN bus in the event of GND disconnection.

4.3 Supply Pin (VCC)

This is the supply pin for the CANH and CANL bus drivers, the bus differential receiver and the bus biasing voltage circuitry. VCC is monitored for undervoltage conditions.

4.4 Supply Pin (VIO)

This is the supply pin for the digital input/output pins. VIO is monitored for undervoltage conditions. See Fail-Safe Features.

4.5 Bus Pins (CANH AND CANL)

These are the CAN bus terminals.

CANH is a high-side driver to VCC, and CANL is a low-side driver to GND. In Normal mode and with TXD high, the CANH and CANL drivers are off, and the voltage at CANH and CANL is approximately 2.5V, provided by the internal bus biasing circuitry. This state is called recessive.

When TXD is low, CANL is pulled to GND and CANH to VCC, creating a differential voltage on the CAN bus. This is called the dominant state.

In Standby mode, the CANH and CANL drivers are off. If the device is in Unpowered mode or Sleep mode, CANH and CANL are highly resistive with extremely low leakage current to GND, making the device ideally passive.

Pins CANH and CANL have integrated ESD protection and extremely high robustness against external disturbances, such as EMC and electrical transients. The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage, and are also protected against overtemperature.

4.6 Input Pin (TXD)

This is the device input pin that controls the CAN bus level. In the application, this pin is connected to the microcontroller transmit terminal. The TXD pin has an internal pull-up toward VIO to ensure a safely defined recessive driver state in case this pin is left floating.

In Normal mode, when TXD is high or floating, the CAN bus is driven to the recessive state.

TXD must be pulled to GND in order to activate the CANH and CANL drivers and set the bus to the dominant state. A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)}$ TXD, the transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high.

If the TXD pin is held low (e.g., by a short circuit to GND), the transmitter is disabled and the device is switched into Normal mode and the bus lines are in the recessive state. The transceiver remains in this state until the TXD pin goes high.

4.7 Output Pin (RXD)

In Normal and Silent modes, this pin reports the state of the CAN bus to the microcontroller. In the application, this pin is connected to the microcontroller receive terminal. RXD is high when the bus is recessive. When the bus is dominant, RXD is low.

The output is a push-pull structure. The high side is connected to VIO and the low side to GND.

In Standby mode, the RXD output is switched to VIO. When a wake-up event is detected, RXD will be forced to low.

An RXD recessive clamping function (see section RXD Recessive Clamping) is implemented. This fail-safe feature prevents the controller from sending data on the bus if the RXD line is clamped to high (e.g., recessive).

4.8 Inhibit Output Pin (INH)

The inhibit output pin provides an internal switch towards VS and is used to control external voltage regulators. If the device is in Normal or Standby mode, the inhibit high-side switch is turned on. When the device is in Sleep mode, the inhibit switch is turned off, thus disabling the connected external voltage regulators or other connected external devices.

A wake-up event on the CAN bus or at the WAKE pin switches the INH pin to the VS level. After a system power-up (VS rises from zero), the INH pin switches to the VS level automatically.

The INH output pin has an additional function when the watchdog is enabled. At every Watchdog Reset, the INH pin will be switched off for a predefined time. This will trigger a Power-on Reset (POR) of the microcontroller if the supply of the microcontroller is controlled by the INH pin.

4.9 Wake Input Pin (WAKE)

In the ATA6574, this pin is a high-voltage input used for waking up the device from Sleep mode. It is usually connected to an external switch to generate a local wake-up. If the WAKE pin is not needed, the local wake-up should be disabled and the WAKE pin should be connected to GND to ensure optimal EMI performance.

The WAKE pin has a special design structure and is triggered by a LOW-to-HIGH and/or a HIGH-to-LOW transition on the WAKE pin. This feature allows for maximum flexibility when designing a local wake-up circuit.

An internal filter is implemented to avoid a false wake-up event due to noise. A serial resistor should be inserted in order to limit the input current mainly during transient pulses and ESD. The recommended resistor value is 10 kΩ. An external 10 nF capacitor is advised for better EMC and ESD performance (see Typical Application Circuits).

4.10 SPI Serial Data In Pin (SDI)

Serial Data In input connected to an output of the microcontroller.

4.11 SPI Serial data out Pin (SDO)

Serial Data Out output connected to an input of the microcontroller; this pin is in tri-state if NCS is high.

4.12 SPI Clock Pin (SCK)

Serial data clock; default level is low due to internal pull-down.

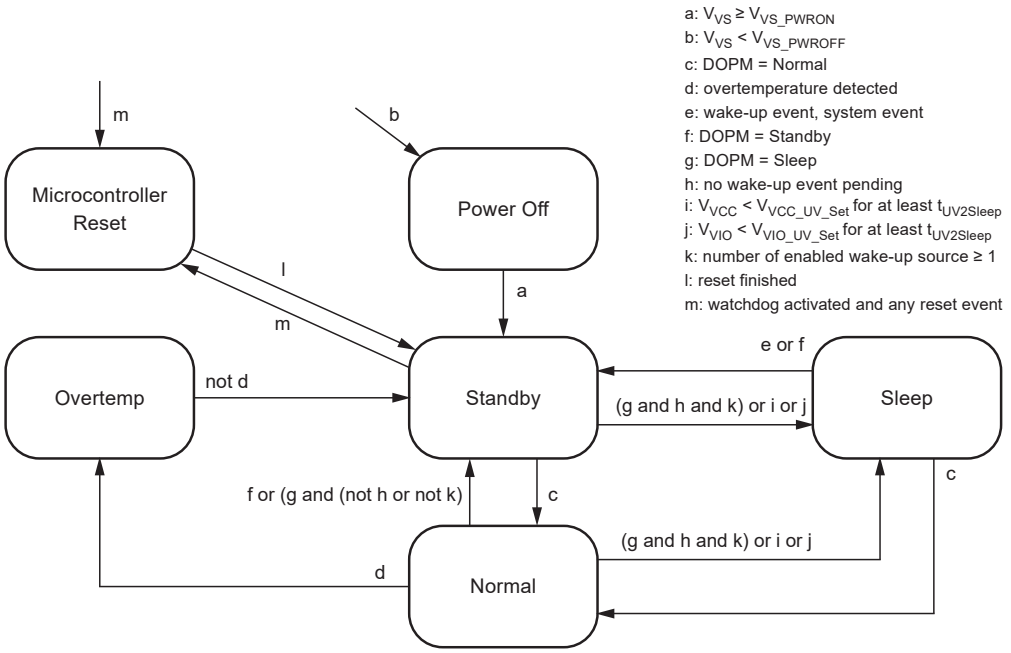
4.13 SPI Chip Select Pin (NCS)

Chip Select pin; active-low. If Chip Select is not active, no data are loaded from SDI on SCK edges or provided at SDO.

5. Functional Description

5.1 Device Operating Modes

Figure 5-1. Overview to the Device Operating Modes



The mode control unit in the ATA6574 implements six different modes, as depicted in Figure 5-1. All of the modes are briefly described in this section.

Table 5-1. Operating Modes and Functions

Block	Device Operating Mode				
	Power Off	**Standby**	**Normal**	**Sleep**	**Overtemp**
SPI	Disabled	Active	Active	Active if VIO Supplied	Disabled
INH	High Ohmic	VS Level	VS Level	High Ohmic	VS Level
CAN	TRX Off	TRX Standby/TRX Biased Standby	TRX Normal/TRX Standby/TRX Biased Standby/TRX Silent (determined by bits COPM)	TRX Standby/TRX Biased Standby	TRX Off
RXD	VIO Level	VIO Level/Low if Wake-up/ Interrupt Event Detected	CAN Bit Stream if COPM = 01/10/11; Otherwise, same as Standby/Sleep	VIO Level/Low if Wake-up/ Interrupt Event Detected	VIO Level/Low if Wake-up/ Interrupt Event Pending

5.1.1 Power-Off Mode

The device is in Power-Off mode when the supply voltage of the device (V_{VS}) is lower than the defined device power-off detection voltage threshold (V_{VS_PWROFF}). This is the default mode when the battery is first connected. In this mode, the integrated CAN transceiver is in the TRX Off mode (see section TRX Off Mode). The watchdog is also in Off mode. The pins, CANH and CANL, are high ohmic, and the INH output is switched off. The device is not able to provide any functionality. As soon as V_{VS} rises above the power-on detection threshold (V_{VS_PWRON}), the device starts the transition to Standby mode. The whole device is reset and initialized. After $t_{startup}$, the device is in the Standby mode.

5.1.2 Standby Mode

The Standby mode is the default mode after a Power-on Reset. In Standby mode, the integrated CAN transceiver is unable to transmit or receive data. The INH pin is at the VS level, and the external voltage regulator controlled by the pin is switched on.

The ATA6574 supports the autonomous bus biasing according to ISO 11898-2:2024 in Standby and Sleep modes (provided $V_{VS} > V_{VS\_UV\_CAN\_Clear}$). The bus pins are biased to GND (via R_{CANH}, R_{CANL}) when the bus is inactive and at approximately 2.5V when a remote CAN bus wake-up request (Wake-Up Pattern, WUP, according to ISO 11898-2:2024) is detected.

In Standby mode, the ATA6574 supports both CAN bus remote wake-up via a standard WUP and via a selective Wake-up Frame (WUF). The CAN bus remote wake-up is only activated when the register bit CWUE is set to '1' (see section TRXECR). The low-power wake-up comparator in the receiver then monitors the bus activity and wakes up the device after detecting a valid wake-up event (V_{VS} must be above the VS CAN undervoltage release threshold; otherwise, the integrated transceiver is in TRX Off mode and no bus wake-up can be detected).

If CPNE = PNCFOK = 1, the selective wake-up is enabled. After a successful detection of a wake-up pattern, the bus pins are biased to 2.5V and the device is ready for decoding WUFs. Only after detecting a valid WUF, the wake-up event is registered and the wake-up process is finished. Decoding of CAN data and remote frames is supported during all mode transitions of the device. If the data frame is a valid WUF, the device will indicate a wake-up event.

If the selective wake-up is disabled and CAN remote wake-up is enabled, the standard wake-up via WUP is activated. The device biases its bus pin to 2.5V after successfully detecting a wake-up pattern, registers the wake-up event and completes the wake-up process.

The device also supports detecting system events (see section Wake-up and Interrupt Event Diagnosis via RXD Pin) and a local wake-up event via the WAKE pin in Standby mode. The internal wake-up flags, CWUS, LWURS and LWUFS (see sections TRXESR and WKESR), and the system event status registers are set to '1' by the device if the corresponding event is detected.

The device will not leave Standby mode after detecting a valid wake-up event. It will only set the corresponding internal Status register bits. A transition to the Normal mode will only happen when the register bits DOPM are set to '111' via SPI.

In Standby mode, the detection of a wake-up event or an interrupt event (see section Wake-up and Interrupt Event Diagnosis via RXD Pin) is denoted via the RXD pin, provided that the corresponding event interrupt is enabled (see section SECR to section WKECR). The RXD pin is usually at V_{VIO} level and will be forced to low if an enabled event is detected. The Status registers (see sections GESR through WKESR) allow the microcontroller to get further detailed information about the device via SPI.

As shown in Figure 5-1, the device will enter Standby mode in the following cases:

1. From Power-Off mode: When the Power-on Reset disappears after V_{VS} rises above the power-on detection voltage threshold V_{VS_PWRON}.
2. From Overtemp mode: After the chip temperature drops more than the thermal shutdown hysteresis T_{vJsd_hys}.
3. From Sleep mode: After detecting enabled wake-up event or interrupt event.
4. From Sleep mode or Normal mode via SPI (DOPM = 0x4): If a valid interface voltage V_{VIO} is applied.
5. During a pending wake-up event: If Sleep mode is requested (DOPM = 0x1 is written) via SPI or all wake-up sources are disabled.

The watchdog can be activated (Window or Time-out mode) in Standby mode. To avoid unwanted configuration of the watchdog, configuration can only be done in Standby mode.

5.1.3 Sleep Mode

Sleep mode is the most power-saving mode of the device. In this mode, the INH output is switched off. Therefore, the external voltage regulator(s) controlled by this pin is also switched off. This is the only difference between Sleep mode and Standby mode. If a valid Interface Supply Voltage (V_{VIO}) is applied, registers of the device can still be accessed via the device's SPI interface.

As in Standby mode, the device can react to a variety of wake-up events (see section Wake-up). The device can be configured to be woken up in different ways. If a valid Interface Voltage V_{VIO} is applied, it is even possible to wake up the device from Sleep mode via an SPI command (DOPM = Standby/Normal).

The INH output switches on when either a CAN bus wake-up event, a host wake-up event (via SPI), a local wake-up, or an interrupt event (see section Interrupt Event/Wake-up Event Delay) is detected and the device switches into Standby mode. The INH output also switches on when a Watchdog Reset (Time-out mode) occurs and the device switches to microcontroller Reset mode.

As shown in Figure 5-1, the device enters Sleep mode in the following cases:

1. From the Normal mode or Standby mode via an SPI command, if no wake-up event is pending and at least one wake-up source (see section Wake-up) is enabled.
2. From the Normal mode or Standby mode, when detecting VCC or VIO undervoltage ($V_{VIO} < V_{VIO\_UV\_Set}$ or $V_{VCC} < V_{VCC\_UV\_Set}$ for $t > t_{UV2Sleep}$). In this case, all pending wake-up events will be cleared. CAN bus wake-up (CWUE = 1; see section TRXECR) and local wake-up via the WAKE pin (LWUFE = 1 && LWURE = 1) are enabled. Selective wake-up is disabled (see section VCC/VIO Undervoltage Protection for details about VCC/VIO undervoltage protection).

The ATA6574 provides an SMTS bit (see DMSR) to denote whether or not the recent transition to Sleep mode is triggered by a VCC/VIO undervoltage event. The bit can be read by the microcontroller in Sleep mode (if a valid interface supply voltage is provided) or after waking up from Sleep mode.

5.1.4 Normal Mode

In Normal mode, the transceiver can transmit and receive data through the bus lines CANH and CANL. This is the normal transmitting and receiving mode of the CAN Interface, in accordance with the CAN specification. The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the differential signal on the bus lines into a digital signal, which is output to the RXD pin. The bus biasing is set to $V_{VCC/2}$. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible Electromagnetic Emission (EME).

The INH output is switched ON, so external loads controlled by the INH pin are also switched ON.

Wake-up flag CWUS and Interrupt Event Status registers will still be set to '1' by the device if the corresponding event is detected.

As shown in Figure 5-1, the device will enter Normal mode from Standby mode or Sleep mode via an SPI command.

5.1.5 Overtemp Mode

The Overtemp mode is the operating mode which protects the device against damage due to overtemperature. The overtemperature protection is only active in Normal mode.

The device provides two levels of overtemperature protection. If the chip temperature rises above the overtemperature protection prewarning threshold ($T > T_{OT\_Prew}$), the device first sets the status bit to OTPWS = 1. If the overtemperature prewarning interrupt is enabled (OTPWE = 1), an overtemperature prewarning interrupt will be generated (OTPW = 1, RXD signalization if COPM = 00 and DOPM = 111 (Normal mode)).

The device will enter Overtemp mode when the chip temperature rises above the overtemperature protection shutdown threshold (T_{jsd}). In Overtemp mode, the integrated CAN transceiver is switched

to the TRX Off mode. The CAN bus pins are high ohmic. No further wake-up event will be detected, but the pending wake-up/interrupt event will still be signaled by a low level on pin RXD. As shown in Figure 5-1, the device will enter Overtemp mode from Normal mode when the chip temperature rises up the overtemperature protection shutdown threshold.

The device will exit Overtemp mode and enter Standby mode when the chip temperature drops by more than the thermal shutdown hysteresis (T_{vJsd_hys}) or when the device is powered off.

5.1.6 Microcontroller Reset Mode

Transitions to Reset mode are only enabled when the watchdog is activated. In this mode, the INH output is switched off and the transceiver is disabled. The device transitions to Standby mode when the reset pulse width is reached.

5.1.7 Related Registers

5.1.7.1 Device Mode Control Register (Address 0x01)

Name: DMCR
Offset: 0x01
Reset: 0x4
Property: Read/Write

The device operating mode is selected via bits DOPM in the device mode control register. The register is accessed via SPI at address 0x01. The register reflects the current mode when read.

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					DOPM[2:0]		
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

Bits 7:3 – Reserved[4:0] Reserved for future use

Bits 2:0 – DOPM[2:0] Select Device Operating Mode

DOPM[2:0]	Device Operating Mode
3'b001	Sleep mode
3'b100	Standby mode
3'b111	Normal mode

5.1.7.2 Device Mode Status Register (Address 0x03)

Name: DMSR
Offset: 0x03
Reset: 0x20
Property: Read-only

The register provides device operating mode transition related information.

Bit	7	6	5	4	3	2	1	0
	SMTS	OTPWS	NMTS	Reserved[4:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	0

Bit 7 – SMTS Sleep mode transition status
The device sets the bit to '0' if the recent transition to Sleep mode was triggered by an SPI command and sets the bit to '1' if the recent transition to Sleep mode was forced by a VCC/VIO undervoltage.

Bit 6 – OTPWS Overtemperature prewarning status

The device sets the bit to '1' if the device temperature is higher than the overtemperature prewarning threshold and to '0' if the device temperature is below the overtemperature prewarning threshold.

Bit 5 – NMTS Normal mode transition status

The device sets the bit to '0' when IC has entered Normal mode after power-up and set the bit to '1' when the IC has powered up but has not yet switched to Normal mode.

Bits 4:0 – Reserved[4:0] Reserved for future use

5.2 Integrated CAN Transceiver Operating Modes

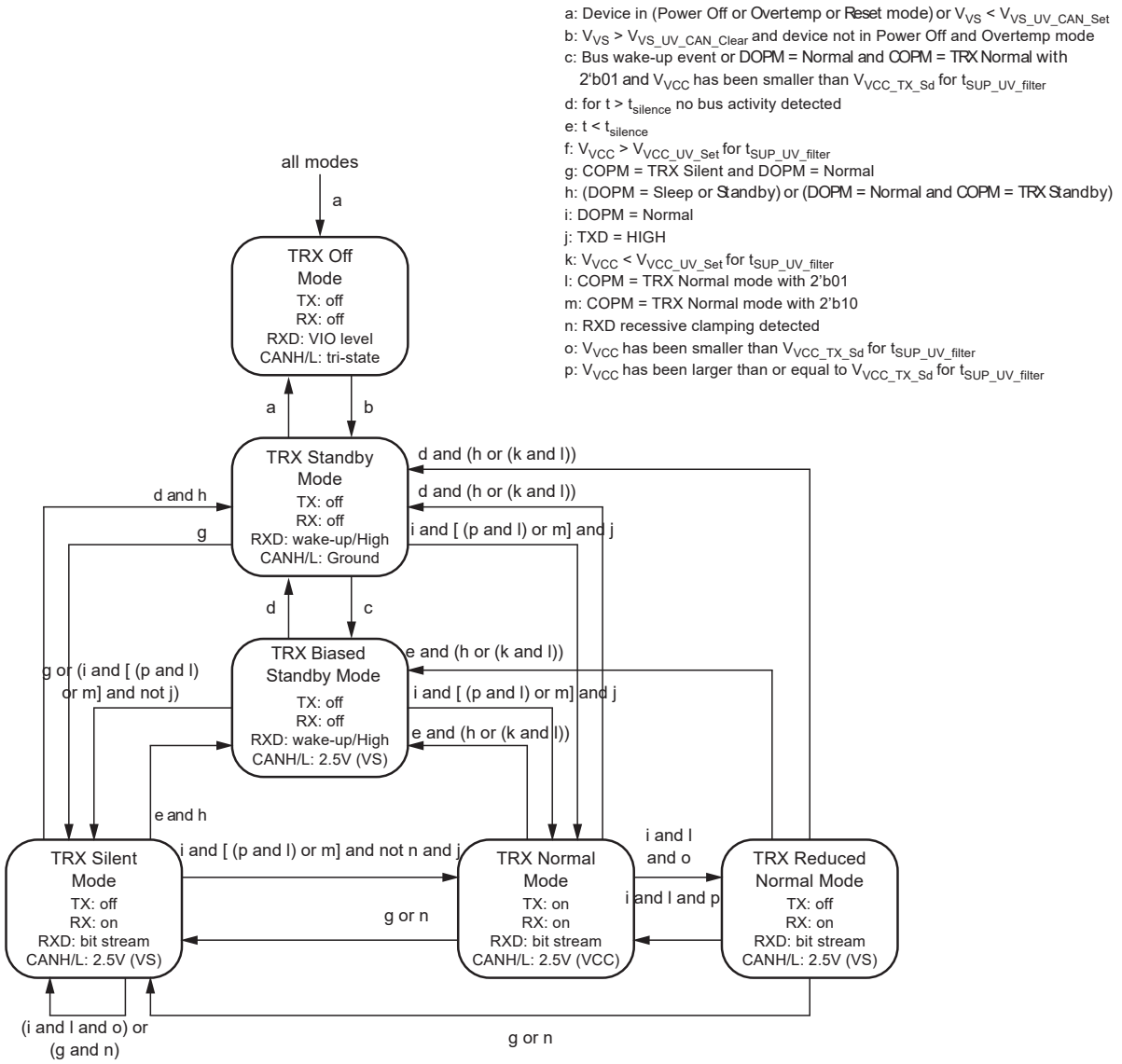
The integrated high-speed CAN transceiver in the ATA6574 is designed for classical CAN bit rates up to 1 Mbit/s and CAN Flexible Data-Rate (CAN FD) bit rates up to 5 Mbit/s. It provides differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:2024 compliant.

The integrated CAN transceiver supports the following operating modes: TRX Normal, TRX Reduced Normal, TRX Silent, TRX Standby and TRX Biased Standby (see Figure 5-2). The CAN transceiver operating mode depends on the device operating mode and on the setting of bits COPM in the CAN Mode Control register (see section TRXCR). When the device is in Normal mode, all four operating modes can be selected. The TRX Biased Standby mode cannot be selected via the COPM bits directly (see section TRX Biased Standby Mode). The operating modes of the integrated transceiver can be selected via bits COPM in the CAN Mode Control register (see section TRXCR). When the device is in Standby or Sleep mode, the transceiver is either in TRX Standby mode or in TRX Biased Standby mode.

The CAN transceiver supports autonomous bus biasing in compliance with ISO 11898-2:2024. It is active in CAN TRX Standby mode. The bus is biased to 2.5V if there is activity on the bus (TRX Biased Standby mode). In TRX Biased Standby mode, the CAN bias voltage is derived directly from V_{VS}. If there is no activity on the bus for $t > t_{Silence}$, the bus is biased to GND (TRX Standby mode).

In TRX Normal and TRX Silent mode, the bus pins, CANH and CANL, are biased to 2.5V (see section TRXCR). The CAN bias voltage is derived from V_{VCC} in TRX Normal mode and derived from V_{VS} in TRX Silent mode. In TRX Off mode, the bus pins are highly resistive and the transceiver is disengaged from the bus.

Figure 5-2. Overview to the Integrated CAN TRX Operating Modes



5.2.1 TRX Off Mode

The CAN transceiver is completely switched off in TRX Off mode. The CAN bus pins, CANH and CANL, are highly resistive and the RXD pin is at the VIO level.

As shown in Figure 5-2, the integrated CAN transceiver enters the TRX Off mode in the following cases:

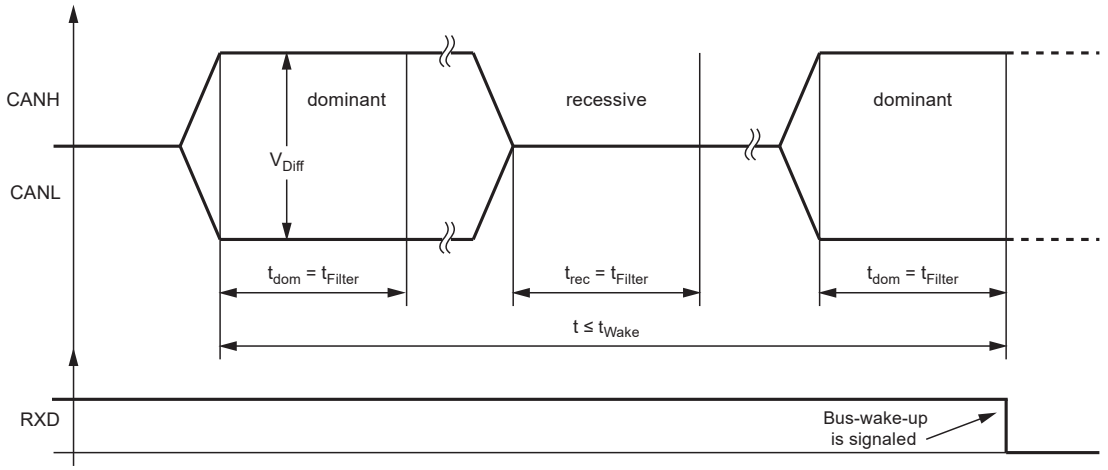
1. The device switches to Power-Off mode.
2. The device switches to Overtemp mode.
3. V_{VS} falls below the CAN undervoltage detection threshold, $V_{VS\_UV\_CAN\_Set}$.

The integrated CAN transceiver will be switched on again and will enter CAN TRX Standby mode when V_{VS} rises above the CAN undervoltage release threshold and the device is no longer in Power-Off/Overtemp mode.

5.2.2 TRX Standby Mode

In TRX Standby mode, the transmitter and the receiver are switched off to reduce current consumption. The wake-up comparator monitors the bus lines for a valid remote bus Wake-up Pattern (WUP), provided that CAN bus wake-up detection is enabled (CWUE = 1). Two periods of dominant bus levels, separated by a period of recessive bus level, each of at least t_{Filter}, switch the RXD pin to low to signal a wake-up request to the microcontroller. Figure 5-3 describes the process and timing of the WUP detection. In the TRX Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum.

Figure 5-3. Timing of CAN Standard Wake-up via Wake-up Pattern (WUP)



As shown in Figure 5-2, the CAN transceiver enters TRX Standby mode in the following cases:

1. When the device leaves Power-Off mode or Overtemp mode and sufficient V_{VS} is applied.
2. Any of the conditions for CAN TRX Biased Standby mode are valid for longer than $t_{Silence}$ (see section TRX Biased Standby Mode).

5.2.3 TRX Biased Standby Mode

The CAN transceiver behavior in the TRX Biased Standby mode is fundamentally the same as in the TRX Standby mode. The only difference is that in the TRX Biased Standby mode, the bus pins are biased to 2.5V. The integrated CAN transceiver will enter this mode when activity is detected on the CAN bus while the transceiver is in TRX Standby mode. The transceiver will return to TRX Standby mode if the CAN bus is silent for longer than $t_{Silence}$ (see Figure 5-4).

As shown in Figure 5-2, the CAN transceiver enters TRX Biased Standby mode in the following cases:

1. From TRX Silent/Normal/Reduced Normal mode, when $t_{Silence}$ did not expire and the device is in Standby (DOPM = 100) or Sleep mode (DOPM = 001).
2. From TRX Silent/Normal/Reduced Normal mode, when $t_{Silence}$ did not expire and the device is in Normal mode (DOPM = 111), and the COPM is set to TRX Standby mode (COPM = 00).
3. From TRX Normal/Reduced Normal mode (COPM = 01), when VCC < $V_{VCC\_UV\_Set}$ is detected and $t_{Silence}$ did not expire.
4. From TRX Standby mode when the device is in Normal mode (DOPM = 111), COPM is set to TRX Normal mode (COPM = 01) and VCC < $V_{VCC\_TX\_Sd}$ has been detected.
5. From TRX Standby mode when a wake-up event is detected on the CAN bus.

5.2.4 TRX Silent Mode

The TRX Silent mode is a Receive-Only mode of the CAN transceiver. It can be used to test the connection of the bus medium or for the software-driven selective wake-up. In the TRX Silent mode, the device can still receive data from the bus, but the transmitter is disabled, and therefore, no data can be sent to the CAN bus. The bus pins are released to the recessive state. All other IC functions continue to operate as they do in the TRX Normal mode. CAN biasing remains active. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.
As shown in Figure 5-2, the CAN transceiver enters the TRX Silent mode in the following cases:

1. The device is in Normal mode (DOPM = Normal) and the CAN transceiver is in TRX Silent mode (COPM = TRX Silent).
2. The device is in Normal mode and the CAN transceiver is in TRX Normal mode, and a RXD recessive clamping failure is detected.

The CAN transceiver will remain in TRX Silent mode if a VCC undervoltage or an RXD recessive clamping failure is detected, even if CAN TRX Normal mode is selected in device Normal mode.

5.2.5 TRX Normal Mode

In TRX Normal mode, the integrated transceiver is able to transmit and receive data via the CANH and CANL bus lines. The output driver stage is active and drives data from the TXD input to the CAN bus. The receiver converts the analog data on the bus lines into digital data, which are output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of V_{VCC} is active.

The slope of the output signals on the bus lines is controlled and optimized in a way that ensures the lowest possible Electromagnetic Emission (EME).

As shown in Figure 5-2, the CAN transceiver enters TRX Normal mode in the following cases:

1. The device is in Normal mode (DOPM = Normal) **AND** the CAN transceiver has been enabled by setting bits COPM to '01' or '10' **AND** no VCC undervoltage is detected, **AND** no RXD recessive clamping is detected.
2. The transceiver is in the TRX Reduced Normal mode and $V_{VCC} > V_{VCC\_TX\_Sd}$ for $t > t_{SUP\_UV\_filter}$.

If pin TXD is held low (e.g., by a short circuit to GND) when CAN TRX Normal mode is selected via bits COPM, the transceiver will not enter CAN TRX Normal mode but will switch to or remain in TRX Silent mode. It will remain in TRX Silent mode until pin TXD goes high in order to prevent a hardware and/or software failure from driving the bus lines to an unwanted dominant state.

The application can determine whether the CAN transceiver is ready to transmit data or is disabled by reading the CAN Transmitter Status bit (TXS) in the Transceiver Status Register (see section TRXSR).

5.2.6 TRX Reduced Normal Mode

In the TRX Reduced Normal mode, the transmitter is switched off as VCC is lower than the $V_{VCC\_TX\_Sd}$ threshold. All other features available in the TRX Normal mode are also provided in the TRX Reduced Normal mode.

As shown in Figure 5-2, the CAN transceiver enters the TRX Reduced Normal mode when the transceiver is in TRX Normal mode and $V_{VCC} < V_{VCC\_TX\_Sd}$ for $t > t_{SUP\_UV\_filter}$.

5.2.7 Related Registers

5.2.7.1 CAN Transceiver Control Register (Address 0x20)

Name: TRXCR
Offset: 0x20
Reset: 0x41
Property: Read/Write

Bit	7	6	5	4	3	2	1	0
	Reserved	CFDPE	PNCFOK	CPNE	Reserved[1:0]		COPM[1:0]	
Access	R	R/W	R/W	R/W	R	R	R/W	R/W
Reset	0	1	0	0	0	0	0	1

Bit 7 – Reserved Reserved for future use

Bit 6 – CFDPE
The host microcontroller should set the bit to '1' to enable the CAN FD passive feature when selective wake-up is activated, otherwise, it should be set to '0'. The bit is set to 1 by default after Power-on Reset. This setting has the effect that CAN FD frames are ignored when the device is waiting for a WUP. If set to '0', the error counter will increase if FD frames with a higher data bit rate are sent during that time.

Bit 5 – PNCFOK
The host microcontroller should set the bit to '1' after successfully configuring the partial networking registers, otherwise set to '0'. In addition, the device will reset the bit to 0 automatically after any write access to the partial networking configuration related registers.

Bit 4 – CPNE
The host microcontroller should set the bit to '1' to enable selective wake-up; otherwise, it should be set to '0'.

Bits 3:2 – Reserved[1:0] Reserved for future use

Bits 1:0 – COPM[1:0]
The TRXCR register is a control register. Therefore, the state of the transceiver will not be mirrored to this register. The COPM bit only defines the targeted state of the transceiver when the device is switched to Normal mode. The finite state machine in Figure 5-2 will not change the COPM bits.

COPM[1:0]	CAN TRX Operating Mode
2'b00	TRX Standby mode.
2'b01	TRX Normal mode (when DOPM = Normal), VCC undervoltage detection active for the transceiver finite state machine. The transceiver switches to the TRX Biased Standby mode immediately after detecting the VCC undervoltage.
2'b10	TRX Normal mode (when DOPM = Normal), VCC undervoltage detection inactive for the transceiver finite state machine. The transceiver switches from TRX Normal/Reduced Normal mode to TRX Biased Standby mode when the device is forced to Sleep mode by a VCC undervoltage event.
2'b11	TRX Silent mode.

5.2.7.2 CAN Transceiver Status Register (Address 0x22)

Name: TRXSR
Offset: 0x22
Reset: 0x48
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	TXS	PNERRS	PNCFS	PNOSCS	CBSS	Reserved	VCCS	TXDOUT
Access	R	R	R	R	R	R	R	R
Reset	0	1	0	0	1	0	0	0

Bit 7 – TXS
The device sets the bit to '1' if the transmitter is ready to transmit data and to '0' if the CAN transmitter is disabled.

Bit 6 – PNERRS
The device sets the bit to '0' if no CAN partial networking error is detected (PNEFD = 0 and PNCFOK = 1 and no oscillator hardware failure is detected (default)); it is set to '1' if PNEFD = 1 || PNCFOK = 0.

Bit 5 – PNCFS
The device sets the bit to '0' if a partial networking configuration error is detected (PNCFOK = 0); otherwise it is set to '1'.

Bit 4 – PNOSCS
The device sets the bit to '1' if the CAN partial networking oscillator is running at target frequency; otherwise it is set to '0'.

Bit 3 – CBSS
The device sets the bit to '1' if the CAN bus is inactive (for longer than $t_{Silence}$); otherwise it is set to '0'.

Bit 2 – Reserved Reserved for future use

Bit 1 – VCCS
The device sets the bit to '1' if V_{VCC} is below the undervoltage detection threshold; it is set to '0' if V_{VCC} is above the undervoltage detection threshold. This bit is only active in Device Standby and Normal mode.

Bit 0 – TXDOUT
The device sets the bit to '1' if the CAN transmitter is disabled due to a TXD dominant time-out event; it is set to '0' if no TXD dominant time-out event was detected.

5.2.7.3 Bus Failure Indication Register (Address 0x33)

Name: BFIR
Offset: 0x33
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						BOUT	BSC
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0] Reserved for future use

Bit 1 – BOUT

The BOUT bit shows the current status of the bus dominant time-out detection. If the bit reads '1', the bus is currently in a dominant time-out state; otherwise, the bit reads '0'.

Bit 0 – BSC

The BSC bit shows the current status of the bus short-circuit event detection. If the bit reads '1', the bus is currently in a short-circuit state, otherwise the bit reads '0'.

5.2.7.4 Transceiver Event Status Register 2 (Address 0x35)

Name: TRXESR2
Offset: 0x35
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[6:0]							RXDRCS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:1 – Reserved[6:0] Reserved for future use

Bit 0 – RXDRCS

The device sets the bit to '1' if the event is enabled in the TRXECR2 register and a RXD recessive clamping event is detected. The bit is reset to '0' by the device either when the device enters Sleep, Standby or Unpowered mode, or the RXD pin shows dominant again.

5.3 Wake-up

5.3.1 Local Wake-up via WAKE Pin

The device provides the high-voltage WAKE input pin that can be used to wake-up the device. It is an edge-sensitive pin (LOW-to-HIGH or HIGH-to-LOW transition). Thus, even if the WAKE pin is at high or low voltage, it is possible to switch the IC into Sleep mode. The WAKE pin is usually connected to the ignition switch to generate a local wake-up when the ignition is switched on.

A glitch suppression circuit is integrated to avoid unexpected wake-up due to noise. The voltage on the pin is detected as stable only when the level remains stable for t_{local_wu}. Therefore, a local wake-up request is detected when the logic level on the WAKE pin has already been stable for at least t_{local_wu} and the new level remains stable for at least t_{local_wu}.

Local wake-up via the WAKE pin can be enabled/disabled via the register bits, LWUFE and LWURE (see section WKECR), and the logic level at the WAKE pin can be read via the register PWKS (see section PWKS) if V_{VIO} is within valid range.

To reduce the battery current during Low-Power mode, the WAKE pin has internal pull-up/pull-down current sources that are activated when a stable level at the WAKE pin has been detected:

- High level on pin is followed by an internal pull-up towards VS.
- Low level is followed by an internal pull-down toward GND.

Local wake-up can only be activated in Standby and Sleep mode. In Normal mode, the status of the voltage on the WAKE pin can always be read via bit PWKVS. Otherwise, PWKVS is only valid if local wake-up is enabled. In applications that do not make use of the local wake-up feature, local wake-up should be disabled and the WAKE pin should be connected to GND to ensure optimal EMI performance.

5.3.2 Remote Wake-up Pattern (WUP) According to ISO 11898-2:2024 (Partial Networking Disabled)

If the CAN transceiver is in TRX Standby mode and CAN bus wake-up is enabled (CWUE = 1), but CAN selective wake-up is disabled (CPNE = 0 or PNCFOK = 0), the device will monitor the bus for a wake-up pattern as specified in ISO 11898-2:2024.

This filtering helps avoid spurious wake-up events, which could be triggered, for example, by a dominant clamped bus or by dominant phases due to noise, spikes on the bus, transients or EMI.

The wake-up pattern consists of two dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bits in between the above mentioned phases that are shorter in duration than t_{Filter} are ignored.

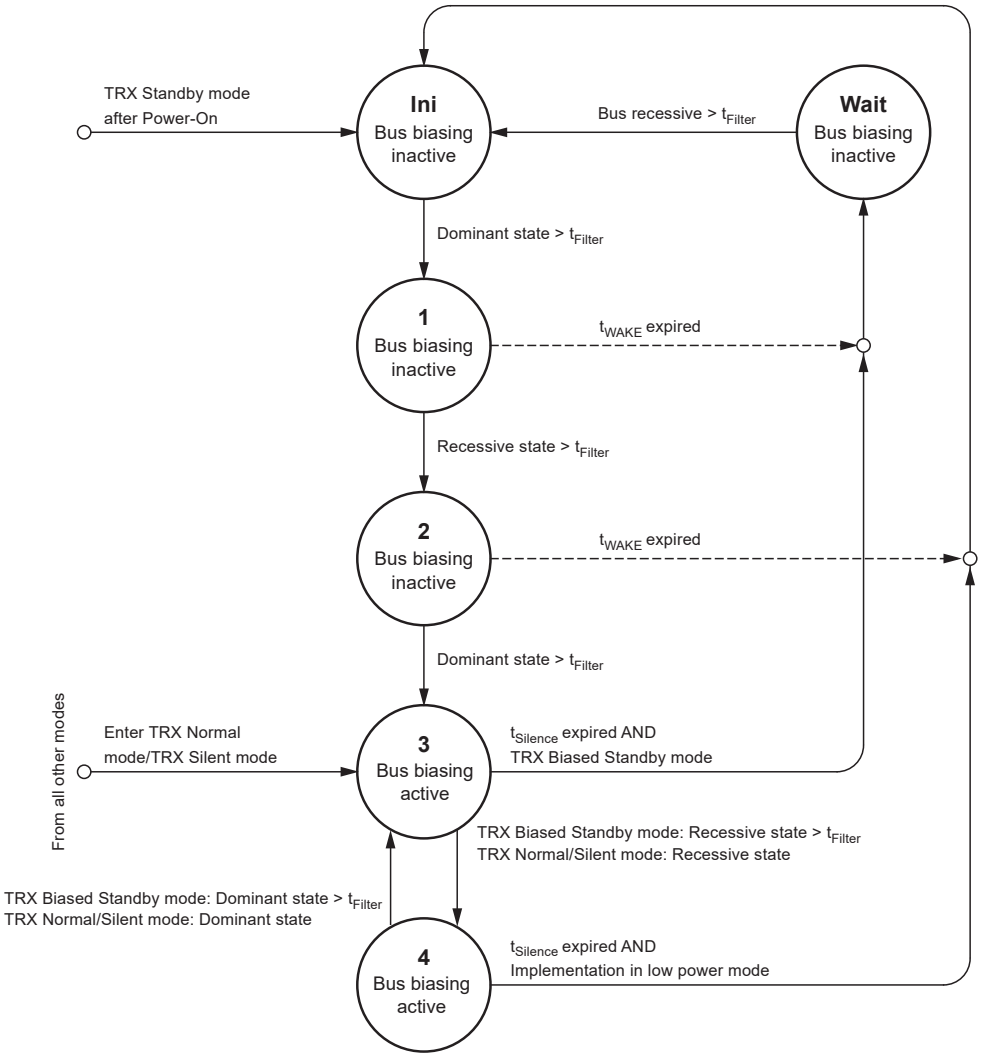
The complete dominant-recessive-dominant pattern, as shown in Figure 5-3, must be received within t_{Wake} to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event.

When a valid CAN WUP is detected on the bus, the wake-up bit CWUS in the Transceiver Event Status register is set (see section TRXESR), and the RXD pin driven low. If the device is in Sleep mode when the wake-up event is detected, it will switch the INH pin to VS to activate external voltage regulators (e.g., for supplying VCC and VIO) and enter Standby mode.

CAN wake-up via WUP can only be disabled via bit CWUE. If CWUE is set to '0', no remote wake-up via the CAN bus is possible. If CWUE is set to '1' and selective wake-up is disabled, the device will switch to Standby mode after detecting the Wake-up Pattern (WUP) coming from Sleep mode. If CWUE is set to '1' and the selective wake-up is enabled, the device will first switch on the bus biasing after detecting the WUP and will only switch to Standby mode afterward, when it detects a valid WUF (please refer to section CAN Selective Wake-up for WUF).

Figure 5-4 illustrates the control of the bus biasing and the WUP detection.

Figure 5-4. WUP Detection and Bias Control



5.3.3 Remote Wake-up Frame (WUF) According to ISO 11898-2:2024

5.3.3.1 CAN Selective Wake-up

Partial networking makes it possible for a CAN node or a CAN sub-network to be woken up individually by means of dedicated and predefined frames, the so-called Wake-up Frames (WUF). When a particular node's tasks are not required, it is in selective Sleep mode.

The transceiver monitors the bus for dedicated CAN wake-up frames when both CAN wake-up (CWUE = 1) and CAN selective wake-up (CPNE = 1) are enabled, and the Partial Networking registers are configured correctly (PNCFOK = 1). An accurate oscillator and a low-power, high-speed comparator are activated to correctly detect wake-up frames.

According to ISO11898-2, a wake-up frame is a CAN frame consisting of an Identifier field (ID), a Data Length Code (DLC), a data field (optional) and a Cyclic Redundancy Check (CRC) code, including the CRC delimiter.

The wake-up CAN frame (ID and data) is fully configurable via the related registers for configuring CAN partial networking. A Standard (11-bit) or Extended (29-bit) Identifier for the wake-up frame format can be selected via the IDE bit in the Frame Control register, CFCR (see section CFCR).

The WUF ID is configured in the ID registers (see sections CIDR0 to CIDR3). ID bits can be masked using the ID mask (see sections CIDMR0 to CIDMR3), where a '1' means 'don't care'.

A single wake-up frame can wake up multiple groups of nodes by comparing the incoming data field with the data mask, as the data field indicates which nodes are to be woken up. Groups of nodes can be predefined and associated with bits in a data mask.

The number of data bytes expected in the data field of a CAN wake-up frame is set with the Data Length Code (bits DLC in the Frame Control register in section CFCR). If DLC ≠ 0000 (one or more data bytes expected), at least one bit in the data field of the received wake-up frame must be set to '1' and at least one corresponding bit in the associated Data Mask register in the transceiver (register for data mask to be defined) must also be set to '1' for a successful wake-up. Each matching pair of logic '1's indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

If DLC = 0000, a node will wake-up if the WUF contains a valid identifier and the received data length code is '0000', regardless of the values stored in the data mask. If DLC ≠ 0000 and all data mask bits are set to '0', the device cannot be woken up via the CAN bus (note that all data mask bits are '1' by default). If a WUF contains a valid ID but the DLCs (in the Frame Control register and in the WUF) do not match, the data field is ignored and no nodes will be woken up. The Data Length Code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0 (see section CFCR), only the identifier field is evaluated to determine if the frame contains a valid wake-up frame. If PNDM = 1 (the default value), the data field is included as part of the wake-up filtering.

When PNDM = 0, a valid wake-up frame is detected and a wake-up event is captured (and CWUS is set to '1') when:

- The identifier field in the received wake-up frame matches the pattern in the ID registers after filtering **AND**
- The CRC field in the received frame (including a recessive CRC delimiter) was received without error.

When PNDM = 1, a valid wake-up frame is detected when:

- The identifier field in the received wake-up frame matches the pattern in the ID registers after filtering **AND**
- The frame is not a remote frame **AND**
- The Data Length Code in the received frame matches the configured Data Length Code (bits DLC) **AND**
- If the Data Length Code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated Data Mask register is also set **AND**
- The CRC field in the received frame (including a recessive CRC delimiter) was received without error.

The internal error counter will be incremented when an erroneous CAN frame (e.g., a stuffing error) is received prior to the ACK field. If a CAN frame is received without any errors preceding the ACK field, the counter will be decremented. Any data received after the CRC delimiter and before the next SOF will be ignored by the partial networking module. If the counter overflows (FEC > ERRCNT, see section EFCR), a frame detect error is captured (PNEFD = 1, see section TRXESR) and the device wakes up; the counter is reset to 0 when the bias is switched off.

After configuring the PN registers, the microcontroller must set the PNCFOK bit to '1'. The device will clear the PNCFOK bit after a write access to any of the CAN Partial Networking Configuration registers (see sections DRCR to CDMR0..7).

Any valid wake-up pattern (according to ISO 11898-2:2024) will trigger a wake-up event if selective wake-up is disabled (CPNE = 0), or partial networking is not configured correctly (PNCFOK = 0), and the CAN transceiver is in TXD Standby mode with wake-up enabled (CWUE = 1).

All wake-up patterns will be ignored if the CAN transceiver is in CAN Normal/Silent mode or CAN wake-up is disabled (CWUE = 0).

5.3.3.2 CAN Selective Wake-up and CAN FD

CAN Flexible Data-Rate (CAN FD) is an improved CAN protocol with regard to bandwidth and payload. As specified in ISO 11898-1:2024, CAN FD is based on the CAN protocol and still uses the same arbitration method. However, after the arbitration phase, the data rate is increased and the data bits are transferred with a higher bit rate than in the arbitration phase. At the CRC delimiter, before the controllers transmit the Acknowledge bits, the bit rate is switched back to the same bit rate as used in the arbitration phase. Besides the increased bit speed, the new CAN FD allows data frames up to 64 bytes compared to the maximum of 8 bytes with classical CAN.

The ATA6574 can be configured to recognize CAN FD frames as valid frames. When CFDPE = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The device remains in Sleep mode with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the device ignores further bus signals until Idle is detected again.

When CFDPE is set to '0', CAN FD frames are interpreted as frames with errors by the partial networking module. Therefore, the error counter is incremented when a CAN FD frame is received. The PNEFD bit is set to '1' and the device wakes up if the error counter overflows.

5.3.4 Wake-up via SPI

In case of an SPI command while the system is in a low-power mode, but with the SPI interface enabled, the device will be woken up and will enter the operating mode issued together with the SPI command. An SPI command failure, such as an invalid length of an SPI command or write access to a read-only register, etc., will also trigger an interrupt event on the device (see Wake-Up Events).

5.3.5 Related Registers for Configuring the CAN Partial Networking

5.3.5.1 Data Rate Configuration Register (Address 0x26)

Name: DRCR
Offset: 0x26
Reset: 0x05
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					DR[2:0]		
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	1

Bits 7:3 – Reserved[4:0] Reserved for future use

Bits 2:0 – DR[2:0] Select CAN Data-Rate

DR[2:0]	CAN Data Rate (Kbit/s)
3'b000	50
3'b001	100
3'b010	125
3'b011	250
3'b100	Reserved (intended for future use; currently selects 500 Kbit/s)
3'b101	500
3'b110	Reserved (intended for future use; currently selects 500 Kbit/s)
3'b111	1000

5.3.5.2 CAN ID Register 0 (Address 0x27)

Name: CIDR0
Offset: 0x27
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	ID0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ID0[7:0]
ID07 to ID00 Bits of the Extended Frame Format

5.3.5.3 CAN ID Register 1 (Address 0x28)

Name: CIDR1
Offset: 0x28
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	ID1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ID1[7:0]
ID15 to ID08 Bits of the Extended Frame Format

5.3.5.4 CAN ID Register 2 (Address 0x29)

Name: CIDR2
Offset: 0x29
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	ID2[7:2]						ID2[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – ID2[7:2]
ID23 to ID18 Bits of the Extended Frame Format; ID05 to ID00 Bits of the Standard Frame Format

Bits 1:0 – ID2[1:0]
ID17 to ID16 Bits of the Extended Frame Format

5.3.5.5 CAN ID Register 3 (Address 0x2A)

Name: CIDR3
Offset: 0x2A
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[7:5]			ID3[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[7:5] Reserved for future use

Bits 4:0 – ID3[4:0]
ID28 to ID24 Bits of the Extended Frame Format, ID10 to ID06 Bits of the Standard Frame Format

5.3.5.6 CAN ID Mask Register 0 (Address 0x2B)

Name: CIDMR0
Offset: 0x2B
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	IDM0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – IDM0[7:0]
Mask Bits ID07 to ID00 of the Extended Frame Format. ‘1’ means ‘don’t care’.

5.3.5.7 CAN ID Mask Register 1 (Address 0x2C)

Name: CIDMR1
Offset: 0x2C
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	IDM1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – IDM1[7:0]
Mask Bits ID15 to ID08 of the Extended Frame Format. ‘1’ means ‘don’t care’.

5.3.5.8 CAN ID Mask Register 2 (Address 0x2D)

Name: CIDMR2
Offset: 0x2D
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	IDM2[7:2]						IDM2[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – IDM2[7:2]
Mask Bits ID23 to ID18 of the Extended Frame Format; ID05 to ID00 Bits of the Standard Frame Format. '1' means 'don't care'.

Bits 1:0 – IDM2[1:0]
Mask Bits ID17 to ID16 of the Extended Frame Format. '1' means 'don't care'.

5.3.5.9 CAN ID Mask Register 3 (Address 0x2E)

Name: CIDMR3
Offset: 0x2E
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[7:5]			IDM3[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[7:5] Reserved for future use

Bits 4:0 – IDM3[4:0]
Mask Bits ID28 to ID24 of the Extended Frame Format, ID10 to ID06 Bits of the Standard Frame Format. '1' means 'don't care'.

5.3.5.10 CAN Frame Configuration Register (Address 0x2F)

Name: CFCR
Offset: 0x2F
Reset: 0x40
Property:

Bit	7	6	5	4	3	2	1	0
	IDE	PNDM	Reserved[1:0]		DLC[3:0]			
Access	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

Bit 7 – IDE Identifier Format
The host microcontroller should set the bit to '1' if identifier is in extended frame format (29-bit), set to '0' if identifier is in standard frame format (11-bit).

Bit 6 – PNDM Partial Networking Data Mask
The host microcontroller should set the bit to '1' if Data Length Code and data field are evaluated at wake-up, set to '0' if Data Length Code and data field are 'don't care' at wake-up.

Bits 5:4 – Reserved[1:0] Reserved for future use

Bits 3:0 – DLC[3:0] Data Length Configuration Select number of data bytes expected in a CAN frame.

DLC[3:0]	Number of Data Bytes
4'b0000	0
4'b0001	1
4'b0010	2
4'b0011	3
4'b0100	4
4'b0101	5
4'b0110	6
4'b0111	7
4'b1000	8
4'b1001 to 4'b1111	Tolerated, 8 bytes expected; DM0 (Data Mask 0) ignored

5.3.5.11 Error Frame Counter Threshold Register (Address 0x3A)

Name: EFCR
Offset: 0x3A
Reset: 0x1F
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[7:5]			EERCNT[4:0]				
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

Bits 7:5 – Reserved[7:5] Reserved for future use

Bits 4:0 – EERCNT[4:0]
Set the Error Frame Counter Overflow Threshold. If the counter overflows (counter > ERRCNT), a frame detect error is captured (PNEFD = 1) and the device wakes up.

5.3.5.12 Failure Error Counter Register (Address 0x3B)

Name: FECR
Offset: 0x3B
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[7:5]			FEC[4:0]				
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[7:5] Reserved for future use

Bits 4:0 – FEC[4:0]
If the device receives a CAN frame containing errors (e.g., a stuffing error) that are received in advance of the ACK field, an internal error counter is incremented. If a CAN frame is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (FEC > ERRCNT, see section EFCR), a frame detect error is captured (PNEFD = 1, see section TRXESR) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

5.3.5.13 Glitch Filter Threshold Register (Address 0x67)

Name: GLFT
Offset: 0x67
Reset: 0x02

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					GLF[2:0]		
Access	R	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bits 7:3 – Reserved[4:0] Reserved for future use

Bits 2:0 – GLF[2:0]
Set the glitch filter threshold from 5% to 55% of the arbitration bit rate.

GLF[2:0]	#samples (≤ 500 Kbit/s)	#samples (1 Mbit/s)
3'b000	1 [<2.42%/<5.17%]	1 [<4.83%/<10.35%]]
3'b001	2 [<4.83%/<7.76%]	2 [<9.66%/<15.52%]
3'b010	3 [<7.25%/<10.35%]	3 [<14.49%/<20.7%]]
3'b011	4 [<9.66%/<12.94%]	4 [<19.32%/<20.87%]
3'b100	5 [<12.08%/<15.52%]	5 [<24.15%/<31.05%]
3'b101	6 [<14.49%/<18.11%]	6 [<28.99%/<36.22%]
3'b110	7 [<16.91%/<20.7%]	7 [<33.82%/<41.40%]
3'b111	24 [<57.97%/<64.69%]	13 [<62.8%/<72.45%]

Assumption: clock tolerance ±3%; transmitter ±0.5% tolerance.

5.3.5.14 CAN Data Mask Registers 0...7 (Address 0x68...0x6F)

Name: CDMR0..7
Offset: 0x68...0x6F
Reset: 0xFF

Bit	7	6	5	4	3	2	1	0
	DM0...7[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – DM0...7[7:0] data mask 0...7 configuration

Table 5-2. Data Mask and the CAN Data Filed

Type	DLC										
CAN Frame	DLC > 8	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC
Data Mask	__	DLC	00	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 8	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	CRC
Data Mask	__	DLC	DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 7	__	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	CRC
Data Mask	__	__	DLC	DM1	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 6	__	__	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	CRC
Data Mask	__	__	__	DLC	DM2	DM3	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 5	__	__	__	DLC	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	CRC
Data Mask	__	__	__	__	DLC	DM3	DM4	DM5	DM6	DM7	CRC

.....continued

Type	DLC										
CAN Frame	DLC = 4	__	__	__	__	DLC	Byte 0	Byte 1	Byte 2	Byte 3	CRC
Data Mask	__	__	__	__	__	DLC	DM4	DM5	DM6	DM7	CRC
CAN Frame	DLC = 3	__	__	__	__	__	DLC	Byte 0	Byte 1	Byte 2	CRC
Data Mask	__	__	__	__	__	__	DLC	DM5	DM6	DM7	CRC
CAN Frame	DLC = 2	__	__	__	__	__	__	DLC	Byte 0	Byte 1	CRC
Data Mask	__	__	__	__	__	__	__	DLC	DM6	DM7	CRC
CAN Frame	DLC = 1	__	__	__	__	__	__	__	DLC	Byte 0	CRC
Data Mask	__	__	__	__	__	__	__	__	DLC	DM7	CRC

5.3.5.15 Bus Failure Event Capture Enable Register (Address 0x32)

Name: BFECR
Offset: 0x32
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[7:2]						BOUTE	BSCE
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[7:2] Reserved for future use

Bit 1 – BOUTE Bus Dominant Time-out Event Capture Enable
The BOUTE bit must be set to '1' to enable the bus dominant time-out detection. Setting the bit to '0' disables the bus dominant time-out detection.

Bit 0 – BSCE Bus Short-Circuit Event Capture Enable
The BSCE bit must be set to '1' to enable the bus short-circuit event detection. Setting the bit to '0' disables the bus short-circuit event detection.

5.3.5.16 Pin WAKE Status Register (Address 0x4B)

Name: PWKS
Offset: 0x4B
Reset: 0x00
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	Reserved[7:2]						PWKVS	Reserved
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[7:2] Reserved for future use

Bit 1 – PWKVS Pin WAKE Voltage Status
The device sets the bit to '1' if WAKE is high, to '0' if WAKE is low. PWKVS is always '0' in Power-Down mode if local wake-up is disabled.

Bit 0 – Reserved Reserved for future use

5.3.5.17 Global Event Status Register (Address 0x60)

Name: GESR
Offset: 0x60
Reset: 0x01
Property: Read-only

Bit	7	6	5	4	3	2	1	0
	OSCS	Reserved	BFES	Reserved	WKES	TRXES	Reserved	SYSES
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Bit 7 – OSCS System Oscillator Status
The device sets the bit to '1' if a hardware failure of the system oscillator is detected and sets the bit to '0' when the system oscillator is disabled for power-saving purposes, the hardware failure is resolved, or the oscillator is enabled (for instance, in device Normal mode) and no hardware failure is present.

Bit 6 – Reserved Reserved for future use

Bit 5 – BFES Bus Failure Event Status
The device sets the bit to '1' if there is a bus failure event pending (any bit in the BFESR register is '1'). The bit reads '0' if all status bits in the BFESR register are cleared.

Bit 4 – Reserved Reserved for future use

Bit 3 – WKES WAKE Event Status
The device sets the bit to '1' if there is a WAKE pin event pending (any bit in the WKESR register is '1'). The bit reads '0' if all status bits in the WKESR register are cleared.

Bit 2 – TRXES Transceiver Event Status
The device sets the bit to '1' if there is a transceiver event pending (any bit in the TRXESR register is '1'). The bit reads '0' if all status bits in the TRXESR register are cleared.

Bit 1 – Reserved Reserved for future use

Bit 0 – SYSES SYSES System Event Status
The device sets the bit to '1' if there is a system event pending (any bit in the SESR register is '1'). The bit reads '0' if all status bits in the SESR register are cleared.

5.3.5.18 System Event Status Register (Address 0x61)

Name: SESR
Offset: 0x61
Reset: 0x10
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			PWRONS	Reserved	OTPW	SPIFS	Reserved
Access	R	R	R	R/W	R	R/W	R/W	R
Reset	0	0	0	1	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bit 4 – PWRONS Power-on Status

The device sets the bit to '1' if the device has left Power-Off mode after power on. The bit can be reset to '0' by writing a '1' to the bit. PWRONS is also cleared when the device is forced into Sleep mode due to an undervoltage event. The information stored in PWRONS could be lost in this case. The NMTS bit in the Device Mode Status Register (DMSR) can be used in this case. The NMTS bit is set to '0' when the device switches to Normal mode after power on.

Bit 3 – Reserved Reserved for future use

Bit 2 – OTPW Overtemperature Prewarning Status

The device sets the bit to '1' if the event is enabled in the SECR register and the chip temperature has exceeded the overtemperature prewarning threshold. The bit can be reset to '0' by writing a '1' to the bit. OTPW is also cleared when the device is forced into Sleep mode due to an undervoltage event.

Bit 1 – SPIFS SPI Failure Status

The device sets the bit to '1' if the event is enabled in the SECR register and an SPI failure is detected. The bit can be reset to '0' by writing a '1' to the bit. SPIFS is also cleared when the device is forced into Sleep mode due to an undervoltage event.

Bit 0 – Reserved Reserved for future use

5.3.5.19 Transceiver Event Status Register (Address 0x63)

Name: TRXESR
Offset: 0x63
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[7:6]		PNEFD	BS	Reserved[3:2]		TRXF	CWUS
Access	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:6 – Reserved[7:6] For future use

Bit 5 – PNEFD Partial Networking Frame Detection Status

The device sets the bit to '1' if a partial networking frame detection error is detected (error counter overflow). The bit can be reset to '0' by writing a '1' to the bit. PNEFD is also cleared when the device is forced into Sleep mode due to an undervoltage event.

Bit 4 – BS Bus Status

The device sets the bit to '1' if the event is enabled in the TRXECR register and no activity on the CAN bus is detected for $t_{Silence}$. The bit can be reset to '0' by writing a '1' to the bit. BS is also cleared when the device is forced into Sleep mode due to an undervoltage event.

Bits 3:2 – Reserved[3:2] For future use

Bit 1 – TRXF Transceiver Failure Status

The device sets the bit to '1' if the event is enabled in the TRXECR register and a CAN failure event is detected. The bit can be reset to '0' by writing a '1' to the bit. TRXF is also cleared when the device is forced into Sleep mode due to an undervoltage event. TRXF is triggered if:

- TXD is clamped dominant and system is in TRX Normal mode.

- A VCC undervoltage is detected, COPM = 01 and system is in TRX Normal or TRX Reduced Normal mode.
- An RXD recessive clamping error is detected and system is in TRX Normal or TRX Silent mode. The RXD recessive clamping error detection must be individually enabled in the TRXECR2 register.

Bit 0 – CWUS CAN Wake-up Status

The device sets the bit to '1' if the event is enabled in the TRXECR register and a CAN wake-up event is detected. The bit can be reset to '0' by writing a '1' to the bit. CWUS is also cleared when the device is forced into Sleep mode due to an undervoltage event.

5.3.5.20 WAKE Event Status Register (Address 0x64)

Name: WKESR
Offset: 0x64
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[7:2]						LWURS	LWUFS
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[7:2] Reserved for future use

Bit 1 – LWURS Local Wake-up Rising Edge Status

The device sets the bit to '1' if the event detection is enabled in the WKECR register and a rising edge on the WAKE pin is detected. The bit can be reset to '0' by writing a '1' to the bit. LWURS is also cleared when the device is forced into Sleep mode due to an undervoltage event.

Bit 0 – LWUFS Local Wake-up Falling Edge Status

The device sets the bit to '1' if the event detection is enabled in the WKECR register and a falling edge on the WAKE pin is detected. The bit can be reset to '0' by writing a '1' to the bit. LWUFS is also cleared when the device is forced into Sleep mode due to an undervoltage event.

5.3.5.21 Bus Failure Event Indication Status Register (Address 0x65)

Name: BFESR
Offset: 0x65
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved[5:0]						BOUTS	BSCS
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[5:0] Reserved for future use

Bit 1 – BOUTS Bus Dominant Time-out Event Status

The device sets the bit to '1' if a bus dominant time-out event is detected. The bit is set to '0' by writing '1' to the bit via SPI.

Bit 0 – BSCS Device Bus Short-Circuit Event Status
The device sets the bit to '1' if a bus short-circuit event is detected. The bit is set to '0' by writing '1' to the bit via SPI.

5.3.5.22 System Event Capture Enable Register (Address 0x04)

Name: SECR
Offset: 0x04
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[4:0]					OTPWE	SPIFE	Reserved
Access	R	R	R	R	R	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0

Bits 7:3 – Reserved[4:0] Reserved for future use

Bit 2 – OTPWE Overtemperature Prewarning Event Capture
The OTPWE bit must be set to '1' to enable the overtemperature prewarning detection. Setting the bit to '0' disables the overtemperature prewarning detection.

Bit 1 – SPIFE SPI Failure Event Capture
The SPIFE bit must be set to '1' to enable the SPI failure detection. Setting the bit to '0' disables the SPI failure detection.

Bit 0 – Reserved Reserved for future use

5.3.5.23 Transceiver Event Capture Enable Register (Address 0x23)

Name: TRXECR
Offset: 0x23
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[2:0]			BSE	Reserved[1:0]		TRXFE	CWUE
Access	R	R	R	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – Reserved[2:0] Reserved for future use

Bit 4 – BSE BSE Bus Status Capture Enable
The BSE bit must be set to '1' to enable the CAN bus silence detection. Setting the bit to '0' disables the CAN bus silence detection.

Bits 3:2 – Reserved[1:0] Reserved for future use

Bit 1 – TRXFE Transceiver Failure Status Capture Enable
The TRXFE bit must be set to '1' to enable the CAN failure detection. Setting the bit to '0' disables the CAN failure detection.

Bit 0 – CWUE CAN Bus Wake-up Detection Enable
The CWUE bit must be set to '1' to enable the CAN wake-up detection. Setting the bit to '0' disables the CAN wake-up detection. At an undervoltage event, the bit is set to '1' automatically.

5.3.5.24 Transceiver Event Capture Enable Register 2 (Address 0x34)

Name: TRXECR2
Offset: 0x34
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[6:0]							RXDRCE
Access	R	R	R	R	R	R	R	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:1 – Reserved[6:0] Reserved for future use

Bit 0 – RXDRCE RXD Recessive Clamping Capture Enable
The RXDRCE bit must be set to '1' to enable the RXD recessive clamping detection. Setting the bit to '0' disables the RXD recessive clamping detection.

5.3.5.25 WAKE Event Capture Enable Register (Address 0x4C)

Name: WKECR
Offset: 0x4C
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	Reserved[7:2]						LWURE	LWUFE
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:2 – Reserved[7:2] Reserved for future use

Bit 1 – LWURE
The bit must be set to '1' to enable the WAKE pin rising edge detection interrupt. Setting the bit to '0' disables the interrupt. The LWURE bit is set automatically before Sleep mode is activated due to an undervoltage event.

Bit 0 – LWUFE
The bit must be set to '1' to enable the WAKE pin falling edge detection interrupt. Setting the bit to '0' disables the interrupt. The LWUFE bit is set automatically before Sleep mode is activated due to an undervoltage event.

5.4 Fail-Safe Features

5.4.1 TXD Dominant Time-out Function

A TXD dominant time-out timer is started when the TXD pin is set to low and the transceiver is in TRX Normal mode. If the low state on the TXD pin persists for longer than $t_{to(dom)}$, the transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high. The TXD dominant time-out time also defines the minimum possible bit rate of 4 Kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated (TRXF = 1; see section TRXESR), if enabled (TRXFE = 1; see section TRXECR). In addition, the status of the TXD dominant time-out can be read via the TXDOUT bit in the Transceiver Status register (see section

TRXSR), and the TXS bit is set to '0'. TXDOUT is reset to '0' and TXS is set to '1' when the TXD pin is set to high again.

5.4.2 TXD-to-RXD Short-Circuit Detection

When a short circuit appears between the RXD and TXD pins, the bus will be locked into a permanent dominant state due to the low-side driver of the RXD pin typically being stronger than the high-side driver of the connected microcontroller to TXD. To prevent such lock-ups, the implemented TXD-to-RXD short-circuit detection disables the transmitter. The TXD dominant time-out timer is used to detect this failure (refer to section TXD Dominant Time-out Function for the behavior in this case). The TXD dominant time-out timer is activated when the transceiver is in TRX Normal mode and the TXD pin is low.

5.4.3 Bus Dominant Clamping Detection

A CAN bus short circuit (to VS, VCC or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The bus dominant time-out timer is activated when the transceiver is in the TRX Normal mode, the TXD pin is high and the bus is dominant. The timer for detecting the bus dominant clamping failure will be reset by any signal change at the TXD pin or on the CAN bus. When the bus dominant clamping is detected and the failure detection is enabled (BOUTE = 1; see section BFECR), the bits BOUT and BOUTS are set to '1' by the device, and a bus failure interrupt is generated (BFES = 1; see section GESR). The BOUT bit is reset to '0' as soon as the bus state is changed to recessive again. The status of the bus dominant clamping detection can be read via the BOUT bit in the Bus Status register (see section BFIR).

5.4.4 Bus Recessive Clamping Detection

The bus failure flag (BSC = 1; see section BFIR) is set if the failure detection is enabled (BSCE = 1; see section BFECR) when the device detects a CAN bus recessive clamping for $t_{bus\_rec\_clamp}$. In case a bus recessive clamping is detected, the BSC and BSCS bits are set to '1' and a bus failure interrupt is generated (BFES = 1; see section GESR). The status of the bus recessive clamping failure can be read via the BSC bit in the Bus Status register. The BSC bit is reset to '0' as soon as the bus state changes to dominant again.

5.4.5 Internal Pull-up Structure of the TXD Input Pin

The TXD pin has an internal pull-up structure to VIO. This ensures a safe, defined state in case the pin is left floating. The pull-up current flows into the pin in all states; therefore, the pin should be in a high state during TRX Standby mode to minimize the current consumption.

5.4.6 Undervoltage Detection on Pin VCC

An enabled CAN failure interrupt is generated (TRXF = 1) when the CAN transceiver supply voltage, V_{VCC}, falls below the undervoltage detection threshold ($V_{VCC\_UV\_Set}$), provided COPM = 01. In addition, status bit VCCS is set to '1' (see section DMSR). The VCCS bit only reflects the correct status while the device is in Normal or Standby mode.

5.4.7 Short-Circuit Protection of the Bus Pins

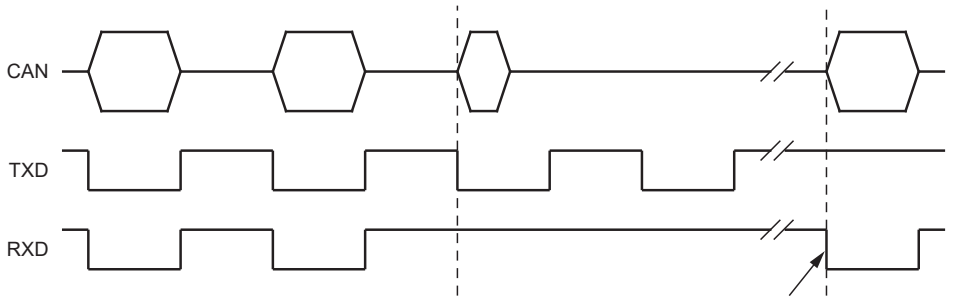
The CANH and CANL bus outputs are short-circuit protected against GND and against positive supply voltages (V_{VS}, V_{VCC}). A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

5.4.8 RXD Recessive Clamping

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped too high (e.g., recessive). If the RXD pin cannot signalize a dominant bus condition, e.g., because it

is shorted to VCC, the transmitter is disabled to avoid possible data collisions on the bus. In TRX Normal mode and TRX Silent mode, the device continuously compares the state of the High-Speed Comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than $t_{RXD\_rec\_clmp}$ without the RXD pin doing the same, a recessive clamping situation is detected.

Figure 5-5. RXD Recessive Clamping Detection



A CAN transceiver failure interrupt (not denoted at the RXD pin) is generated (TRXF = 1; see section TRXESR), if enabled (TRXFE = 1 and RXDRCE = 1; see section TRXECR and section TRXECR2). In addition, the status of the RXD recessive clamping failure can be read via the RXDRCS bit in the Status register (see section TRXESR2), and the TXS bit is set to '0'. The RXD recessive clamping detection is reset by either entering Sleep, Standby or Unpowered mode, or when the RXD pin shows dominant again.

5.4.9 Overtemperature Detection

The device provides two levels of overtemperature protection. In the case that the chip temperature rises above the Overtemperature Protection Prewarning Threshold ($T > T_{OT\_Prew}$), the device will set the status bit OTPWS = 1. If the overtemperature prewarning event capture is enabled (OTPWE = 1), COPM is set to '00' (and DOPM is set to '111') , and an overtemperature prewarning interrupt will be generated (OTPW = 1). If DOPM is set to '111' but COPM is not set to '00', and the overtemperature prewarning event capture is enabled (OTPWE = 1), only the overtemperature prewarning flag will be set (OTPW = 1) and no interrupt will be generated. The device will enter the Overtemp mode when the chip temperature rises above the Overtemperature Protection Shutdown Threshold (T_{Jsd}). In the Overtemp mode, the CAN transceiver is switched to the TRX Off mode. The transmitter and the receiver are both disabled and the CAN pins are highly resistive. No wake-up event will be detected. A pending wake-up will still be signaled by a low level on pin RXD.

5.4.10 Loss of Power at VS Pin

In case of a power loss on the VS pin, the CAN bus and the I/O pins are tri-stated. No reverse currents will flow from the bus into the device.

5.4.11 Wake-up and Interrupt Event Diagnosis via RXD Pin

Wake-up and interrupt event signaling provide status information to the microcontroller. The information is stored in the Event Status registers (see sections SESR to BFESR) and is signaled on the RXD pin, if enabled.

The device provides a mechanism which indicates to the microcontroller that a wake-up has occurred. This mechanism works continuously after power on of the device.

The device sets the internal wake-up flags (CWUS, LWURS and LWUFS see section TRXESR and section WKESR) if a valid wake-up event occurs. The device signals a wake-up to the microcontroller as follows:

1. RXD pin = low, if V_{VS} and V_{VIO} are present.
2. INH pin = active, if only V_{VS} is present.

A distinction is made between regular wake-up events (see Table 5-3) and interrupt events (see Table 5-4). At least one regular wake-up source must be enabled before the device can transition to Sleep mode.

Table 5-3. Wake-up Events

Symbol	Event	Power On	Description
CWUS	CAN Bus Wake-up	Disabled	A CAN wake-up event was detected.
LWURS	Rising Edge on WAKE Pin	Disabled	A rising-edge wake-up was detected on the WAKE pin.
LWUFS	Falling Edge on WAKE Pin	Disabled	A falling-edge wake-up was detected on the WAKE pin.

Table 5-4. Interrupt Events

Symbol	Event	Power On	Description
PWRONS	Device Power On	Always enabled	The device has exited Power-Off mode (after battery power has been restored/connected).
OTPW	Overtemperature Prewarning	Disabled	The device temperature has exceeded the overtemperature warning threshold (only in Normal mode).
SPIFS	SPI Failure	Disabled	SPI clock count error (only 16, 24 and 32-bit commands are valid), illegal DOPM code or attempted write access to locked register (not in Sleep mode).
PNEFD	Partial Networking Frame Detection Error	Always enabled	Partial networking frame detection error counter overflow.
BS	CAN Bus Silence	Disabled	No activity on CAN bus for $t_{Silence}$.
TRXF	CAN Transceiver Failure	Disabled	One of the following CAN failure events detected (not in Sleep mode): • TXD dominant clamping detected (TXD dominant time-out detected). • CAN transceiver deactivated due to a V_{VCC} undervoltage event (if COPM = 01, $V_{VCC} < V_{VCC\_UV\_Set}$). • CAN transceiver recessive clamping error detected (TRX Normal or Silent mode only).
BOUTS	Bus Dominant Time-out Failure	Disabled	Bus is detected as dominant for $t > t_{BUS\_dom}$ (not in Sleep mode).
BSCS	Bus Short-Circuit (recessive time-out) Failure	Disabled	The device detects a CAN bus recessive clamping on first occurrance of dominant recessive cycle (not in Sleep mode).

PWRONS and PNEFD system events are always captured. The detection of other wake-up and interrupt events can be enabled/disabled individually using the event capture enable registers (see section SECR to section WKECR).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in TRX Standby mode, the RXD pin (if VIO is applied) is forced low to indicate that a wake-up or interrupt event has been detected. If the device is in Sleep mode when the event occurs, the INH pin is forced high and the device switches to Standby mode. If VIO is applied, the RXD pin is forced low. If the device is in Standby mode when the event occurs, the RXD pin is forced low to flag an interrupt/wake-up event. The detection of any enabled wake-up or

interrupt event will trigger a wake-up in Standby or Sleep mode. (Please refer to Table 5-1 for an overview on the RXD pin in different operating modes).

The microcontroller can monitor events via the Event Status registers. An extra status register, the Event Summary Status register (see section GESR) is provided to help speed up software polling routines. By polling the Global Event Status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant register.

After the event source has been identified, the status bit should be cleared (set to '0') by writing '1' to the relevant bit (writing '0' will have no effect). A number of status bits can be cleared in a single write operation by writing '1' to all relevant bits. It is strongly recommended to clear only the status bits that were set to '1' when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

5.4.12 Interrupt Event/Wake-up Event Delay

Frequent interrupt or wake-up events while the transceiver is in CAN TRX Standby mode can require significant microcontroller processing time because the RXD pin is driven low each time an interrupt/wake-up is generated. Therefore, the device incorporates an interrupt/wake-up delay timer to limit the frequency of wake-up events.

When one of the event capture status bits is cleared, the RXD pin is released (high) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after td(event), the RXD pin goes low again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process multiple events, rather than for each individual event. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d\_evt\_cap}$, the RXD pin remains high (since there are no pending events). The Event Capture registers can be read at any time.

5.4.13 Sleep Mode Protection

It is very important that event detection is configured correctly when the device switches to Sleep mode to ensure it will respond to a wake-up event. To ensure that the device wakes up from Sleep mode, at least one regular wake-up event must be enabled, and all event status bits must be cleared before the device transitions to Sleep mode. Otherwise, the device will transition to Standby mode in response to a Go-to-Sleep command (DOPM = Sleep).

5.5 Device ID

A byte is reserved at address 0x7E for a device identification code.

5.5.1 Device ID Register (Address 0x7E)

Name: DIDR
Offset: 0x7E
Reset: 0x74
Property: Read-only

The register provides the ID of the ATA6574.

Bit	7	6	5	4	3	2	1	0
	DID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	1	1	1	0	1	0	0

Bits 7:0 – DID[7:0]
The device ID is 0x74 for ATA6574.

5.6 Lock Control Register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this feature only protects locked bits from being modified via the SPI and will not prevent the device from updating status registers.

5.6.1 Register Write Protection Register (Address 0x0A)

Name: RWPR
Offset: 0x0A
Reset: 0x00
Property:

Bit	7	6	5	4	3	2	1	0
	Reserved	WP6	WP5	WP4	WP3	WP2	WP1	WP0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – Reserved For future use

Bit 6 – WP6
Address Area 0x67 to 0x6F Partial Networking Data Byte registers; the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

Bit 5 – WP5
Address Area 0x50 to 0x5F; the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

Bit 4 – WP4
Address Area 0x40 to 0x4F WAKE pin configuration; the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

Bit 3 – WP3
Address Area 0x30 to 0x3F; the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

Bit 2 – WP2
Address Area 0x20 to 0x2F transceiver control and partial networking; the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

Bit 1 – WP1
Address Area 0x10 to 0x1F; the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

Bit 0 – WP0
Address Area 0x06 to 0x09: the external microcontroller should set the bit to '1' to enable register write protection and set to '0' to disable it.

5.7 Window Watchdog

The watchdog is used to monitor the proper function of the microcontroller and to trigger a Reset if the microcontroller stops serving the watchdog due to a lock-up in the software or any malfunction. Since this device does not have a Reset output pin, the microcontroller Reset is triggered via the INH pin. The device enters Microcontroller Reset mode and switches off the INH pin. This causes

the supply voltage of the microcontroller to ramp down, resulting in a Power-on Reset (POR) of the microcontroller.

The Window Watchdog (WWD) in the ATA6574 is, by default, deactivated and should be enabled by the microcontroller. The watchdog supports two operating modes: Window mode (only available in device Normal mode, see Figure 5-6) and Time-out mode (see Figure 5-7). In Window mode, a watchdog trigger event within a closed watchdog window causes a transition to Microcontroller Reset mode. In Time-out mode, the watchdog can be triggered at any time within the trigger range by a watchdog trigger. In Time-out mode, the watchdog can also be used for cyclic wake-up of the microcontroller.

Figure 5-6. Window Watchdog in Window Mode

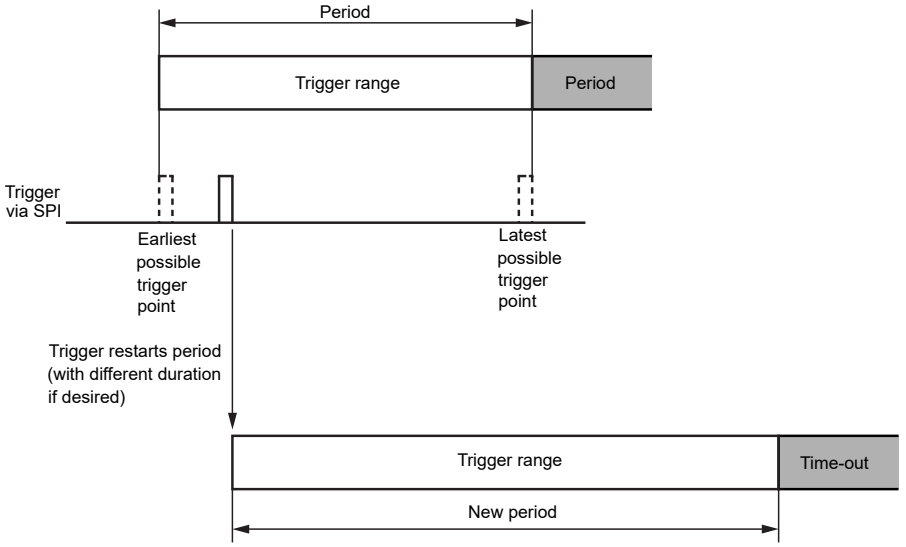
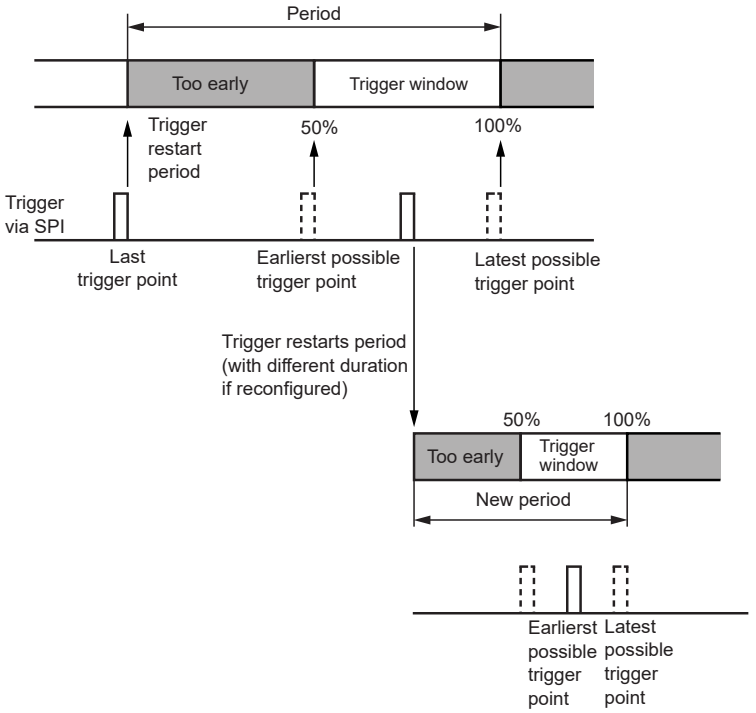


Figure 5-7. Window Watchdog in Time-out Mode



In order to avoid unwanted configuration of the watchdog, the ATA6574 only allows configuration of the watchdog (write access to WDCR1 register and WDCR2, see Table 5-5 and Table 5-6) when the device is in Standby mode. If the WWD is deactivated, the microcontroller shall configure the WWD correctly before the WWD is enabled (WDC = 010/100). As soon as the WWD is activated, the watchdog runs with the latest configuration. If the WWD is active, the microcontroller is allowed to configure the WWD any time when the device is in Standby mode. Every write access to the WDCR1 and WDCR2 registers via SPI will reset the Watchdog Timer and immediately apply the changes. If Window mode is selected (WDC = 100), the watchdog will remain in (or switch to) Time-out mode until the device enters Normal mode (Window mode is only supported when the device is in Normal mode).

Any attempt to configure the watchdog (write access to WDCR1 register and WDCR2 register, see Table 5-5 and Table 5-6) while the device is not in Standby mode will deactivate the inhibit switch, and the device will set the ILLCONF bit in the Watchdog Status register, WDSR (illegal watchdog configuration, see Table 5-7). After Reset, the device enters Standby mode.

Table 5-5. Watchdog Configuration Register 1 (WDCR1, 0x36)

Bits	Symbol	Access	Value	Description
7:5	WDC	R/W		Watchdog mode control
			001	Off mode (default)
			010	Time-out mode
			100	Window mode

.....continued				
Bits	**Symbol**	**Access**	**Value**	**Description**
4:3	WDPRE	R/W		Watchdog period control (extend watchdog period by prescaling with the factor below)
			00	Watchdog prescale factor 1 (default)
			01	Watchdog prescale factor 1.5
			10	Watchdog prescale factor 2.5
			11	Watchdog prescale factor 3.5
2	WDSLP	R/W		Set to '1' to let the window watchdog run in Sleep mode; otherwise, set to '0'; set to '0' by default.
1	WDLW	R/W		Set to '1' if a Reset to Window Watchdog Timer and a long open window exist after INH switch to high; otherwise, set to '0'; set to '1' by default.
0	ADCH	R/W		Enable (1) and disable (0) active discharger of external voltage regulator via VIO pin; by default, set to '0'.

Eight watchdog periods (8 ms to 4096 ms) are supported in the ATA6574. The watchdog period is programmable via the Watchdog Period bits (WWDP) in the Watchdog Configuration Register 2 (WDCR2). The selected period is valid for both Window and Time-out modes. The default watchdog period is 128 ms. A watchdog trigger event (an SPI write access to WDTRIG register with the pattern '01010101') resets the Watchdog Timer. The watchdog period and the reset pulse width can also be configured via the WRPL bits in the Watchdog Configuration Register 2. A window watchdog active discharger is integrated in the ATA6574 to ensure a predictable reset of the external microcontroller. In the ATA6574, if the WWD active discharger is activated (ADCH = 1), the discharger will draw a minimum of 2 mA discharging current from the VIO pin when a microcontroller Reset is triggered by the window watchdog.

To keep the watchdog active when the device is in Sleep mode, the WDSLP bit of the WWD Control register must be set to '1'. When the device goes into Sleep mode with WDSLP = 1, the Watchdog Timer gets reset and restarts immediately. When the device goes into Sleep mode with WDSLP = 0, the Watchdog Timer gets reset immediately, but it restarts only at the next INH low-to-high transition (entering Long Window mode if the mode is enabled).

Table 5-6. Watchdog Configuration Register 2 (WDCR2, 0x37)

Bits	Symbol	Access	Value	Description
7:4	WWDP	R/W		Window watchdog period configuration (ms, prescale factor = 1, ±10%)
			1000	8
			0001	16
			0010	32
			1011	64
			0100	128 (default)
			1101	256
			1110	1024
			0111	4096

.....continued				
Bits	Symbol	Access	Value	Description
0:3	WRPL	R/W		Window Watchdog Reset pulse length (ms)
			1000	1 to 1.5
			0001	3.6 to 5 (default)
			0010	10 to 12.5
			1011	20 to 25
			0100	40 to 50
			1101	60 to 75
			1110	100 to 125
			0111	150 to 190

The watchdog is an important safety mechanism that must be configured correctly. Two mechanisms are provided to prevent watchdog parameters from being changed by mistake:

- All configuration bitfields in the registers WDC, WWDP and WRPL have a Hamming distance of at least two for valid states;
- Reconfiguration protection: Only configurable in Standby mode.

Having a Hamming distance of at least two for all valid states for the control bitfields, WDC, WWDP and WRPL, ensures that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be flipped to reconfigure WDC, WWDP or WRPL). If an attempt is made to write an invalid code to the WDCR1 register or WDCR2 register, the SPI write to the WDCRx register is ignored and the CACC bit in the Watchdog Status register is set.

After the device transitions from µC Reset mode to Standby mode, the microcontroller should trigger the watchdog prior to writing to a watchdog configuration register.

Table 5-7. Watchdog Status Register (WDSR, 0x38h)

Bits	Symbol	Access	Description
7	OFF	R	Window watchdog is off
6	CACC	R/W	Corrupted write access to the Window Watchdog Configuration registers
5	ILLCONF	R/W	An attempt is made to reconfigure the Watchdog Control register while the device is not in Standby mode.
4	TRIGS	R	The device sets the bit to '1' if the window watchdog is in the first half of window and sets the bit to '0' if the window watchdog is in second half of the window. If the WWD is not in Window mode, the bit will always be set to '0'.
3	OF	R/W	Watchdog overflow (Time-out mode or Window mode in Standby or Normal mode)
2	OFSLP	R/W	Watchdog overflow in Sleep mode (Time-out mode)
1	ETRIG	R/W	Watchdog triggered too early (Window mode)
0	-	R	

Writing '1' to the corresponding bit of the Watchdog Status register will reset the bit.

A transition to microcontroller Reset mode is triggered immediately in response to an illegal watchdog configuration (configuration of the watchdog in Normal or Sleep mode), an incorrect watchdog trigger event in Window mode (watchdog overflow or triggered too early) or when the watchdog overflows in Time-out mode. If a Reset is triggered by the window watchdog, the Window Watchdog Reset Event register will be set. The device will enter the Microcontroller Reset mode and enter Standby mode after the Reset is finished.

If there is a corrupted write access to the Window Watchdog Configuration registers and/or an illegal configuration of the Watchdog Configuration register when the watchdog is in Off mode, the corresponding status register bit will be set. If the register bits are not reset to zero before enabling the window watchdog, a Reset will be triggered to the microcontroller immediately after enabling the window watchdog.

5.7.1 Watchdog Trigger Register (Address 0x39)

Name: WDTRIG
Offset: 0x39
Reset: 0x00
Property: Write-only

Bit	7	6	5	4	3	2	1	0
	WDTRIG[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – WDTRIG[7:0]
A watchdog trigger event (an SPI write access to WDTRIG register with the pattern 01010101) resets the Watchdog Timer.

5.7.2 Watchdog Behavior in Window Mode

The watchdog runs continuously in Window mode. The watchdog will be in Window mode if WDC = `100` and the device enters the Normal mode. In Window mode, the watchdog must only be triggered during the second half of the watchdog period. If the watchdog overflows or is triggered in the first half of the watchdog period (defined by WWDP in WDCR2 in Table 5-6), a Reset is performed after the device enters the Microcontroller Reset mode. The INH output switches off for a defined length. The Reset source (either 'watchdog triggered too early' or 'watchdog overflow') is captured in the watchdog status bits in the Watchdog Status register (WDSR). If the watchdog is triggered in the second half of the watchdog period, the Watchdog Timer is restarted.

5.7.3 Watchdog Behavior in Time-out Mode

The watchdog runs continuously in Time-out mode. The watchdog will be in Time-out mode if WDC = `010`. In Time-out mode, the Watchdog Timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event is captured in the Watchdog Status register (WDSR). In Time-out mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the ATA6574 is in Sleep mode. When the device is in Sleep mode with Watchdog Time-out mode selected, a wake-up event is generated after the nominal Watchdog Period (WWDP). The device switches to the Microcontroller Reset mode.

5.7.4 Watchdog Behavior During Power On and After Microcontroller Reset

After the watchdog has been activated, it starts a long open window (600 ms to 650 ms started from when INH is high). Within this long open window, the watchdog must be triggered by the microcontroller. Otherwise, the watchdog will transition to microcontroller Reset mode. After the first trigger within the long open window, the WWD starts its normal operating modes.

If the WDLW bit from the Window Watchdog Configuration register is set to '`1`' (default value), the Watchdog Timer will always be reset after INH is switched on and starts the long open window. Otherwise, the WWD will continue its normal operating modes.

5.7.5 Watchdog During VIO Undervoltage and Overtemperature

If the device detects a VIO undervoltage, it will transition to Sleep mode and stop and reset the window watchdog. The device will only restart the window watchdog when it leaves Sleep mode,

even if WDSLP = 1.
The window watchdog is stopped if the device enters Overtemperature mode. The watchdog is reset and restarts when the device enters Standby mode.

5.8 General Purpose Memory (GPMn)

The device allocates 4 bytes of RAM as general purpose registers for storing user information. The general purpose registers can be accessed via the SPI at addresses 0x06 to 0x09.

5.8.1 General Purpose Memory 0 (Address 0x06)

Name: GPM0
Offset: 0x06
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	GPM0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM0[7:0] General Purpose Memory Bits

5.8.2 General Purpose Memory 1 (Address 0x07)

Name: GPM1
Offset: 0x07
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	GPM1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM1[7:0]
General Purpose Memory Bits

5.8.3 General Purpose Memory 2 (Address 0x08)

Name: GPM2
Offset: 0x08
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	GPM2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM2[7:0]
General Purpose Memory Bits

5.8.4 General Purpose Memory 3 (Address 0x09)

Name: GPM3
Offset: 0x09
Reset: 0x00

Bit	7	6	5	4	3	2	1	0
	GPM3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – GPM3[7:0]
General Purpose Memory Bits

5.9 VIO Supply Pin

The VIO pin should be connected to the microcontroller supply voltage. This will adjust the signal levels of the TXD, RXD and the SPI interface pins to the I/O levels of the microcontroller, enabling direct interfacing without the need for level shifters.

5.10 VCC/VIO Undervoltage Protection

If an undervoltage is detected on the VCC or VIO pins, and it remains valid for longer than the Undervoltage Detection Delay Time, $t_{VSUP\_UV\_filter}$, the device transitions to Sleep mode after $t_{UV2Sleep}$ (see Figure 5-1). The following preventative measures are taken before the device transitions to Sleep mode to avoid deadlock and unpredictable states:

- All previously captured events (address ranges: 0x61 to 0x65) are cleared before the device switches to Sleep mode to avoid repeated attempts to wake-up while an undervoltage is present.
- Both CAN remote wake-up (CWUE = 1) and local wake-up via the WAKE pin (LWUFE = LWURE = 1) are enabled to ensure that the device can be woken up after entering Sleep mode.
- Partial networking is disabled (CPNE = 0) to ensure immediate wake-up in response to bus traffic after the device has recovered from an undervoltage event.
- The Partial Networking Configuration bit is cleared (PNCFOK = 0) to indicate that partial networking might not have been configured correctly when the device switched to Sleep mode.

Status bit SMTS is set to '1' when a transition to Sleep mode was caused by an undervoltage event (see DMSR). This bit indicates that the settings of the wake-up source should be reconfigured (CWUE, LWUFE, LWURE and CPNE).

5.11 Serial Peripheral Interface (SPI)

5.11.1 General

The SPI-interface is used to communicate with a microcontroller. The ATA6574 is configured and operated using SPI transfers.

The SPI allows full-duplex data transfer. Status information is returned when new control data are shifted in. The interface also offers read-only access, allowing registers to be read back without changing the register content.

Bits are sampled on the falling edge of the clock and data are shifted in/out on the rising edge, as illustrated in Figure 5-8.

Figure 5-8. SPI Timing Protocol

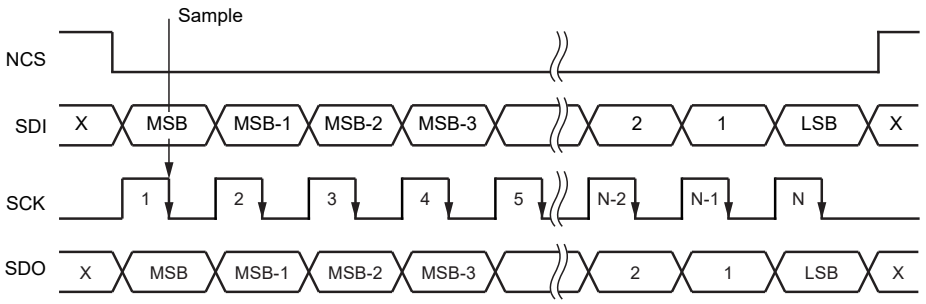
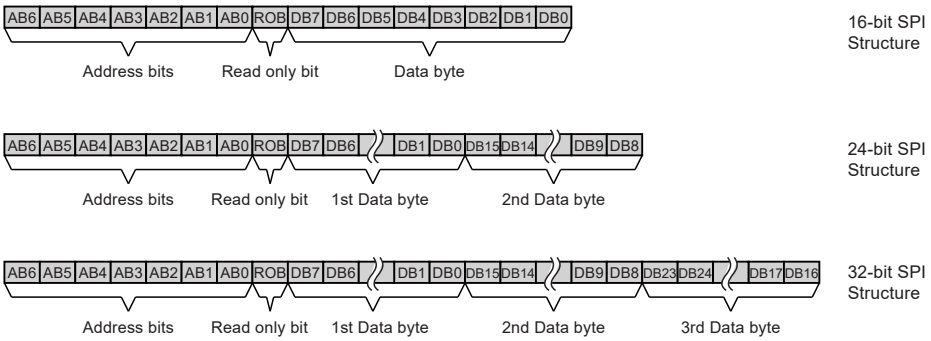


Figure 5-9. SPI Data Structure



The SPI data is stored in dedicated 8-bit registers, and each register is assigned a unique 7-bit address. 16 bits must be transmitted to the device for a single register write operation. The first byte contains the 7-bit address, along with a 'read-only' bit (the LSB). The read-only bit must be '0' to indicate a write operation. If this bit is '1', a read operation is performed and any data after this bit are ignored. The second byte contains the data to be written to the register. The contents of the addressed register(s) are returned via the SDO pin, while a read or write operation is performed. For faster programming, 24 and 32-bit read and write operations are also supported. In this case, the register address is automatically incremented: once for a 24-bit operation and twice for a 32-bit operation.

Attempting to write to non-existing registers is not prohibited; if the available address space is exceeded during a write operation, the data above the valid address range are ignored (without generating an SPI failure event).

The number of the transmitted SPI bits is always monitored during SPI transfers, and if the number of bits does not equal 16, 24 or 32, the write operation is aborted. An SPI failure event is captured (SPIF = 1) if the SPI failure detection is enabled (SPIFE = 1) and the following SPI failure is detected:

1. SPI clock count error (only 16, 24 and 32-bit commands are valid), both read and write operations.
2. Illegal DOPM code.
3. Attempted write access to locked register.

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is looped back on SDO from bit 33 onwards.

5.11.2 Register Summary

The ATA6574 contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in the table below. Undocumented registers and bits are reserved for future use. Reserved bits should be written to 0 unless otherwise stated.

Addr.	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device control registers									
0x01	DMCR	-	-	-	-	-	DOPM[2:0]		
0x03	DMSR	SMTS	OTPWS	NMTS	-	-	-	-	-
0x04	SECR	-	-	-	-	-	OTPWE	SPIFE	-
0x06	GPM0	GPM0[7:0]							
0x07	GPM1	GPM1[7:0]							
0x08	GPM2	GPM2[7:0]							
0x09	GPM3	GPM3[7:0]							
0x0A	RWPR	-	WP6	WP5	WP4	WP3	WP2	WP1	WP0
TRX control registers									
0x20	TRXCR	-	CFDPE	PNCFOK	CPNE	-	-	COPM[1:0]	
0x22	TRXSR	TXS	PNERRS	PNCFS	PNOSCS	CBSS	-	VCCS	TXDOUT
0x23	TRXECR	-	-	-	BSE	-	-	TRXFE	CWUE
0x26	DRCR	-	-	-	-	DR[3:0]			
0x27	CIDR0	ID0[7:0]							
0x28	CIDR1	ID1[7:0]							
0x29	CIDR2	ID2[7:0]							
0x2A	CIDR3	-	-	-	ID3[4:0]				
0x2B	CIDMR0	IDM0[7:0]							
0x2C	CIDMR1	IDM1[7:0]							
0x2D	CIDMR2	IDM2[7:0]							
0x2E	CIDMR3	-	-	-	IDM3[4:0]				
0x2F	CFCR	IDE	PNDM	-	-	DLC[3:0]			
0x32	BFECR	-	-	-	-	-	-	BOUTE	BSCE
0x33	BFIR	-	-	-	-	-	-	BOUT	BSC
0x34	TRXECR2	-	-	-	-	-	-	-	RXDRCE
0x35	TRXESR2	-	-	-	-	-	-	-	RXDRCS
0x36	WDCR1	WDC[2:0]			WDPRE[1:0]		WDSLP	WDLW	ADCH
0x37	WDCR2	WWDP[3:0]				WRPL[3:0]			
0x38	WDSR	OFF	CACC	ILLCONF	TRIGS	OF	OFSLP	ETRIG	-
0x39	WDTRIG	WDTRIG[7:0]							
0x3A	EFCR	ERRCNT[4:0]							
0x3B	FECR	FEC[4:0]							
0x67	GLF	GLF[2:0]							
0x68	CDMR0	DM0[7:0]							
0x69	CDMR1	DM1[7:0]							
0x6A	CDMR2	DM2[7:0]							
0x6B	CDMR3	DM3[7:0]							
0x6C	CDMR4	DM4[7:0]							
0x6D	CDMR5	DM5[7:0]							
0x6E	CDMR6	DM6[7:0]							
0x6F	CDMR7	DM7[7:0]							

.....continued

Addr.	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WAKE control and status registers									
0x4B	PWKS	-	-	-	-	-	-	PWKVS	-
0x4C	WKECR	-	-	-	-	-	-	LWURE	LWUFE
Event status registers									
0x60	GESR	OSCS	-	BFES	-	WKES	TRXES	-	SYSES
0x61	SESR	-	-	-	PWRONS	-	OTPW	SPIFS	-
0x63		-	-	PNEFD	BS	-	-	TRXF	CWUS
0x64	WKESR	-	-	-	-	-	-	LWURS	LWUFS
0x65		-	-	-	-	-	-	BOUTS	BSCS
Device ID register									
0x7E	DIDR	DIDR[7:0]							

5.11.3 Operating Modes and Register Bit Settings

When switching from one operating mode to another, a number of register bits change their state automatically. This happens when the device switches to Power-Off mode or when the device is forced to Sleep mode because of an undervoltage event. These changes are summarized in the table below. SPI mode change commands are ignored during state changes (automatic mode changes have priority).

Register Bit	Power Off	Standby	Normal	Sleep	Overtemp	Forced Sleep (UV)
BS	0	No change	No change	No change	No change	0
BSE	0	No change	No change	No change	No change	No change
CBSS	1	Actual state	Actual state	Actual state	Actual state	Actual state
DR	101	No change	No change	No change	No change	No change
TRXF	0	No change	No change	No change	No change	0
CFDPE	1	No change	No change	No change	No change	No change
TRXFE	0	No change	No change	No change	No change	No change
TXDOUT	0	Actual state	Actual state	Actual state	Actual state	Actual state
COPM	01	No change	No change	No change	No change	No change
PNOSCS	0	Actual state	Actual state	Actual state	Actual state	Actual state
CPNE	0	No change	No change	No change	No change	0
PNERRS	1	Actual state	Actual state	Actual state	Actual state	Actual state
PNCFS	0	Actual state	Actual state	Actual state	Actual state	Actual state
TXS	0	0	Actual state	0	0	0
CWUS	0	No change	No change	No change	No change	0
CWUE	0	No change	No change	No change	No change	1
DMn	11111111	No change	No change	No change	No change	No change
DLC	0000	No change	No change	No change	No change	No change
SMTS	0	No change	No change	0	No change	1
GPMn	00000000	No change	No change	No change	No change	No change
IDn	00000000	No change	No change	No change	No change	No change
IDE	0	No change	No change	No change	No change	No change
DIDR	01110000	01110000	01110000	01110000	01110000	01110000
WPn	0	No change	No change	No change	No change	No change
IDMn	00000000	No change	No change	No change	No change	No change
DOPM	100	100	111	001	Don't care	001

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Register Bit	Power Off	Standby	Normal	Sleep	Overtemp	Forced Sleep (UV)
NMTS	1	No change	0	No change	No change	No change
OTPW	0	No change	No change	No change	No change	0
OTPWE	0	No change	No change	No change	No change	No change
OTPWS	0	Actual state	Actual state	Actual state	Actual state	Actual state
PNCFOK	0	No change	No change	No change	No change	0
PNDM	1	No change	No change	No change	No change	No change
PNEFD	0	No change	No change	No change	No change	0
PWRONS	1	No change	No change	No change	No change	0
SPIFS	0	No change	No change	No change	No change	0
SPIFE	0	No change	No change	No change	No change	No change
SYSES	1	No change	No change	No change	No change	0
TRXES	0	No change	No change	No change	No change	0
VCCS	0	Actual state	Actual state	0	0	0
OSCS	0	No change	No change	No change	No change	No change
BFES	0	No change	No change	No change	No change	0
WKES	0	No change	No change	No change	No change	0
LWUFS	0	No change	No change	No change	No change	0
LWURS	0	No change	No change	No change	No change	0
LWUFE	0	No change	No change	No change	No change	1
LWURE	0	No change	No change	No change	No change	0
LWURE	0	No change	No change	No change	No change	1
PWKVS	0	No change	No change	No change	No change	No change
GLF	010	No change	No change	No change	No change	No change
RXDRCS	0	No change	No change	No change	No change	No change
RXDRCE	0	No change	No change	No change	No change	No change
BOUTE	0	No change	No change	No change	No change	No change
BSCE	0	No change	No change	No change	No change	No change
BOUTS	0	No change	No change	No change	No change	0
BSCS	0	No change	No change	No change	No change	0

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions, beyond those indicated in the DC/AC Characteristics of this data sheet, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter(s)	Symbol	Min.	Max.	Unit
CANH, CANL				
DC Voltage	V_{CANH}, V_{CANL}	-27	+40	V
Transient Voltage according to IEC 62228-3 ref. ISO 7637-2		-150	+100	V
Maximum Differential Bus Voltage	V_{Diff}	-40	+40	V
DC Voltage on Pins TXD, RXD, SDO, SDI, NCS, SCK, VCC, VIO	V_x	-0.3	+5.5	V
DC Voltage on Pin VS	V_{VS}	-0.3	+40	V
DC Voltage on Pin INH, WAKE	V_{INH}, V_{WAKE}	-0.3	+40	V
ESD according to IBEE CAN EMC Test Specification Following IEC 62228, IEC 61000-4-2: - Pin CANH, CANL		±6		kV
ESD according to IBEE CAN EMC Test Specification Following IEC 62228, IEC 61000-4-2: - Pin VS, WAKE to GND		±15		kV
HBM JESD22-A114/AEC-Q100-002 - Pins CANH, CANL to GND - Pins VS, WAKE to GND		±8 ±4		kV
HBM JESD22-A114/AEC-Q100-002 - All pins		±2		kV
Charge Device Model ESD AEC-Q100-011		±750		V
Machine Model ESD AEC-Q100-003		±100		V
Storage Temperature	T_{stg}	-55	+150	°C
Virtual Junction Temperature	T_{vJ}	-40	+175	°C

6.2 DC/AC Characteristics

All parameters valid for 4.5V ≤ V_{VS} ≤ 28V, 4.7V ≤ V_{VCC} ≤ 5.5V, 2.8V ≤ V_{VIO} ≤ 5.5V, all voltages are defined with respect to ground, $R_{(CANH-CANL)}$ = 60Ω, Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C, T_{vJ} ≤ +170°C, typical values are given at V_{VS} = 13V, T_{amb} = +25°C, unless otherwise noted.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
VS									
0.10	Supply Voltage Threshold for Power-On Detection	V_{VS} rising	VS	V_{VS_PWRON}	4.0		4.5	V	A
0.20	Supply Voltage Threshold for Power-Off Detection	V_{VS} falling	VS	V_{VS_PWROFF}	2.8		3.1	V	A
0.30	Supply Voltage Threshold for CAN TRX Undervoltage Detection Release	V_{VS} rising	VS	$V_{VS\_UV\_CAN\_Clear}$	4.5		5	V	A
0.40	Supply Voltage Threshold for CAN TRX Undervoltage Detection	V_{VS} falling	VS	$V_{VS\_UV\_CAN\_Set}$	4.0		4.5	V	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
0.50	VS Supply Current	Sleep mode, DOPM = Sleep, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V	VS	I_{VS_Sleep}		16	30	µA	A
0.501		Sleep mode, DOPM = Sleep, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V, T_{amb} = +85°C	VS	I_{VS_Sleep}		18		µA	C
0.502		Sleep mode, DOPM = Sleep, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V, T_{amb} = +125°C	VS	I_{VS_Sleep}		21		µA	C
0.503		Sleep mode, DOPM = Sleep, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V, T_{amb} = +150°C	VS	I_{VS_Sleep}		24		µA	C
0.51		Standby mode, DOPM = Standby, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V	VS	I_{VS_Stb}		18	40	µA	A
0.511		Standby mode, DOPM = Standby, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V, T_{amb} = +85°C	VS	I_{VS_Stb}		20		µA	C
0.512		Standby mode, DOPM = Standby, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V, T_{amb} = +125°C	VS	I_{VS_Stb}		23		µA	C
0.513		Standby mode, DOPM = Standby, CWUE = 1, CAN TRX Standby mode, V_{VS} = 7V to 18V, T_{amb} = +150°C	VS	I_{VS_Stb}		26		µA	C
0.52		Additional current in Sleep/ Standby mode with bus biasing on, V_{VS} = 7V to 18V	VS	I_{VS_Bias}		112	140	µA	A
0.521		Additional current in Sleep/ Standby mode with bus biasing on, V_{VS} = 7V to 18V, T_{amb} = +85°C	VS	I_{VS_Bias}		120		µA	C
0.522		Additional current in Sleep/ Standby mode with bus biasing on, V_{VS} = 7V to 18V, T_{amb} = +125°C	VS	I_{VS_Bias}		124		µA	C
0.523		Additional current in Sleep/ Standby mode with bus biasing on, V_{VS} = 7V to 18V, T_{amb} = +150°C	VS	I_{VS_Bias}		127		µA	C
0.53		Additional current when partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V	VS	ΔI_{VS_Pn}		310	350	µA	A
0.531		Additional current when partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V, T_{amb} = +85°C	VS	ΔI_{VS_Pn}		310		µA	C
0.532		Additional current when partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V, T_{amb} = +125°C	VS	ΔI_{VS_Pn}		310		µA	C
0.533		Additional current when partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V, T_{amb} = +150°C	VS	ΔI_{VS_Pn}		310		µA	C
0.55		Normal mode, TRX Normal mode, partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V	VS	I_{VS_Norm}		1	1.5	mA	A
0.551		Normal mode, TRX Normal mode, partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V, T_{amb} = +85°C	VS	I_{VS_Norm}			1	mA	C
0.552		Normal mode, TRX Normal mode, partial networking enabled, bus active, CPNE = 1, PNCFOK = 1, V_{VS} = 7V to 18V, T_{amb} = +125°C	VS	I_{VS_Norm}			1	mA	C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
VCC									
1.10	VCC Undervoltage Detection Set Threshold	V_{VCC} falling	VCC	$V_{VCC\_UV\_Set}$	3.7		4.25	V	A
1.20	VCC TX Undervoltage Shutdown Threshold	V_{VCC} falling	VCC	$V_{VCC\_TX\_Sd}$	4.0		4.7	V	A
1.30	VCC Supply Current	CAN TRX Normal mode, CAN recessive, $V_{TXD} = V_{VIO}$	VCC	I_{VCC_Norm}			2.5	mA	A
1.31		Device Standby/Normal mode and CAN TRX Standby mode	VCC	I_{VCC_Stb}			4	µA	A
1.32		Device Sleep mode and CAN TRX Standby mode	VCC	I_{VCC_Sleep}			4	µA	A
1.40	Supply Current in Normal Mode	Dominant, V_{TXD} = 0V	VCC	I_{VCC_dom}	30	50	70	mA	A
1.41	Supply Current in Normal Mode	Short between CANH and CANL	VCC	I_{VCC_short}			85	mA	B
VIO									
2.10	VIO Undervoltage Detection Set Threshold	V_{VIO} falling	VIO	$V_{VIO\_UV\_Set}$	2.4		2.8	V	A
2.20	VIO Supply Current	Standby/Normal, TXD = 1	VIO	I_{VIO_Stb}			5	µA	A
2.21	VIO Supply Current	Sleep, TXD = 1, Tamb ≤ +125°C	VIO	I_{VIO_Sleep}			5	µA	A
2.30	Active Discharge Current	VIO = 0.5V	VIO	I_{VIO_Disch}	2			mA	C
SDI, SCK, NCS									
3.10	High-Level Input Voltage		SDI, SCK, NCS	V_{SDI_H}, V_{SCK_H}, V_{NCS_H}	0.7 × V_{VIO}		V_{VIO} + 0.3	V	A
3.20	Low-Level Input Voltage		SDI, SCK, NCS	V_{SDI_L}, V_{SCK_L}, V_{NCS_L}	-0.3		0.3 × V_{VIO}	V	A
3.30	Input Current		SDI	I_{I_SDI}	-5		+5	µA	A
3.40	Pull-up Resistance on Pin NCS		NCS	R_{PU_NCS}	40	60	80	kΩ	A
3.50	Pull-Down Resistance on Pin SCK		SCK	R_{PD_SCK}	40	60	80	kΩ	A
SDO, RXD									
4.10	High-Level Output Voltage	I = -4 mA	SDO, RXD	V_{SDO_H}, V_{RXD_H}	V_{VIO} – 0.4		V_{VIO}	V	A
4.20	Low-Level Output Voltage	I = 4 mA	SDO, RXD	V_{SDO_L}, V_{RXD_L}			0.4	V	A
4.40	OFF State Leakage Current		SDO	I_{leak_SDO}	-5		+5	µA	A
TXD									
5.10	High-Level Input Voltage		TXD	V_{TXD_H}	0.7 × V_{VIO}		V_{VIO} + 0.3	V	A
5.20	Low-Level Input Voltage		TXD	V_{TXD_L}	-0.3		0.3 × V_{VIO}	V	A
5.30	Pull-up Resistor		TXD	R_{PU_TXD}	40	60	80	kΩ	A
WAKE									
6.10	High-Level Input Current	V_{WAKE} = 4.2V, V_{VS} ≥ 5.2V	WAKE	I_{WAKE_H}	-10	-5	-1	µA	A
6.20	Low-Level Input Current	V_{WAKE} = 2.3V	WAKE	I_{WAKE_L}	1	5	10	µA	A
6.30	Threshold Voltage	WAKE rising	WAKE	V_{WAKE_TH}	2.8		4.1	V	A
6.31		WAKE falling	WAKE	V_{WAKE_TH}	2.4		3.75	V	A
6.40	Input Hysteresis Voltage		WAKE	V_{hys}	0.25		0.8	V	C
INH									
7.10	On Mode High-Level Voltage	Normal mode or Standby mode, I_{INH} = −180 µA	INH	V_{INH_On}	V_{VS} -0.8		V_{VS}	V	A
7.20	Off Mode Leakage Current	Leakage of grounded INH pin in Off mode	INH	I_{INH_Off}	-2		2	µA	A
CANH, CANL (see the CAN Transceiver Timing Diagram for the definition of R_L and the test circuit)									
8.10	Single-Ended Dominant Output Voltage	R_L = 50Ω to 65Ω	CANH	V_{CANH}	2.75	3.5	4.5	V	B
8.11			CANL	V_{CANL}	0.5	1.5	2.25	V	B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.30	Transmitter Voltage Symmetry	$V_{Sym} = (V_{CANH} + V_{CANL})/V_{CC}$ R_L = 60Ω, C_1 = 4.7 nF f_{TXD} = 1 MHz		V_{Sym}	0.9	1.0	1.1		D
8.40	Bus Differential Output Voltage	CAN TRX Normal mode, V_{TXD} = 0V,t < $t_{to(dom)TXD}$$R_L$ = 50Ω to 65ΩV_{VCC} = 4.7V to 5.5V		V_{Diff}	1.5		3	V	B
8.41		CAN TRX Normal mode, V_{TXD} = 0V,t < $t_{to(dom)TXD}$$R_L$ = 45Ω to 70ΩV_{VCC} = 4.7V to 5.5V		V_{Diff}	1.4		3.2	V	B
8.42		CAN TRX Normal mode, V_{TXD} = 0V,t < $t_{to(dom)TXD}$$R_L$ = 2240 ΩV_{VCC} = 4.7V to 5.5V		V_{Diff}	1.5		5	V	D
8.50	Recessive Output Voltage	Single-ended output voltage on CANH/CANL, CAN TRX Normal mode, V_{VCC} > 4.3V, V_{TXD} = V_{VIO}, no load	CANH, CANL	V_{CANH}, V_{CANL}	2	0.5 × V_{VCC}	3	V	A
8.51		Single-ended output voltage on CANH/CANL, CAN TRX Standby mode, V_{TXD} = V_{VIO}, no load	CANH, CANL	V_{CANH}, V_{CANL}	-0.1		+0.1	V	A
8.52		Single-ended output voltage on CANH/CANL, CAN TRX Biased Standby/TRX Silent mode, V_{TXD} = V_{VIO}, no load	CANH, CANL	V_{CANH}, V_{CANL}	2	2.5	3	V	A
8.53		Differential output voltage (bus biasing active), no load		V_{Diff}	-50		+50	mV	A
8.54		Differential output voltage (bus biasing inactive), no load		V_{Diff}	-50		+50	mV	A
8.60	Differential Receiver Threshold Voltage	CAN TRX Normal/TRX Silent modes, V_{CANL} = V_{CANH} = -12V to +12V		$V_{Diff\_rx\_th}$	0.5	0.7	0.9	V	A
8.61		CAN TRX Standby mode, V_{CANL} = V_{CANH} = -12V to +12V		$V_{Diff\_rx\_th}$	0.4	0.7	1.15	V	A
8.70	Differential Receiver Hysteresis Voltage	CAN TRX Normal/TRX Silent mode, V_{CANL} = V_{CANH} = -12V to +12V		V_{Hys_rx}	50	120	200	mV	C
8.80	Leakage Current	V_{VS} = V_{VCC} = V_{VIO} = 0VV_{CANH} = V_{CANL} = 5 V	CANH, CANL	I_{leak}	-5		+5	µA	A
		VS = VCC = VIO connected to GND with 47 kΩ V_{CANH} = V_{CANL} = 5V	CANH, CANL	I_{leak}	-5		+5	µA	D
8.90	Maximum Driver Output Current	CAN TRX Normal mode; CAN dominant, V_{TXD} = 0, t < $t_{to(dom)TXD}$, V_{VCC} = 5VV_{CANH} = -5V	CANH	I_{CANH_max}	-75		-33	mA	A
8.91	Maximum Driver Output Current	CAN TRX Normal mode, CAN dominant; V_{TXD} = 0, t < $t_{to(dom)}$, V_{VCC} = 5VV_{CANL} = +27V	CANL	I_{CANL_max}	33		75	mA	A
8.100	Single-Ended Input Resistance	V_{CANH} = V_{CANL} = 4V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	A
		−2V ≤ V_{CANH} ≤ 7V−2V ≤ V_{CANL} ≤ 7V	CANH, CANL	R_{CANH}, R_{CANL}	9	15	28	kΩ	D
8.110	Matching of Internal Resistance between CANH and CANL	V_{CANH} = V_{CANL} = 4V mR = 2 × (R_{CANH} − R_{CANL})/(R_{CANH} + R_{CANL})		mR	-0.01		+0.01		A
		-2V ≤ V_{CANH} ≤ 7V -2V ≤ V_{CANL} ≤ 7VmR = 2 × (R_{CANH} − R_{CANL})/(R_{CANH} + R_{CANL})		mR	-0.01		+0.01		D
8.120	Differential Internal Resistance	V_{CANH} = V_{CANL} = 4V		R_{Diff}	18	30	56	kΩ	A
		-2V ≤ V_{CANH} ≤ 7V−2V ≤ V_{CANL} ≤ 7V		R_{Diff}	18	30	56	kΩ	D
8.130	Common-Mode Input Capacitance	f = 500 kHz, CANH and CANL referred to GND		$C_{i(cm)}$			20	pF	D
8.140	Differential Input Capacitance	f = 500 kHz, between CANH and CANL		C_{Diff}			10	pF	D

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.141	Differential Bus Voltage Range for Recessive State Detection	Bus biasing active, Bus biasing inactive -12V ≤ V_{CANH} ≤ +12V -12V ≤ V_{CANL} ≤ +12V		$V_{Diff\_rec\_a}$ $V_{Diff\_rec\_i}$	-3.0 -3.0		+0.5 +0.4	V V	D D
8.142	Differential Bus Voltage Range for Dominant State Detection	Bus biasing active, Bus biasing inactive -12V ≤ V_{CAN_H} ≤ +12V -12V ≤ V_{CAN_L} ≤ +12V		$V_{DIFF\_dom\_a}$ $V_{DIFF\_dom\_i}$	0.9 1.15		8.0 8.0	V V	D D
Transceiver Timing, Pins WAKE, INH, CANH, CANL, TXD and RXD. Refer to the CAN Transceiver Timing Diagrams for the definition of the timing parameters and the test circuit.									
9.10	Delay Time from TXD to Bus Dominant	R_L = 60Ω, C2 = 100 pF	CANH, CANL, TXD	t_{TXDBUS_dom}		65		ns	C
9.20	Delay Time from TXD to Bus Recessive	R_L = 60Ω, C2 = 100 pF	CANH, CANL, TXD	t_{TXDBUS_rec}		90		ns	C
9.30	Delay Time from Bus Dominant to RXD	R_L = 60Ω, C2 = 100 pF	CANH, CANL, RXD	t_{BUSRXD_dom}		60		ns	C
9.40	Delay Time from Bus Recessive to RXD	R_L = 60Ω, C2 = 100 pF	CANH, CANL, RXD	t_{BUSRXD_rec}		65		ns	C
9.50	Propagation Delay from TXD to RXD (the input signal on TXD shall have rise and fall times (10%/90%) of less than 10 ns.) (Time span from signal edge on TXD input to next signal edge with the same polarity on RXD output, the maximum delay of both signal edges is to be considered.)	R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}	40		190	ns	A
9.51		R_L = 150Ω, C2 = 100 pF, C_{RXD} = 15 pF	TXD, RXD	t_{Loop}			300	ns	C
9.60	Received Recessive Bit Time on Pin RXD	t_{B_TXD} = 500 ns, R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	400		550	ns	C
9.61		t_{B_TXD} = 200 ns, R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	120		220	ns	A
9.62		t_{B_TXD} = 125 ns, R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF	RXD	$t_{Bit(RXD)}$	70		140	ns	A
9.70	Receiver Timing Symmetry	$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ t_{B_TXD} = 500 ns (Refer to 9.100 for $t_{Bit(Bus)}$)		Δt_{Rec}	-65		+40	ns	C
9.71		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ t_{B_TXD} = 200 ns (Refer to 9.110 for $t_{Bit(Bus)}$)		Δt_{Rec}	-45		+15	ns	A
9.72		$\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ t_{B_TXD} = 125 ns (Refer to 9.111 for $t_{Bit(Bus)}$)		Δt_{Rec}	-45		+10	ns	A
9.80	TXD Dominant Time-out Time	V_{TXD} = 0V, Normal mode	TXD	$t_{to(dom)}$	2.7		3.3	ms	B
9.90	Bus Dominant Time-out Time	$V_{CANH-CANL}$ > 0.9 V		t_{BUS_dom}	2.7		3.3	ms	B
9.100	Transmitted Recessive Bit Width on the Bus	t_{B_TXD} = 500 ns R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF		$t_{Bit(Bus)}$	435		530	ns	C
9.110		t_{B_TXD} = 200 ns R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF		$t_{Bit(Bus)}$	155		210	ns	A
9.111		t_{B_TXD} = 125 ns R_L = 60Ω, C2 = 100 pF, C_{RXD} = 15 pF		$t_{Bit(Bus)}$	85		140	ns	A

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.120	CAN Activity Filter Time for Standard Remote Wake-up Pattern (WUP)	First pulse (after first recessive) and second pulse for wake-up on pins CANH and CANL, CAN TRX Standby	CANH, CANL	t_{Filter}	0.5		1.8	µs	A
9.130	Bus Bias Reaction Time		CANH, CANL	t_{Bias}			200	µs	C
9.140	Time-out Time for Bus Inactivity	Bus recessive time measurement started in all CAN TRX modes	CANH, CANL	$t_{Silence}$	0.95		1.17	s	B
9.150	CAN Start-up Time	When switching to CAN TRX Normal mode	CANH, CANL	$t_{TRX\_startup}$			220	µs	A
9.160	Event Capture Delay Time	CAN TRX Standby mode	RXD	$t_{d\_evt\_cap}$	0.9		1.1	ms	B
9.180	Delay Time from Bus Wake-up to INH High	Load on INH pin, R_{LOAD} = 10 kΩ	INH	t_{WU_INH}			100	µs	A
9.190	Undervoltage Detection Filter Time		VCC, VIO	$t_{VSUP\_UV\_filter}$	6		54	µs	A
9.200	Delay Time from VIO/VCC Undervoltage Detection to Enter Sleep Mode		VCC, VIO	$t_{UV2Sleep}$	200		400	ms	B
9.210	Start-up Time after Power On	From V_{VS} rises above the power-on detection threshold V_{VS_PWRON} until pin INH high	VS	$t_{startup}$			1	ms	A
9.220	Standard Remote Wake-up Time-out Time	Between first and second dominant pulses, CAN TRX Standby mode		t_{Wake}	900		1200	µs	B
9.230	Debouncing Time for Recessive Clamping State Detection	$V_{(CAN\_H-CAN\_L)}$ > 900 mV, RXD = high	RXD	$t_{RXD\_rec\_clmp}$	60	90	175	ns	D
9.240	Local Wake-up Time		WAKE	t_{local_wu}	5		50	µs	B
9.250	Transmitter Resume Time	From TXD goes high to TX operates after TXD dominant time-out event detected		$t_{TX\_resume\_TXDOUT}$			4	µs	D
9.260	Bus Recessive Clamping Detection Time	Bus recessive clamping time after TXD goes low		$t_{bus\_rec\_clamp}$	1			µs	D
SPI Timing									
10.10	Clock Cycle Time	Normal/Standby/Sleep mode	SPI	t_{clk}	250			ns	D
10.20	SPI Enable Lead Time	Normal/Standby/Sleep mode	SPI	t_{EN_Lead}	50			ns	D
10.30	SPI Enable Lag Time	Normal/Standby/Sleep mode	SPI	t_{EN_Lag}	50			ns	D
10.40	Clock High Time	Normal/Standby/Sleep mode	SPI	t_{Clk_H}	125			ns	D
10.50	Clock Low Time	Normal/Standby/Sleep mode	SPI	t_{Clk_L}	125			ns	D
10.60	Data Input Setup Time	Normal/Standby/Sleep mode	SPI	t_{Setup}	50			ns	D
10.70	Data Input Hold Time	Normal/Standby/Sleep mode	SPI	t_{Hold}	50			ns	D
10.80	Data Output Valid Time	Normal/Standby/Sleep mode	SPI	t_{Dout_v}			65	ns	D
10.90	Chip Select Pulse Width High	Normal/Standby/Sleep mode, pin SDO, C_L = 20 pF	SPI	t_{NCS_pw}	250			ns	D
Temperature Protection									
11.30	Overtemperature Protection Prewarning Threshold			T_{OT_Prew}	120	134	147	°C	B
11.31	Overtemperature Protection Prewarning Hysteresis			$T_{OT\_Prew\_hys}$		10		°C	C

Notes: * Type means:

- A = 100% tested
- B = 100% Tested through indirect testing or calculation
- C = Characterized, not production tested
- D = Simulated, not production tested

Figure 6-1. CAN Transceiver Timing Diagram 1

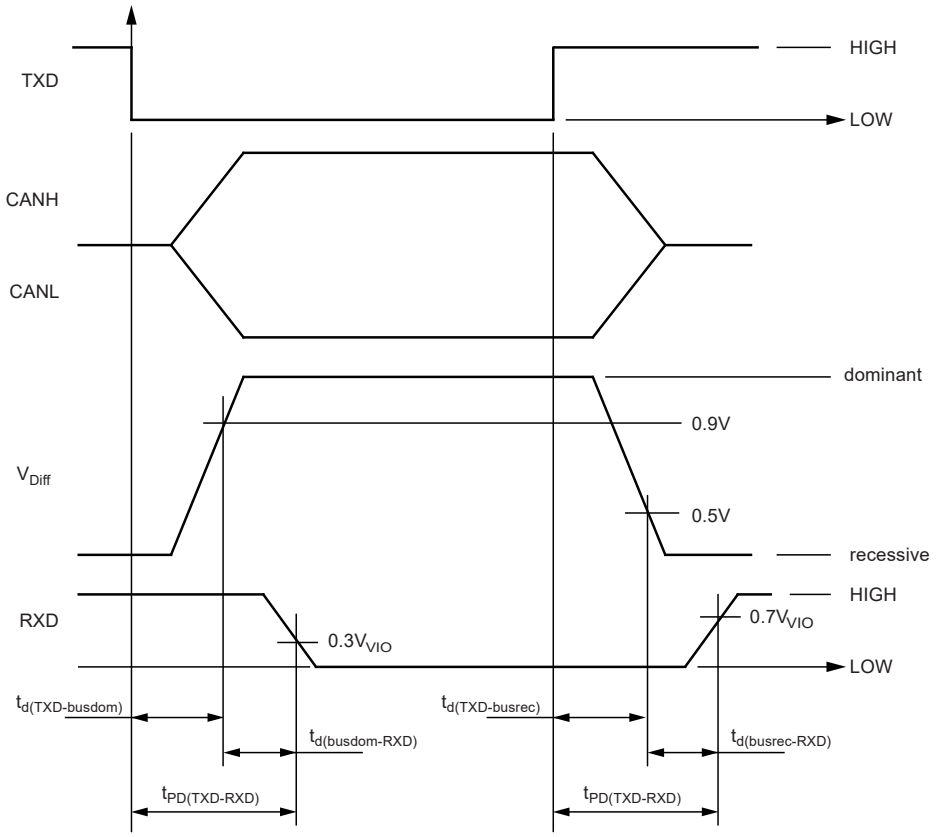


Figure 6-2. CAN Transceiver Timing Diagram 2

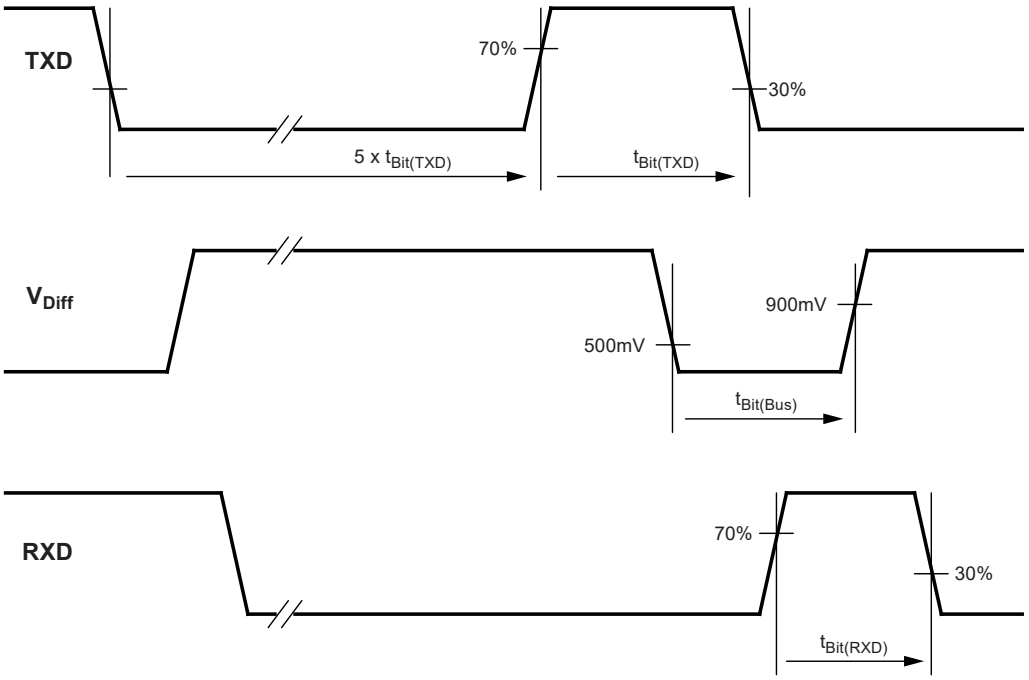
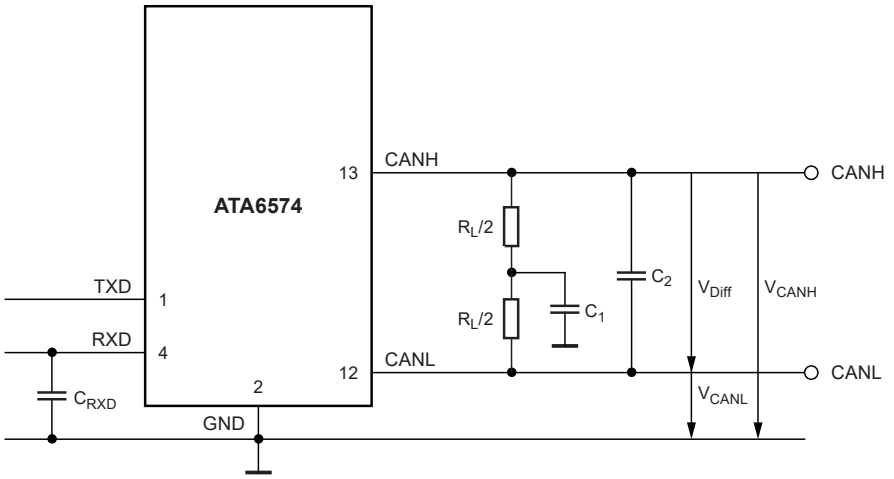


Figure 6-3. ATA6574 Test Circuit



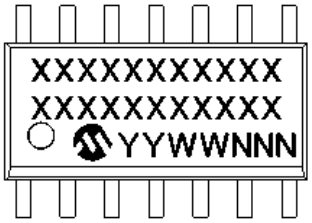
6.3 Thermal Characteristics

Table 6-1. Thermal Characteristics 14-Lead SOIC

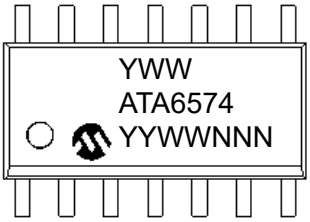
Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal Package Resistance					
Thermal Resistance Virtual Junction to Ambient, Where IC is Soldered to PCB According to JEDEC	R_{thvJA}	—	110	—	K/W
Thermal Shutdown of the Bus Drivers Output					
ATA6574-GNQW1 (Grade 1)	T_{vJsd}	150	—	195	°C
ATA6574-GNQW0 (Grade 0)	T_{vJsd}	170	—	195	°C
Thermal Shutdown Hysteresis	T_{vJsd_hys}	—	30	—	°C

7. Package Information

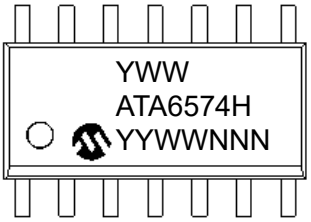
14-Lead SOIC



Example (Grade 1)



Example (Grade 0)

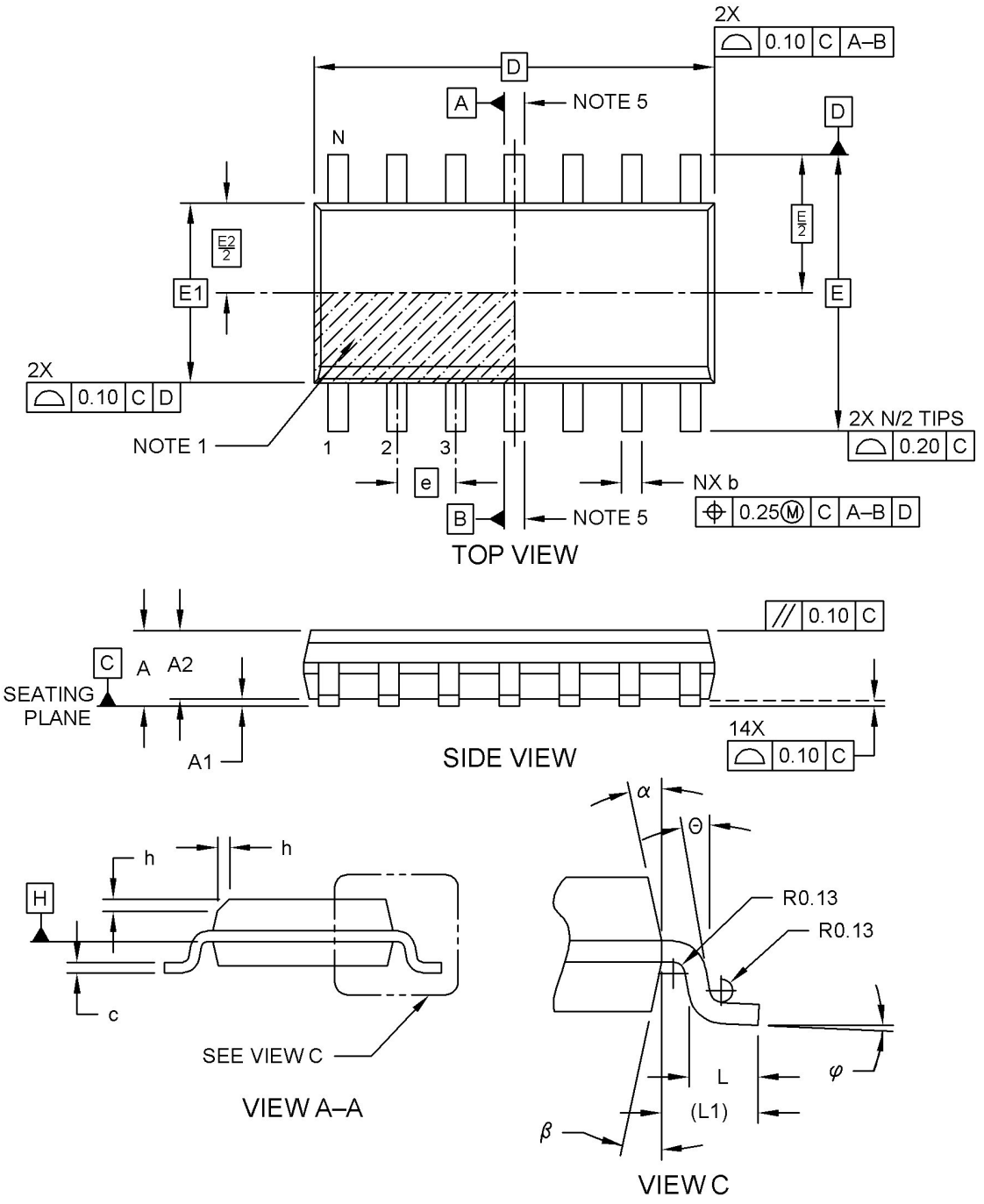


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)*	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

14-Lead Plastic Small Outline (4ZW) - Narrow, 3.90 mm Body [SOIC]

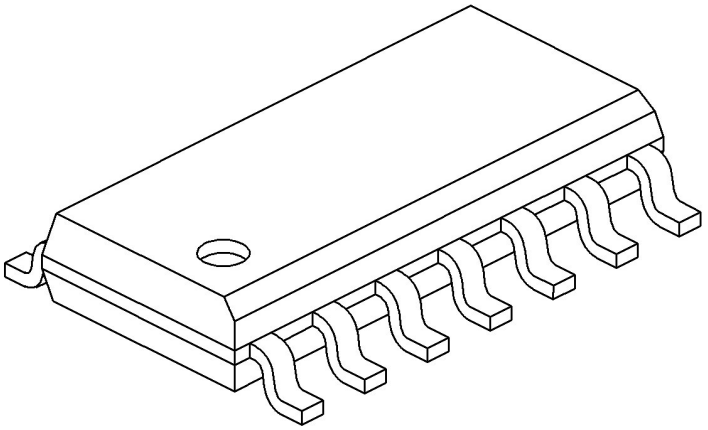
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-21319-4ZW Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (4ZW) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.19	-	0.25
Lead Width	b	0.33	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

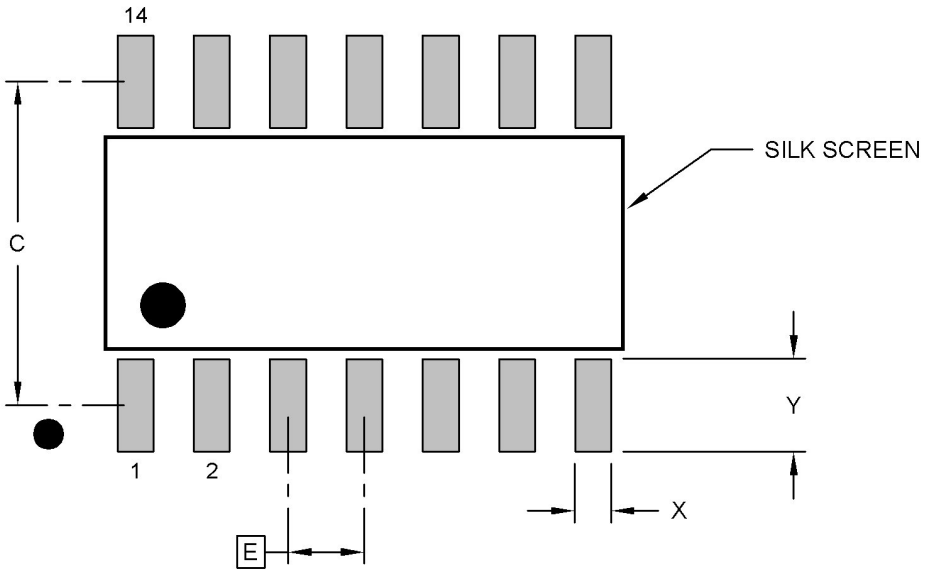
Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-21319-4ZW Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (4ZW) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-23319-4ZW Rev D

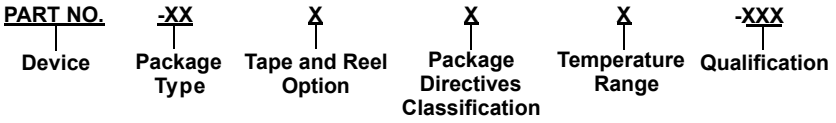
8. Revision History

Revision A (November 2024)

Original release of this document.

9. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Device:	ATA6574: High-Speed CAN Transceiver with Partial Networking	
Package:	GN	14-Lead SOIC
Tape and Reel Option:	Q	330 mm Diameter Tape and Reel (1)
Package Directives Classification:	W	Package according to RoHS (3)
Temperature Range:	0	Temperature Grade 0 (-40°C to +150°C)
	1	Temperature Grade 1 (-40°C to +125°C)
Qualification:	VAO	Automotive Qualified Device

Examples:

- ATA6574-GNQW0-VAO - High-Speed CAN Transceiver with Partial Networking and Watchdog (Default Off), CAN FD Capable, 14-Lead SOIC Package, Tape and Reel, RoHS Compliant, Automotive Qualified (Grade 0, -40°C to +150°C Temperature Range)
- ATA6574-GNQW1-VAO - High-Speed CAN Transceiver with Partial Networking and Watchdog (Default Off), CAN FD Capable, 14-Lead SOIC Package, Tape and Reel, RoHS Compliant, Automotive Qualified (Grade 1, -40°C to +125°C Temperature Range)

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.
3. RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (CI) and less than 0.15% (1500) total Bromine (Br) and Chlorine (CI) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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ISBN: 978-1-6683-0517-1

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