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MC74VHC573

Octal D-Type Latch with 3-State Output

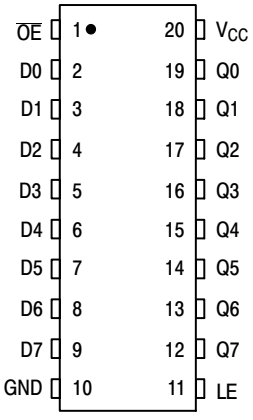
The MC74VHC573 is an advanced high speed CMOS octal latch with 3−state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8−bit D−type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: t_{PD} = 4.5 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 218 FETs or 54.5 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

PIN ASSIGNMENT



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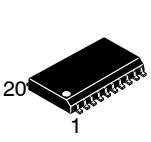
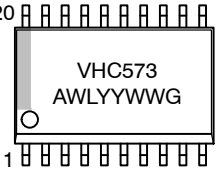
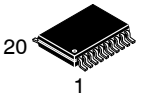
MARKING DIAGRAMS

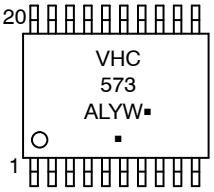


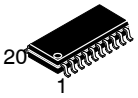
SOIC−20
DW SUFFIX
CASE 751D





TSSOP−20
DT SUFFIX
CASE 948E





SOEIAJ−20
M SUFFIX
CASE 967

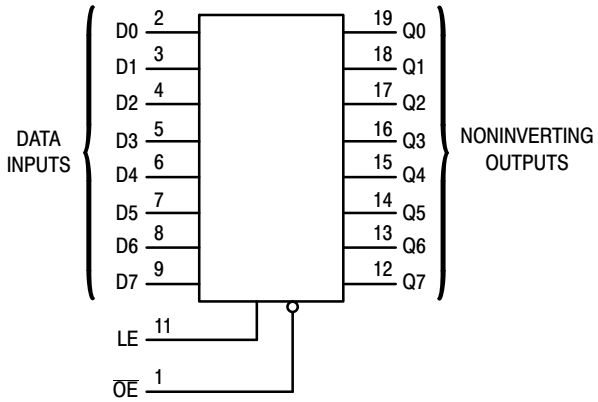
VHC573	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC573DWR2G	SOIC−20	1000 / Reel
MC74VHC573DTR2G	TSSOP−20	2500 / Reel
MC74VHC573MELG	SOEIAJ−20	2000 / Reel

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V V_{CC} = 5.0V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.6	11.9	1.0	14.0	ns
			C_L = 50pF		10.1	15.4	1.0	17.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		5.0	7.7	1.0	9.0	
			C_L = 50pF		6.5	9.7	1.0	11.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q	V_{CC} = 3.3 ± 0.3V	C_L = 15pF		7.0	11.0	1.0	13.0	ns
			C_L = 50pF		9.5	14.5	1.0	16.5	
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF		4.5	6.8	1.0	8.0	
			C_L = 50pF		6.0	8.8	1.0	10.0	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 15pF		7.3	11.5	1.0	13.5	ns
			C_L = 50pF		9.8	15.0	1.0	17.0	
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 15pF		5.2	7.7	1.0	9.0	
			C_L = 50pF		6.7	9.7	1.0	11.0	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Q	V_{CC} = 3.3 ± 0.3V R_L = 1kΩ	C_L = 50pF		10.7	14.5	1.0	16.5	ns
		V_{CC} = 5.0 ± 0.5V R_L = 1kΩ	C_L = 50pF		6.7	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V (Note 1)	C_L = 50pF			1.5		1.5	ns
		V_{CC} = 5.5 ± 0.5V (Note 1)	C_L = 50pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)				6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2)	29	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50 pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.9	– 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 3.3 \pm 0.3$V $V_{CC} = 5.0 \pm 0.5$V		5.0 5.0	5.0 5.0	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 3.3 \pm 0.3$V $V_{CC} = 5.0 \pm 0.5$V		3.5 3.5	3.5 3.5	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 3.3 \pm 0.3$V $V_{CC} = 5.0 \pm 0.5$V		1.5 1.5	1.5 1.5	ns

SWITCHING WAVEFORMS

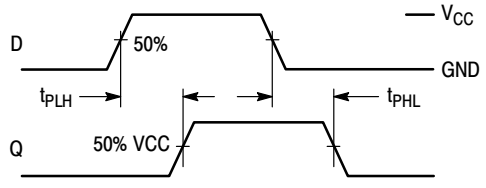


Figure 1.

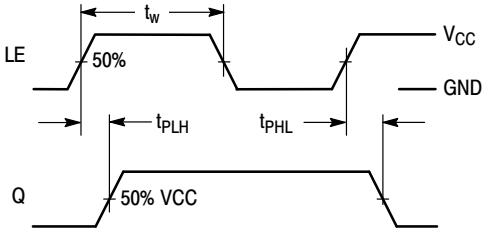


Figure 2.

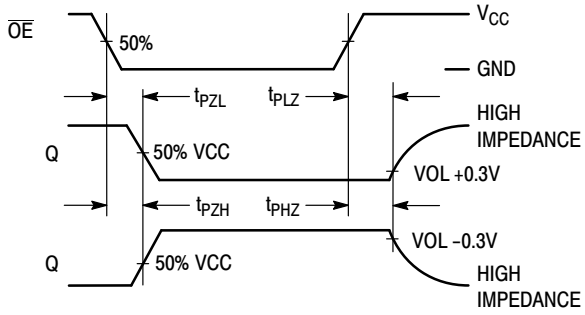


Figure 3.

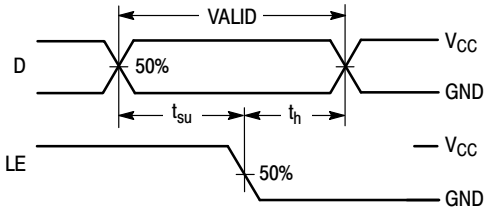
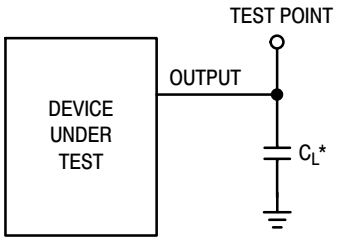


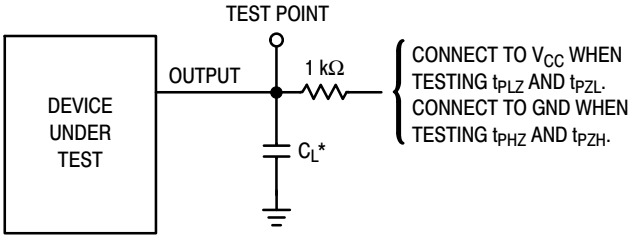
Figure 4.

TEST CIRCUITS



*Includes all probe and jig capacitance

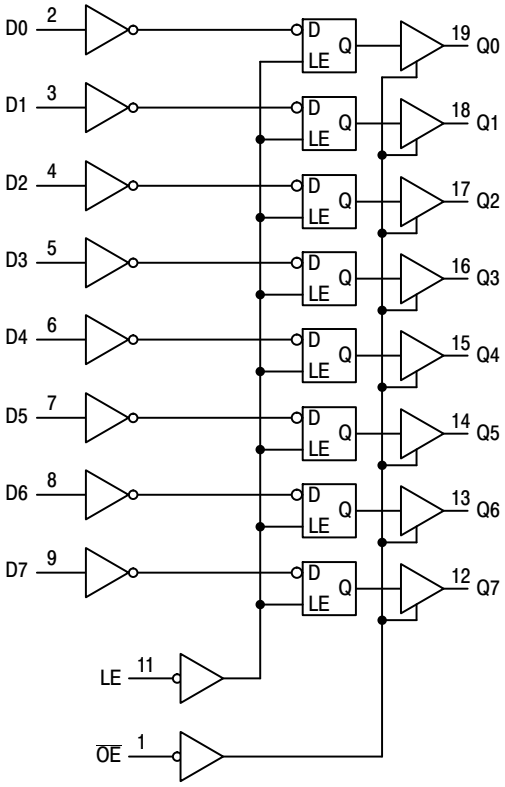
Figure 5.



*Includes all probe and jig capacitance

Figure 6.

EXPANDED LOGIC DIAGRAM



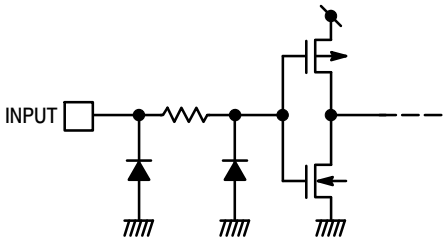
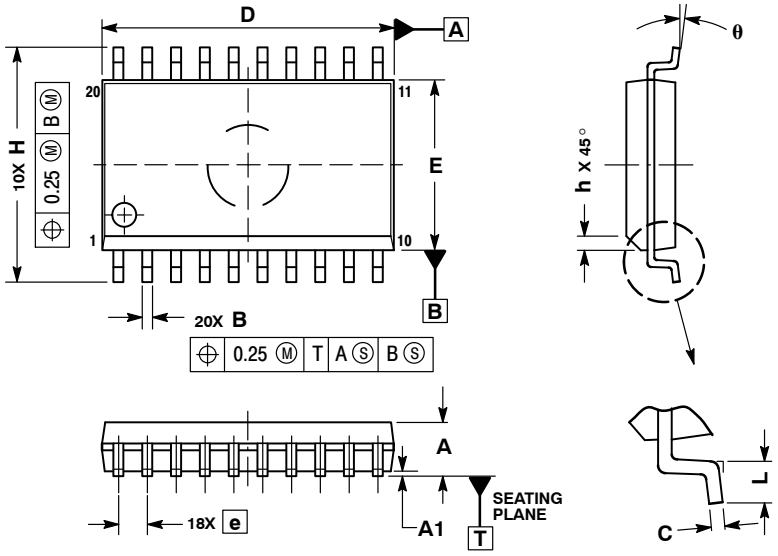


Figure 7. Input Equivalent Circuit

PACKAGE DIMENSIONS

SOIC−20
DW SUFFIX
CASE 751D−05
ISSUE G

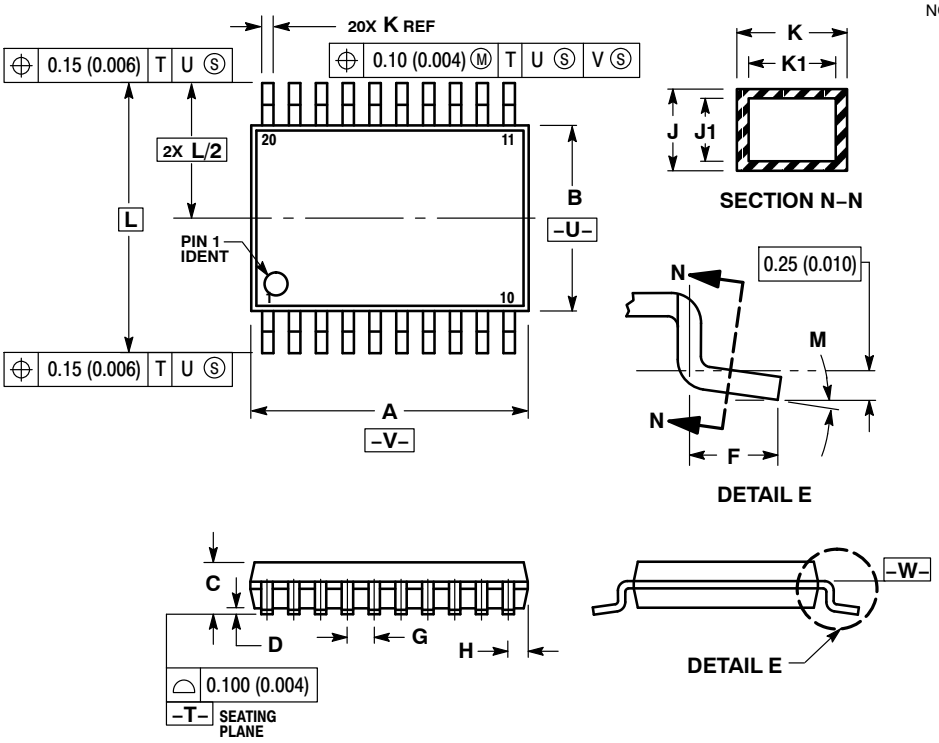


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

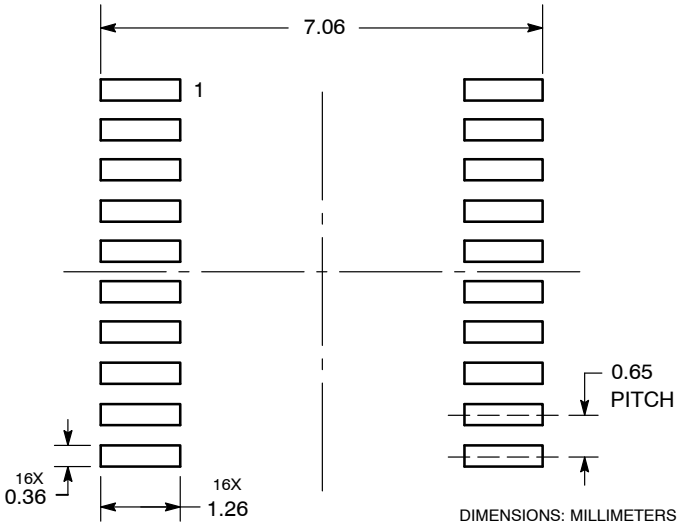
TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

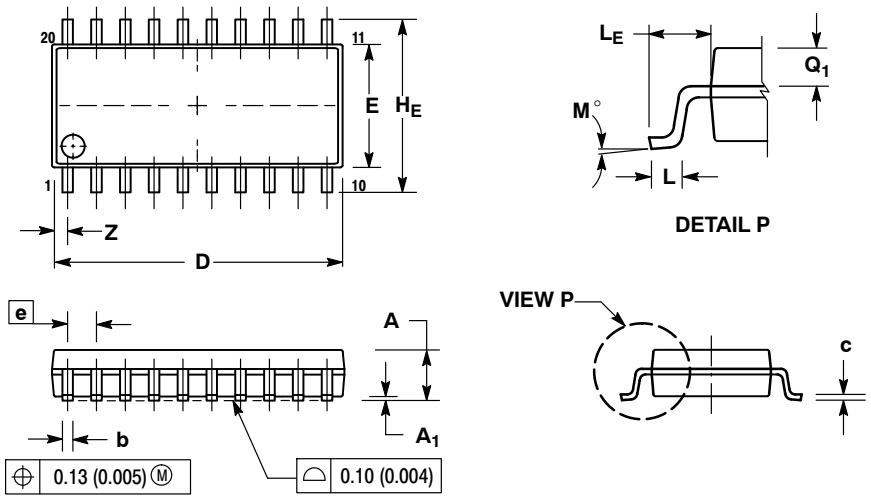
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

SOEIAJ–20
CASE 967–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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