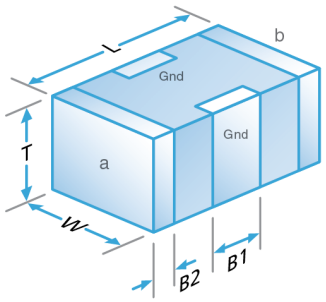
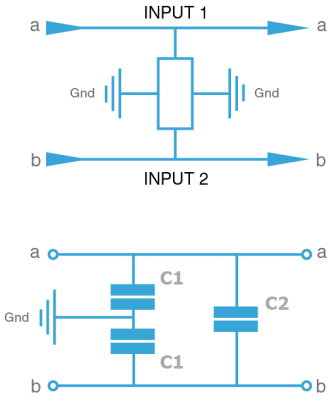
Multilayer Ceramic Chip Capacitor

Part Number: 1812Y1000104METE03

Description: 1812 100Vdc 100nF ±20% X7R (2R1) to AEC-Q200

A range of ceramic MLCC bypass 'C' filters offering exceptionally low inductance and enhanced performance using the 'X2Y' style internal electrode structure, Bypass application means there is no current limiting factor with this component. Ideally suited to balanced line applications, where the 2 capacitors per single chip ensure common thermal & voltage variation. Available with a variety of termination options including FlexiCap™ (on X7R), the world's first commercially available flexible termination. Tested and approved to automotive specification AEC-Q200.





Mechanical Specification

Size Code	1812
Length (L1) in mm (")	4.5 +0.45/-0.35 (0.177 +0.018/-0.014)
Width (W) in mm (")	3.2 ± 0.30 (0.126 ± 0.012)
Thickness (T) in mm (")	2.1 Max (0.08 Max)
Termination Bands (B2) in mm (")	0.75 ± 0.25 (0.03 ± 0.01)
Center (Ground) Band (B1) in mm (")	1.45 ± 0.35 (0.055 ± 0.014)
Termination Material	FlexiCap™ Polymer termination, Nickel barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 1000 per reel

General Electrical Specification

Rated Voltage	100Vdc
Nominal Capacitance Value (line to ground)	100nF
Capacitance Tolerance	±20%
Nominal Capacitance Value (line to line)	50nF
Tangent of Loss Angle (Tan δ)	≤0.025
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1kHz
Voltage Proof (Voltage applied for 5 secs max. @ 50mA max. charge current)	250Vdc
Min Insulation Resistance (IR) L-G	10.00GOhm @ 100Vdc
Min Insulation Resistance (IR) L-L	20.00GOhm
Dielectric Classification	X7R (2R1) to AEC-Q200
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage ±15% Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	<2% per decade

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This datasheet is for a standard item and is confirmed valid on the date generated, the latest published data for this part may differ and is available at http://www.knowlescapacitors.com or by contacting us.

Data is correct to the best of our knowledge, errors and omissions excepted.

Date: Sunday, April 25, 2021

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Multilayer Ceramic Chip Capacitor

Part Number: 1812Y1000104METE03

Description: 1812 100Vdc 100nF ±20% X7R (2R1) to AEC-Q200

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	209 compliant
California Proposition 65	No exposure risk

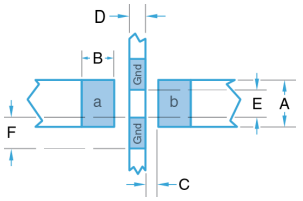
Board Layout

Knowles' conventional 3-terminal chip capacitors should be mounted using the pad design supplied.

It has been developed in conjunction with our customers over the years and has been shown to yield succesful soldering results. It incorporates factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width, but the position of the chip on the board should also be considered.

Note that for optimum noise rejection the ground pads should be placed on the circuit board ground plane, or connected to the ground plane by the shortest and widest route possible.

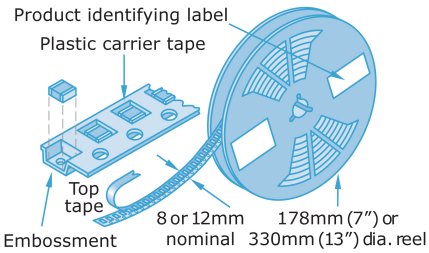
	1812	
A	2.65mm	0.104"
B	1.40mm	0.055"
C	0.80mm	0.031"
D	1.40mm	0.055"
E	2.05mm	0.080"
F	1.08mm	0.043"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.

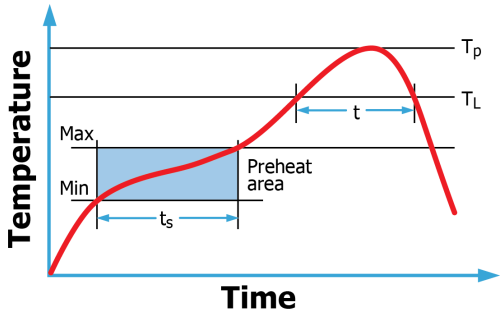


Soldering

Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.



Application notes with mounting and handling guidance are available on request.

Compex DLI Johanson MFG Novacap Syfer Voltronics

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