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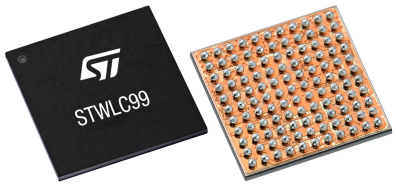
STWLC99

Datasheet

Qi-compliant wireless power receiver for up to 100W output power applications



Product status link
STWLC99

Product summary	
Order code	STWLC99JR
Package	WLCSP121
Packing	Tape and reel

Features

- Up to 100W output power
- Up to 25W output power in Tx mode
- Qi 1.3 compliant
- Integrated low RDS-ON synchronous rectifier with ≥ 98% efficiency
- ARC(Adaptive Rectifier Configuration) mode for enhanced spatial freedom
- Low drop-out linear regulator with output current and input voltage loops
- Programmable output voltage 4V to 20V in steps of 25mV
- 64MHz 32bit Arm® Cortex®-M0+ core with 12KB FTP,8KB RAM,48KB ROM
- 11-bit A/D converter
- Configurable GPIO's
- I^2C Slave, Master interface
- Watchdog timer
- Multi-levels ASK modulator, Enhanced FSK demodulator
- Accurate current sense system for Foreign Object Detection(FOD)
- Coil Q-factor measurement for FOD in Tx mode
- Over voltage, over current and thermal protections
- Proprietary protocol for power negotiation and authentication
- Suitable for industrial applications, power tools, autonomous robots
- Flip chip 121 bumps (4.859 mm x 4.859 mm)

Application

- Smartphones,Tablets, Laptops
- Cordless power tools
- Power banks

Description

The STWLC99 is a highly integrated wireless power receiver suitable for applications delivering an output power up to 100W.The chip has been designed to support Qi specifications 1.3 for inductive communication protocol with Extended Power Profile (EPP) and proprietary ST Super Charge(STSC) protocol for fast charging.

With integrated low-loss synchronous rectifier and low drop-out linear regulator, STWLC99 achieves high efficiency with low power dissipation.

Through I2C interface the user can access and modify the configuration parameters for customized applications, the final configuration parameters are stored in embedded Few Times Programmable(FTP) non-volatile memory and automatically retrieved at power-up.

The device can also operate as a wireless transmitter, capable of transmitting up to 25W of power (depending on the coil used)

The device is housed in a Chip-Scale Package to fit real-estate applications with reduced BOM count.

1 Introduction

The STWLC99 is primarily a wireless power receiver, but it can also reverse its operation and act as a wireless power transmitter in the same application. When configured as wireless power receiver (Rx mode) it rectifies the AC voltage developed across the receiving coil and provides a regulated DC voltage at the output.

The 32-bit core MCU is the supervisor of the whole device and manages all the functional blocks to

- establish and maintain communication with the transmitter.
- ensure adherence to Qi standard specifications (wherever required).
- optimize the efficiency by properly adjusting the operating point.
- guarantee reliability by monitoring and protecting both the load and the device itself.

In order to execute the above mentioned (and many others) task, the MCU core relies on a resident firmware stored in ROM memory.

In addition, some configuration parameters (for example, output voltage, FOD tuning parameters, etc.) can be saved in the internal few-times programmable memory and retrieved at power-up, allowing the STWLC99 to operate as a fully autonomous standalone chip.

The STWLC99 firmware is patchable via the internal FTP memory used to store the configuration parameters.

Applications in which the host system directly monitors or controls the power transfer, the I²C interface provides full access to the internal registers of the STWLC99.

The flexibility of the STWLC99 is further enhanced by

- programmable general-purpose I/O pins (GPIOs) to implement specific functions (for example, driving status LEDs, enabling the output on request, informing the host system about faulty conditions, etc.).
- two analog inputs to monitor voltages and signals (for example, the temperature of the coil).
- master I²C interface to manage external devices.

Typical application block diagram is shown below.

The synchronous rectifier converts the AC voltage from the receiving coil into a DC voltage at the VRECT pin.

The four switches of the rectifier (that is basically an H-bridge) are controlled by the digital core in order to minimize both conduction and switching losses as a function of the output voltage and current, both monitored by ADC.

Two bootstrap capacitors are externally connected to the BOOT1-BOOT2 pins to correctly drive the high-side switches of the rectifier.

The output of the rectifier, filtered by an external capacitor, is also the input rail for the main LDO linear regulator and for the auxiliary linear regulators in charge of deriving the 5 V, 1.8 V supply voltages.

The digital core has full control of the main LDO linear regulator in order to manage the output voltage, the output current and the drop-out voltage: since the most relevant contribution to the total chip power dissipation is due to the main linear regulator, minimizing its drop-out voltage is a key factor.

Of course, the minimization of the drop-out voltage requires a closed loop regulation of the voltage at the VRECT pin, that is, a feedback information that is sent to the transmitter (via ASK modulation).

which, in turn, adjusts the delivered power by acting on the supply voltage, the switching frequency or the switching duty-cycle (or a combination of the three) of its own power stage, depending on the adopted technique.

This regulation loop involving the transmitter is an essential part of the wireless power transmission and is extensively described in Qi specifications.

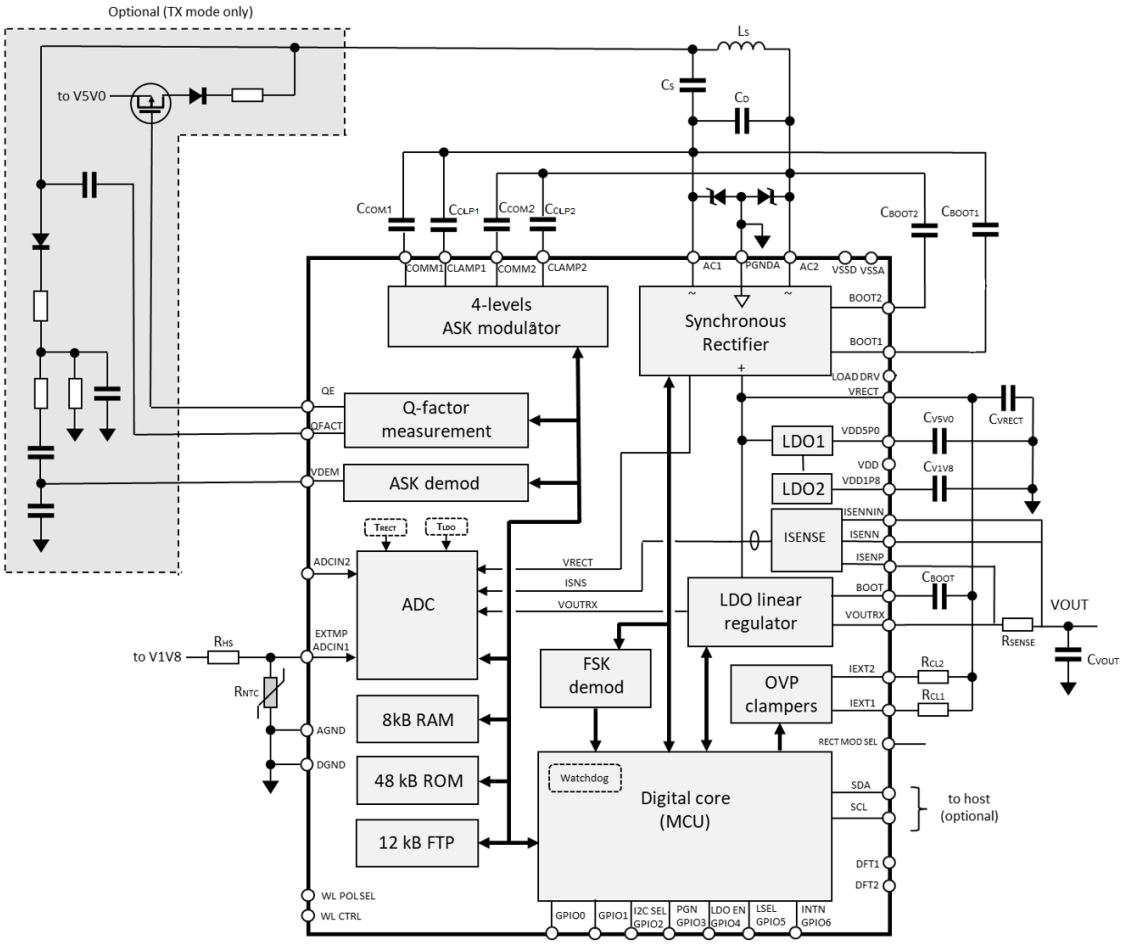
The STWLC99 is equipped with an enhanced and robust FSK/ASK communication circuit that, in combination with a watchdog timer, ensure a superior application reliability.

Regarding the safety precautions for the user, the STWLC99 provides accurate over-current protection (OCP), over-temperature protection (OTP) and two programmable, independent over-voltage protection (OVP) mechanisms.

When configured as a wireless power transmitter (Tx mode), the STWLC99 is capable of delivering up to 25W, depending on the characteristics of the coil.

In this operating mode, a dedicated Q-factor measurement circuit is used to determine the quality factor of the coil for accurate foreign object detection (FOD) prior initiating a power transfer negotiation.

2 Typical application diagram



3 Device pinout

Figure 1. **Pin assignment (through top view)**

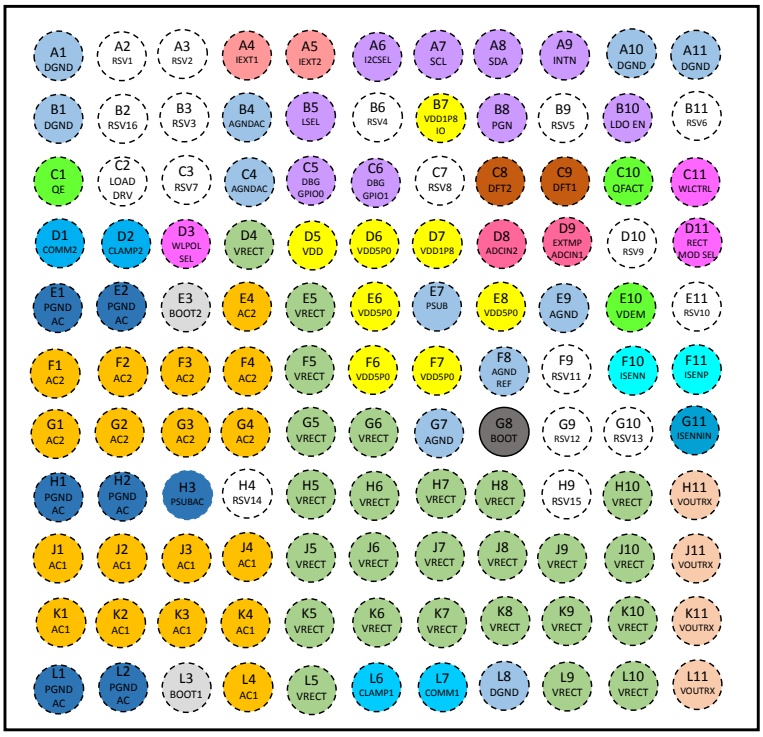


Table 1. **Pin description**

Pin name	Pin location	Pin function
DGND	A1, A10, A11, B1, L8	Digital ground. Reference for digital input and output signals.
PGNDAC	E1, E2, H1, H2, L1, L2	Power return for the synchronous rectifier analog circuitry.
AGNDAC	B4, C4	Power return for analog circuitry.
AGND	E9, G7	Analog ground .
AGNDREF	F8	Analog ground
PSUBAC	H3	AGND for power, PGND, PSUBAC, AGND was connected together on PCB.
PSUB	E7	GROUND
AC1	J1, J2, J3, J4, K1, K2, K3, K4, L4	AC power input: input of the synchronous rectifier. Connect to RX series resonant circuit.
AC2	E4, F1, F2, F3, F4, G1, G2, G3, G4	AC power input: input of the synchronous rectifier. Connect to RX series resonant circuit.
BOOT1	L3	Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC1.
BOOT2	E3	Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC2.
BOOT	G8	Main LDO power transistor bootstrap capacitor. Connect a 4.7 nF (typ.) ceramic capacitor between this pin and VRECT.
COMM1	L7	Modulation switches connection: capacitors between COMM1, CLAMP1 and AC1 pin and between COMM2, CLAMP2 and AC2 pin are used to implement ASK modulation.
CLAMP1	L6	
COMM2	D1	

Pin name	Pin location	Pin function
CLAMP2	D2	Modulation switches connection: capacitors between COMM1, CLAMP1 and AC1 pin and between COMM2, CLAMP2 and AC2 pin are used to implement ASK modulation.
VRECT	D4, E5, F5, G5, G6, H5, H6, H7, H8, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10, L5, L9, L10	Synchronous rectifier output and input for the main LDO linear regulator. A suitable capacitor between these pins and VSSP ensures residual AC ripple filtering and energy storage for proper load transient response.
VOUTRX	H11, J11, K11, L11	Main LDO linear regulator power output. Connect a suitable filter on and proper loading capacitor between these pins and VSSA to ensure stable operation and proper load transient response in all operating conditions.
ISENIN	G11	Current sense input : Connect to ISENN
ISENN	F10	Connect remote Rsense system load side
ISENP	F11	Connect remote Rsense VOUTRX side
VDD1P8IO	B7	1.8V; VDD1P8_IO is only connected to internal pull-up of PGN, INTN. Connect a 0.1uF(typ) filtering capacitor between this pin and ground
VDD1P8	D7	1.8 V LDO output and supply rail for the ADC and the analog circuitry. Connect a 1 µF (typ.) filtering capacitor between this pin and ground.
VDD	D5	input pin: external 5V .
VDD5P0	D6, E6, E8, F6, F7	Output pin: 5V LDO output and supply rail for the auxiliary circuitry. Connect a 4.7 µF (typ.) filtering capacitor between this pin and ground
VDEM	E10	ASK de-modulation input.
IEXT1	A4	Internal pull-down switches for active (dissipative) two-levels over-voltage clamper: a resistor with adequate power dissipation capability must be connected between each pin and VRECT to damp excessive voltage developing at the output of the rectifier.
IEXT2	A5	
LOADDRV	C2	No connection, to be left floating
QE	C1	Coil quality-factor measurement, excitation output. This pin is used to drive an external transistor to inject excitation pulses into the resonant circuit. Used in conjunction with QFACT pin to measure the quality factor of the coil.
QFACT	C10	Coil quality-factor measurement, sensing input. This pin is used to sense the ringing developing across the resonant circuit after an excitation pulse is applied via QE pin.
EXTMP ADCIN1	D9	Coil temperature sensing input: this pin is connected to the center tap of a resistor divider having an NTC in the low-side position. If this function is not used, the pin must be pulled-up to VDD5P0 through a 30kΩ pull up and 100kΩ pulled down resistors to prevent triggering the coil over-temperature protection.
ADCIN2	D8	ADC Input
WLCTRL	C11	WL control signal Chip enable when WLPOLSEL=HIGH, WLCTRL=HIGH; Chip disable when WLPOLSEL=HIGH,WLCTRL= HIGH; Chip disable when WLPOLSEL=LOW, WLCTRL=HIGH; Chip enable when WLPOLSEL=LOW, WLCTRL=LOW;
WLPOLSEL	D3	Used with WLCTRL WLPOL selection; GPIO chip internal pull up to 1.8V
RECT MOD SEL	D11	To be connected to Ground
LSEL/GPIO5	B5	VOUTRX current level select High or floating for 200mohm coil - 3A

Pin name	Pin location	Pin function
		Low for 60mohm coil and large current - 5A
I2CSEL/GPIO2	A6	GPIO input, I²C address selection Floating/Logic HIGH : 0x2B Logic LOW: 0x2C
PGN/GPIO3	B8	GPIO output, Power good signal output pin. High: LDO ON Low: LDO OFF GPIO output internal pull up to VDD_1P8_IO
LDOEN/GPIO4	B10	GPIO input High: Turn off MAIN LDO Low: Turn on MAIN LDO
SCL	A7	I2C bus, clock line input. A pull-up resistor to external supply rail of the host controller is required to ensure correct digital levels.
SDA	A8	I2C bus, data line I/O. A pull-up resistor to external supply rail of the host controller is required to ensure correct digital levels.
DBGGPIO0	C5	Programmable general-purpose I/Os
DBGGPIO1	C6	
INTN/GPIO6	A9	GPIO output, Interrupt output (active low). Programmable open-drain output used to generate an interrupt on specific events for the host controller.
DFT1	C9	Test Mode - DFT , to be left floating
DFT2	C8	Test Mode - DFT , to be left floating
RESERVED	A2,A3,B2,B3,B6,B9,B11,C3,C7,D10,E11,F9,G9,G10,H4,H9	Reserved Pins to be left Floating

4 Electrical and thermal specifications

4.1 Absolute maximum ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in Table 2 is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Parameter	Pin(s)	Min.	Max.	Unit
Pin voltage range	AC1, AC2, COMM1, COMM2, CLAMP1, CLAMP2, respect to ground	-0.9	27	V
	BOOT1 to AC1	-0.3	5.5	
	BOOT2 to AC2			
	BOOT1 and BOOT2 respect to ground (VSSA, VSSD and VSSP pins)	-0.3	32	
	BOOT respect to VRECT	-0.3	5.5	
	VRECT, VOUTRX, IEXT1, IEXT2, and QFACT respect to ground	-0.3	27	
	VDD1P8, VDD1P8_IO respect to ground	-0.3	1.98	
	ADCIN1(EXTMP), ADCIN2, DFT1, DFT2 respect to ground	-0.3	5.5	
	GPIO0 through GPIO5, INTB, RSTB, SDA, SCL, WLCTRL, WLPOLSEL respect to ground If internal pull up, is enable	-0.3	1.98	
	VDD5P0 and VDEM respect to ground (VSSA, VSSD, and VSSP pins)	-0.3	5.5	
	RECTMODSEL and QE respect to ground	-0.3	5.5	
RMS pin current	AC1,AC2		6	A
	VRECT,VOUT		5.4	
	COMM1,COMM2,CLAMP1,CLAMP2		0.5	
	IEXT1,IEXT2		0.5	
HBM ESD susceptibility JEDEC JS001-2012	All pins		2000	V
CDM ESD susceptibility JEDEC JS002-2012			500	
Latch-Up EIA/JESD78E			200	mA

4.2 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{A,OP}$ (1)	Operating ambient temperature		-40		85	°C
$T_{J,OP}$	Operating junction temperature		0		125	
$R_{\Theta JA}$ (2)	Junction to ambient thermal resistance	2s2p		47		°C/W
T_{SHDN}	Thermal shutdown threshold	Default Programmable 105,115,125,135		115		°C
$T_{SHDN,HYST}$	Thermal shutdown hysteresis			10		

1. *Ta -40°C to 85°C , limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization,if not otherwise specified.*
2. *Device mounted on a standard JESD51-5 test board*

4.3 Electrical characteristics

0 °C < T_A < 85 °C; V_{VRECT} = 5 V to 20 V. Typical values are at T_J = 25 °C, if not otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply section						
$V_{VRECT,UVLO}$	VRECT Under-Voltage Lock-Out upper (turn-on) threshold	VRECT pin voltage, rising edge in RX mode		2.9	3.3	V
$V_{VOUT,UVLO}$	VOUT Under-Voltage Lock-Out upper (turn-on) threshold	VOUTRX pin voltage, rising edge in TX mode		2.9	3.3	
$V_{VRECT,MAX}$	VRECT maximum operating supply voltage	Voltage on VRECT pin			22	V
$I_{VOUT,Q}$	VOUT current consumption in shut-down mode	CHIP disable for more than 1 ms, supply voltage (5 V) applied to VOUTRX		910		uA
$I_{VOUT,OP}$	Operating current consumption (not considering the programmed dummy-load current)	CHIP enable, supply voltage applied to VOUTRX		22		mA
1.8V supply voltage LDO linear regulator						
V_{V1V8}	LDO2 output voltage	I_{V1V8} = 5 mA	1.62	1.8	1.98	V
5V supply voltage LDO linear regulator						
V_{V5V0}	LDO1 output voltage	I_{V5V0} = 5 mA	4.75	5	5.25	V
$I_{V5V0,EXT}$	Maximum current allowed for external load				15	mA
Synchronous rectifier						
$f_{AC\ RX}$	Synchronous rectifier operating frequency range		50		1000	KHz
Efficiency	Target rectifier efficiency	I_{VRECT} = 1 A, V_{VRECT}= 5.2 V, f_{AC} = 100 kHz to 200 kHz		94		%
		I_{VRECT} = 2 A, V_{VRECT} = 20 V, f_{AC} = 100 kHz to 200 kHz		98		
$f_{AC\ TX}$	Inverter operating frequency range		100		400	KHz

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ASK modulator						
$R_{DSON,COMMx}$	COMM1,COMM2,CLAMP1,CLAMP2 modulation switches on-resistance	V_{VRECT} = 5 V		1	2	Ω
$I_{COM\ MAX}$	COMM1,COMM2,CLAMP1,CLAMP2 modulation switches current capability	RMS value		0.25		A
I_{DMYL}	Dummy load current (internally drawn from VRECT when enabled)	V_{VRECT} = 5 V to 20 V			64	mA
Main LDO linear regulator						
VOUT	Output voltage range	VOUT_SET = 0x00C8	4.90	5.0	5.10	V
		VOUT_SET = 0x0320	19.8	20	20.2	
	VOUT Line regulation	I_{VOUT} = 0.1 A, VOUT = 5 V, 6 V < V_{VRECT} < 15 V		18		mV
	VOUT Load regulation	V_{VRECT} = 5.5 V, VOUT = 5 V, 1 mA < I_{VOUT} < 800mA		30	70	mV
V_{OUT_STEP}	Programmable step size			25		mV
V_{DROP}	Linear regulator drop-out voltage	I_{OUT} = 1 A		15		mV
TX Mode						
VIN-Tx	VOUT input operating voltage in Tx mode		4.95		20	V
Thermal protection (external NTC)						
$V_{NTC,OTP}$	External over-temperature NTC pin upper threshold		0.55	0.59	0.65	V
	External over-temperature NTC pin hysteresis		50	125	150	mV
$I_{NTC,BIAS}$	NTC pin bias current	V_{NTC} = 1.5 V		1	2	µA
Over-Voltage Protection						
V_{OVPH}	Hard OVP (AC1-AC2 short to VSSP) upper threshold	Default: 26V Programmable 26.5V,26V,25.5V,25V		26		V
	Hard OVP release voltage	Default:19V Programmable 19V,16V,13V,10V		19		
V_{OVPS1}	Soft OVP1 (IEXT1 clamper intervention) upper threshold at VRECT	Default: 23V Programmable 24V,23.5V,23V,22.5V		23		V
V_{OVPS2}	Soft OVP2 (IEXT2 clamper intervention) upper threshold at VRECT	Default: 24.5V Programmable 25V,24.5V,24V,23.5V		24.5		
V_{OVPSL}	Soft OVP1 and soft OVP2 release threshold at VRECT			$V_{OVPS1-1V}$		
$I_{IEXT,MAX}$	IEXT clamping switch current capability	Non-repetitive 100 ms rectangular pulse			0.3	A
$R_{IEXT1,2,ON}$	IEXT switch on-resistance	I_{IEXT} = 250 mA		1.8	3	Ω
V_{OVPFH}	Fast OVP upper threshold at VRECT			18	18.7	V
V_{OVPFL}	Fast OVP release threshold at VRECT		12.4	13	13.6	V
Current sensor						
I_{SNS}	Current sensing range	RX mode	0		6	A

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SNS}	Overall absolute accuracy	RX mode		1	3	%
	Output current accuracy	IVOUT < 1000mA		10		mA
		IVOUT > 1A		1	3	%
Digital signals						
V_{IL}	Low level input voltage	VDDE: IO supply voltage 1.8V			0.3*VDDE	V
V_{IH}	High level input voltage	VDDE: IO supply voltage 1.8V	0.7*VDDE			
V_{OH}	GPIOx high level output voltage	Output high, I_{SOURCE} = 3mA VDDE: IO supply voltage 1.8V	VDDE-0.2			
I_{OH}	GPIOx pin current capability	Output high	3			mA
V_{OL}	Low level output voltage	Output low, I_{SINK}=3mA			0.4	V

5 Device description

5.1 Chip Enable , Disable

Chip disable function to put the device in reset state.

Chip enable function to resume normal operation.

It is controlled by WLCTRL and WLPOLSEL signals

Chip enable when WLPOLSEL=HIGH, WLCTRL= HIGH

Chip disable when WLPOLSEL=HIGH,WLCTRL= LOW

Chip disable when WLPOLSEL=LOW, WLCTRL= HIGH

Chip enable when WLPOLSEL=LOW, WLCTRL= LOW

5.2 Synchronous rectifier

The synchronous rectifier of the STWLC99 is a key block in charge of converting the AC input power from the receiving coil into a DC supply rail for the following linear regulator.

In principle it consists of four N-channel MOSFETs arranged in a H-bridge, conveniently driven by a control block that monitors the voltage at the AC1 and AC2 pins to optimize the commutations and to charge the external bootstrap capacitors for the high-side switches.

Different driving schemes are possible for the switches of the rectifier and the MCU core dynamically selects the optimal one to maximize the overall efficiency as a function of the operating point.

When designing the filtering capacitor at the output of the synchronous rectifier, it must be taken into account that it has to minimize the AC residual ripple and to provide energy storage to sustain load transients, without impacting on the ASK communication with the transmitter.

5.3 Main linear regulator

The main linear regulator of the STWLC99 ensures a constant output voltage with minimum power loss. Excellent line and load regulation are demanded to the analog circuitry of this block, while the optimal operating point is managed by the MCU core.

The minimization of the power loss is achieved by adjusting the drop-out voltage according to a programmed target curve: to do so, the MCU core handles the communication with the transmitter to get the desired VRECT rail voltage.

Key voltages and currents in the block are constantly monitored to optimize the performance of the linear regulator and to provide multiple protection levels (see related section).

The main linear regulator has three independent control loops acting on the power pass element:

- Output voltage regulation loop: this loop regulates the output voltage at the nominal value set in the dedicated register;
- Input current regulation loop: in order to prevent a collapse at the output of the synchronous rectifier, the current through the linear regulator is limited to a programmed threshold.
- Input voltage regulation loop: this loop works in conjunction with the input current one and avoids that the VRECT rail drops below a programmable value.

Both input current and input voltage regulation loops play an important role: since the output of the rectifier is a highly variable voltage source (especially because of unpredictable changes in coupling of the coils), extra care is needed to avoid voltage drops that could lead to an undesirable MCU core reset.

The pass transistor is an N-channel MOSFET and the BOOT pin is dedicated to its bootstrap capacitor, ensuring correct driving and lower on-resistance also in case of drop-out condition.

5.4 ASK , FSK communication

Robust and reliable in-band ASK modulation is critical to the operation of any Qi compliant devices. STWLC99 has dedicated hardware on top of the firmware algorithm to improve the performance of the in-band communication.

STWLC99 allows for two set of modulation capacitor, namely COMM1/2, CLAMP1/2 . These two sets of ASK communication capacitors can be used in parallel or individually according to the load condition of the device.

This allows for high level of flexibility to cater for a wide range of wireless transmitters. The modulation control can be set by the firmware.

STWLC99 comes with an advance FSK demodulation filter which is able to remove any glitches present in the rectifier output.

5.5 ARC (Adaptive Rectifier Configuration) Mode

ARC (Adaptive Rectifier Configuration) mode improves the ping up and power transfer spatial freedom of the system in both X and Y direction.

Without any change in hardware or optimization of the coil, the ping up distance is enhanced by up to 50% in all directions by enabling ARC mode. This transforms the whole surface of the Tx to a usable area. Further enhancement is possible by customization of the coil.

Coil parameter tolerance requirements are widely relaxed due to ARC mode ping up feature. This is critical to applications where coils are of thinner dimensions, and it is relatively costlier to keep coil parameters within tight tolerances.

5.6 GPIOx and INTN pins

The GPIO pins are programmable general-purpose I/O pins whose functions can be assigned in configuration settings. These pins can be configured both as inputs and outputs according to the selected function.

The INTN pin is an interrupt output line that can be associated to any internal interrupt condition and used to inform the host system about specific events. The INTN pin can be programmed to be push-pull or open-drain type as well.

5.7 Protections

Over-voltage protection

The STWLC99 integrates different Over-Voltage Protection circuits to protect itself, the load connected to its output rail and the external components from damage due to overheating and/or exceeding AMR condition.

A sudden change in the coupling factor between transmitting and receiving coils, for example due to abrupt reciprocal repositioning of the coils, easily leads to unpredictable voltage peaks at the AC input terminals: the TX-RX regulation loop is not fast enough to prevent such an event and additional precautions must be taken.

Both the VRECT and VOUT outputs are constantly monitored.

The VRECT rail has different OVP mechanisms: Fast OVP,Hard OVP , Soft OVP1, Soft OVP2.

Fast OVP

In the event VRECT pin ≥ 18V before the digital logic wakes up , Fast OVP is triggered. The protection circuit immediately shorts both AC1 and AC2 pins to ground.

Fast OVP is released when VRECT < 13V.

Hard OVP (Hard Over Voltage Protection)

In the event of VRECT pin ≥ 26V (programmable 25V, 25.5V, 26V, 26.5V),Hard OVP protection circuit is triggered. the protection circuit immediately shorts both AC1 and AC2 pins to ground. HOVP condition releases when VRECT falls below certain voltage, depending on the VOUT set.

Table 5. HOVP release settings

VOUT target voltage(V)	HOVP release when VRECT less than (V)
< 12	10
12 ≤ VOUT < 15	13
15 ≤ VOUT < 18	16
≥ 18	19

SOVP Soft Over Voltage Protections

Two SOVP protections implemented in STWLC99

SOVP1 : In the event of VRECT pin ≥ 24V (Programmable 24V, 23.5V, 23V, 22.5V with 1V hysteresis) during power up, IEXT1 switch will be turned-on.

SOVP2: In the event of VRECT pin ≥ 24.5V (Programmable 25V, 24.5V, 24V, 23.5V with 1V hysteresis) during power up, IEXT2 switch will be turned-on.

SOVP1 and SOVP2 are released when VRECT<(SOVP1 threshold -1V).

SOVP would interrupt Firmware to issue EPT and provide the time needed for the ASK modulation.

Over-temperature protection

The STWLC99 is equipped with three over-temperature detection circuits based on different sources:

1) Internal temperature sensor

2) External NTC temperature sensor

3) TSHUT (hardware)

Over temperature protection (software) the signals coming from the internal temperature sensors are conditioned and routed to the ADC.

The temperature can be monitored in a dedicated register. When the temperature exceeds the set threshold level, it can turn off the Main voltage regulator (VOUT), EPT can be sent to Tx to stop power transfer.

The external sensor (ADC NTC) typically placed very close to the coil to detect the over temperature of the coil, the low-sided NTC of a resistor divider whose center tap is connected to the NTC pin (analog input), while the high-side resistor is connected to the VDD5P0 pin. The temperature threshold is programmable by GUI.

TSHUT comparator monitors the die temperature and turns off the Main voltage regulator (VOUT) when temperature exceeds set threshold level.

When TSHUT is triggered both rectifier low-side switches are turned on while high-side switches are turned-off.

The temperature threshold is programmable by GUI from 105°C to 135°C with 10°C step (10 °C hysteresis).

Over-current protection

ADC OCP : FW is periodically monitoring ADC data and once the current value exceeds set ADC OCP threshold, OCP INT can be triggered , and can turn-off VOUT and EPT can be sent to TX to stop power transfer.

5.8 Wireless power interface

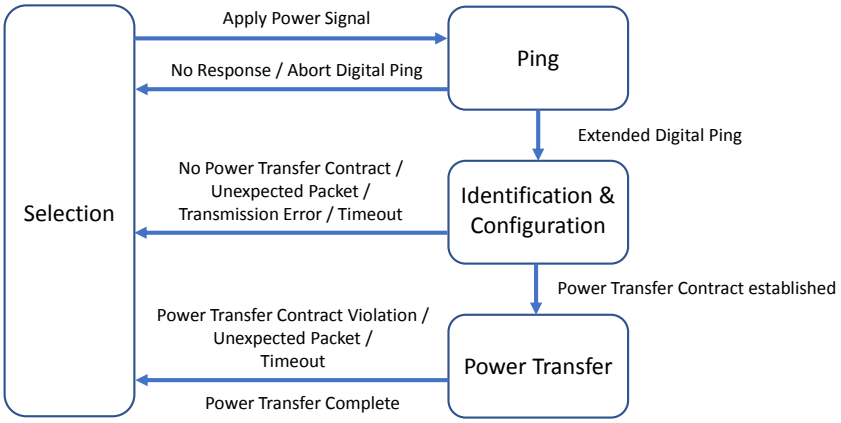
The blocks that refer to the wireless power interface are the synchronous rectifier, the main LDO linear regulator and the ASK modulator, as well as the digital core as supervisor. The power transfer from the transmitter to the receiver is established as a result of a procedure which consists of several distinct stages.

The power transfer begins after the transmitter has properly detected a valid receiver and a specific communication has been established between the two parts.

BPP

The flow-chart in below reports the whole process of power transfer in Baseline Power Profile (BPP up to 1A@5V)

Figure 2. Power transfer phases for Baseline Power Profile



- Digital ping: this phase is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation, the receiver device sends Signal strength packet.
- Identification & configuration: this phase is aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.
- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver.

EPP

The flow-chart in below shows the whole process leading to a power transfer in Extended Power Profile (EPP) up to 1.25A@12V

Figure 3. Power transfer phases for Extended Power Profile

Without entering the details of the different phases, the basic sequence of events taking place when a receiver is properly placed on the transmitting coil are summarized as:

- Digital ping: this phase is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation, the receiver device sends Signal strength packet.

- Identification & configuration: this phase is aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.
- Negotiation: in this phase the Power Receiver negotiates with the Power Transmitter to fine tune the Power Transfer Contract.
- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver

STWLC99 goes autonomously through Selection, Ping, Identification & Configuration phases, entering Power Transfer phase if no error occurs.

During the Power Transfer phase, the device sends Received-Power and Control-Error packets periodically as feedback information for the transmitter.

If a critical event like over-voltage, over-current or over-temperature occurs, the STWLC99 automatically sends the End-Power-Transfer packet.

When the Power Transfer is up and running, the End-Power-Transfer packet (with any response value) or any custom packet (e.g. Proprietary packet or Charge-Status packet) can be sent to the transmitter simply through commands via I^2C interface.

Sending a custom packet may result in a reply (either a data packet or a pattern response from the transmitter) or no reply at all: if a response is received, the content is captured and stored in specific I^2C registers.

Important notes:

- Changing the output voltage must respect the overall system design (selected coil, transmitter type, etc.).
- Output load transient response strongly depends on a correct design of the output capacitors. Severe load transients may lead to temporary output voltage collapse due to the overall TX-RX response time.
- A minimal output load significantly helps in increasing the signal-to-noise ratio during digital ping and is advisable to ensure interoperability with all transmitters.
- The initial load at power-up should not exceed 2.5 W, smoothly ramping-up to full power subsequently.

6 I2C interface

The STWLC99 can operate fully independently, i.e. without being interfaced with a host system.

In applications in which the STWLC99 has to be a part of peripherals managed by the host system, the two SDA and SCL pins could be connected to the existing I²C bus.

The device works as an I²C slave and supports standard (100 kbps) and fast (400 kbps) data transfer modes.

The I2CSEL pin allows setting default I2C address during power up. 7 bit I2C address 0x2B when pin is logic HIGH , 0x2C when pin is logic LOW.

When the bus is idle, both SDA and SCL lines are pulled HIGH.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high and low states of the SDA line can only change when the SCL clock signal is low.

Start and Stop Conditions

Both the SDA and the SCL lines remain high when the I^2C bus is not busy. A START condition is a high-to-low transition of the SDA line when SCL is HIGH, while the STOP condition is a low-to-high transition of the SDA line when SCL is HIGH. A STOP condition must be sent before each START condition.

Interface protocol

The interface protocol consists of

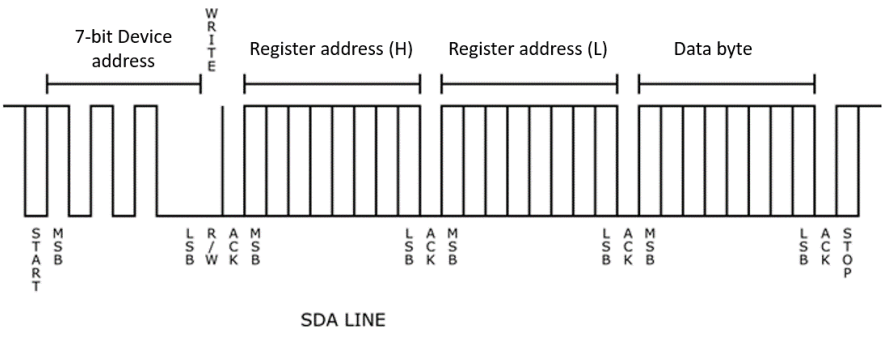
- Start condition (START)
- 7-bit device address + R/W bit (read = 1 / write = 0)
- Register pointer, high-byte
- Register pointer, low-byte
- Data sequence: N x (data byte + ACK)
- Stop condition (STOP)

The register pointer (or address) byte defines the destination register to which the read or write operation applies. When the read or write operation is finished, the register pointer is automatically incremented.

Writing to a single register

Writing to a single register begins with a START condition followed by device address (7-bit device address plus R/W bit cleared), two bytes of the register pointer and the data byte to be written in the destination register. Each transmitted byte is acknowledged by the STWLC99 through an ACK pulse.

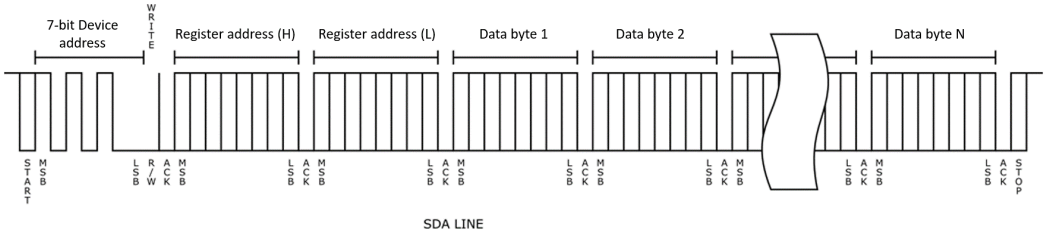
Figure 4. Writing to single register byte



Writing to multiple registers (page write)

The STWLC99 supports writing to multiple registers with auto-incremental addressing. When data is written into a register, the register pointer is automatically incremented, therefore transferring data to a set of subsequent registers (also know as page write) is a straightforward operation.

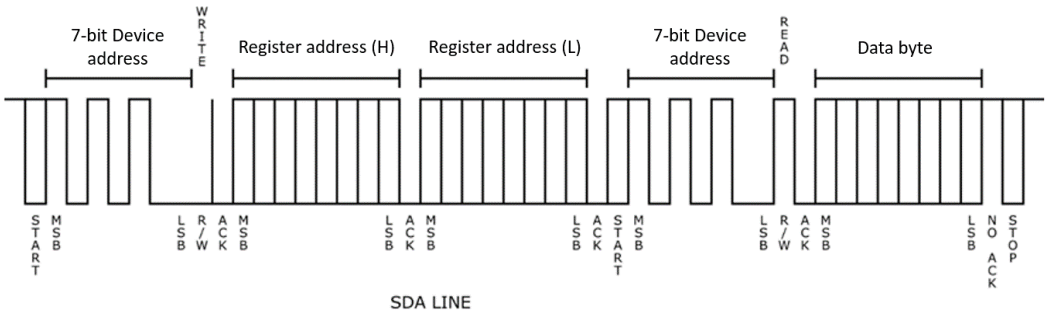
Figure 5. Writing multiple register bytes



Reading from a single register

Reading from a single register begins with a START condition followed by the device address byte (7-bit device address plus R/W bit cleared) and two bytes of register pointer, then a re-START condition is generated and the device address (7-bit device address plus R/W bit asserted) is sent, followed by data reading. ACK pulse is generated by the STWLC99 at the end of each byte, but not for data bytes retrieved from the register. A STOP condition is finally generated to terminate the operation.

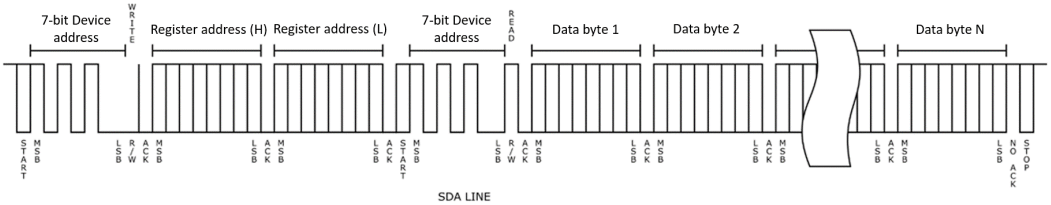
Figure 6. Reading single register byte



Reading from multiple registers (page reading)

Similarly to multiple (page) writing, reading from subsequent registers relies on an auto-increment of the register: the master can extend data reading to the following registers by generating and an ACK pulse at the end of each byte. Data reading starts immediately and the stream is terminated by a NACK pulse at the end of the last data byte, followed by a STOP condition.

Figure 7. Reading multiple bytes



7 I2C register map

The STWLC99 can be monitored and controlled by accessing the internal registers via I2C interface. The following registers map reports the accessible addresses. Addresses not shown in the map and blank bits have to be considered reserved and not altered as well.

Table 6. Register abbreviations

Register type	Description
R/W	can read and write the Bits
R	can read only
W	can write only

Table 7. Chip information

Register address	Register name	R/W	Default	Description
0x0000	Chip ID Low	R	0x63	Chip ID [7..0]
0x0001	Chip ID High	R	0x00	Chip ID [15..8]
0x0002	Chip revision	R	0x02	Chip revision [7..0]
0x0003	Customer ID	R	-	Customer ID [7..0]
0x0004	ROM ID	R	-	ROM ID [7..0]
0x0005	ROM ID	R	-	ROM ID [15..8]
0x0006	NVM Patch ID	R	-	NVM patch ID [7..0]
0x0007	NVM Patch ID	R	-	NVM patch ID [15..8]
0x0008	Patch ID	R	-	RAM Patch ID [7..0]
0x0009	Patch ID	R	-	RAM Patch ID [15..8]
0x000A	Configuration ID	R	-	Configuration ID [7..0]
0x000B	Configuration ID	R	-	Configuration ID [15..8]
0x000C	Production ID	R	-	PE ID [7..0]
0x000D	Production ID	R	-	PE ID [7..0]
0x008F	Operation mode	R	0x01	0x1: Standalone (debug) mode 0x2: Qi RX mode 0x3: Qi TX mode
0x0010 ..0 x001F	Device ID	R	-	Device ID Bytes 0 ...15

Table 8. System information

Register address	Register name	R/W	Default	Description
0x0020	System command	RW	-	Bit 0: Switch to TX command Write 1 to switch to Qi TX mode
		RW	-	Bit 1: Switch to RX command Write 1 to switch to Qi RX mode
			-	Bit 2..7 Reserved

Register address	Register name	R/W	Default	Description
0x002C,0x002D	System error	R	-	Bit 0: Core hard fault error 0: No hard fault error detected 1: Hard fault error detected
		R	-	Bit 1: HW WDT trigger latch 0: HW WDT not triggered 1: HW WDT triggered
		R	-	Bit 2: FTP IP error 0: No FTP IP error detected 1: FTP IP error detected
		R	-	Bit 3: MI2C error 0: No MI2C error detected 1: MI2C error detected
		R	-	Bit 4: FTP Boot error
		-	-	Bit [7..5] Reserved
		R	-	Bit [9..8] FTP PE error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [11..10] FTP Configuration error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [13..12] FTP Patch error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit[15..14]FTP Production Information error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved

Table 9. Communication

Register address	Register name	R/W	Default	Description
0x0038	DTS SEND LEN	RW	-	DTS ADS number of data bytes in stream
0x0039	DTS SEND RQ	RW	-	send ADC request Bits [4..0]
0x003A	DTS RCV LEN	RW	-	DTS ADS number of bytes in stream received
0x003B	DTS RCV RQ	RW	-	received ADC request Bits [4..0]

Table 10. **Mode monitor**

Register address	Register name	R/W	Default	Description
0x0040	RX ICUR	R	-	Output current in mA [7..0]
0x0041				[15..8]
0x0044	VRECT	R		Rectifier voltage in mV [7..0]
0x0045				[15..8]
0x0046	VOUT	R	-	Main LDO Voltage output in mV [7..0]
0x0047				[15..8]
0x0048	TMEAS	R	-	Chip temperature in deg C [7..0]
0xx049				[15..8]
0x003E	OP FREQ	R	-	Operating frequency in kHz [7..0]
0x003F				[15..8]
0x004C	NTC	R	-	NTC temperature measurement [7..0]
0x004D	Reserved			[15..0]
0x004A	ADC IN	R	-	ADC IN measurement [7..0]
0x004B				[15..8]
0x0054	POWER RX	R	-	RX received power in mW [7..0]
0x0055				[15..8]
0x0056				[23..16]
0x0057				[31..24]
0x0058	POWER TX	R	-	TX transferred power in mW[7..0]
0x0059				[15..8]
0x005A	POWER RPP	R		Last RP value sent
0x005B				[15..8]
0x005E	SIG STREN	R	-	[7..0]

Table 11. **GPIO**

Register address	Register name	R/W	Default	Description
0x0030	GPIO0 Function	RW	-	Set GPIO function. Please refer to user manual for detailed description.
0x0031	GPIO1 Function	RW	-	
0x0032	GPIO2 Function	RW	-	GPIO input, used for I2C select Floating/Logic HIGH : 0x2B Logic LOW: 0x2C
0x0033	GPIO3 Function	RW	-	GPIO output, used as Power good signal output pin High: LDO ON Low: LDO OFF
0x0034	GPIO4 Function	RW	-	GPIO input, used as Main LDO ON/OFF control High: Turn off MAIN LDO Low: Turn on MAIN LDO

Register address	Register name	R/W	Default	Description
0x0035	GPIO5 Function	RW	-	GPIO input, used as VOUTRX current level select High or floating - 3A Low - 5A
0x0036	GPIO6 Function	RW	-	INTN , Interrupt output (active low). Programmable open-drain. output used to generate an interrupt on specific events for the host controller.

Receiver mode (Rx) registers

Table 12. RX interrupts enable

Register address	Register name	R/W	Default	Description
0x0098	RX OVTP EN	RW	-	Bit 0: over temperature protection interrupt enable 0: disable 1: enable
	RX OCP EN	RW	-	Bit 1: over current protection interrupt enable 0: disable 1: enable
	RX OVP EN	RW	-	Bit 2: over voltage protection interrupt enable 0: disable 1: enable
	RX SYS ERROR EN	RW	-	Bit 3: system error interrupt enable 0: disable 1: enable
	RX SCP EN	RW	-	Bit4: short circuit protection 0: disable 1: enable
	RX MSG RCVD EN	RW	-	Bit 5: message received from TX 0: disable 1: enable
	RX OUTPUT ON EN	RW	-	Bit 6: output on interrupt enable 0: disable 1: enable
	RX OUTPUT OFF EN	RW	-	Bit 7: Output off interrupt enable 0: disable 1: enable
0x0099	RX SENT PACKET EN	RW	-	Bit 0: Packet sent interrupt enable 0: disable 1: enable
	RX SENT PKT TO EN	RW	-	Bit 1: Packet sending timeout interrupt enable 0: disable

Register address	Register name	R/W	Default	Description
0x0099				1: enable
	RX SIG STR EN	RW	-	Bit 2: Signal Strength sent interrupt enable 0: disable 1: enable
	RX VRECT RDY EN	RW	-	Bit 3: VRECT ready interrupt enable 0: disable 1: enable
	RX TX REMOV EN	RW	-	Bit 4 :TX removal is detected. I2C master should power down ext 5V upon interrupt. 0: disable 1: enable
	RX PWR TRANS RP24 NACK EN	RW	-	Bit 5: Received NACK for normal mode RP24 during power transfer 0: disable 1: enable
	Reserved	RW		Bit [7..6]: Reserved
0x009A	RX DTS SEND SUCCESS EN	RW	-	Bit 0: DTS sending data stream successfully interrupt enable 0: disable 1: enable
	RX DTS SEND TO END EN	RW	-	Bit 1: DTS stopped sending due to timeout error interrupt enable 0: disable 1: enable
	RX DTS RCVD SUCCESS EN	RW	-	Bit 2:DTS received data stream successful interrupt enable 0: disable 1: enable
	RX DTS RCVD TO END EN	RW	-	Bit 3: DTS stopped receiving due to timeout error interrupt enable
	Reserved			Bit [7..4] Reserved

Table 13. RX interrupts Clear

Register address	Register name	R/W	Default	Description
0x0094	RX OVTP CLR	R	-	Bit 0: over temperature protection clear 1: clear
	RX OCP CLR	R	-	Bit 1: over current protection clear 1: clear
	RX OVP CLR	R	-	Bit 2: over voltage protection clear 1: clear
	RX SYS ERROR CLR	R	-	Bit 3: system error clear 1: clear
	RX SCP CLR	R	-	Bit 4: short circuit protection clear

Register address	Register name	R/W	Default	Description
0x0094				1: clear
	RX MSG RCVD CLR	R	-	Bit 5: message received from TX clear 1: clear
	RX OUTPUT ON CLR	R	-	Bit 6: Output on interrupt clear 1: clear
	RX OUTPUT OFF CLR	R	-	Bit 7: Output off interrupt clear 1: clear
0x0095	RX SENT PACKET CLR	R	-	Bit 0: Packet sent interrupt clear 1: clear
	RX SENT PKT TO CLR	R	-	Bit 1: Packet sending timeout interrupt clear 1: clear
	RX SIG STR CLR	R	-	Bit 2: Signal Strength sent interrupt clear 1: clear
	RX VRECT RDY CLR	R	-	Bit 3: VRECT ready interrupt clear 1: clear
	RX TX REMOV CLR	R	-	Bit 4:TX removal is detected. I2C master should power down ext 5V upon interrupt clear 1: clear
	RX PWR TRANS RP24 NACK CLR	R	-	Bit 5:Received NACK for normal mode RP24 during power transfer clear 1: clear
	Reserved	R	-	Bit [7..6]: Reserved
0x0096	RX DTS SEND SUCCESS CLR	R	-	Bit0: DTS sending data stream successfully interrupt clear 1: clear
	RX DTS SEND TO END CLR	R	-	Bit 1: DTS stopped sending due to timeout error interrupt clear 1: clear
	RX DTS RCVD SUCCESS CLR	R	-	Bit 2:DTS received data stream successful interrupt clear 1: clear
	RX DTS RCVD TO END CLR	R	-	Bit 3: DTS stopped receiving due to timeout error interrupt clear 1: clear
		R	-	Bit [7..4]: Reserved

Table 14. RX interrupts latch

Register address	Register name	R/W	Default	Description
0x0090	RX OVTP LTCH	R	-	Bit 0: over temperature protection latch
	RX OCP LTCH	R	-	Bit 1: over current protection latch
	RX OVP LTCH	R	-	Bit 2: over voltage protection latch
	RX SYS ERROR LTCH	R	-	Bit 3: system error latch

Register address	Register name	R/W	Default	Description
0x0090	RX SCP LTCH	R	-	Bit 4: short circuit protection latch
	RX MSG RCVD LTCH	R	-	Bit 5: message received from TX latch
	RX OUTPUT ON LTCH	R	-	Bit 6: Output on interrupt latch
	RX OUTPUT OFF LTCH	R	-	Bit 7: Output off interrupt latch
0x0091	RX SENT PACKET LTCH	R	-	Bit 0: Packet sent interrupt latch
	RX SENT PKT TO LTCH	R	-	Bit 1: Packet sending timeout interrupt latch
	RX SIG STR LTCH	R	-	Bit 2: Signal Strength sent interrupt latch
	RX VRECT RDY LTCH	R	-	Bit 3: VRECT ready interrupt latch
	RX TX REMOV LTCH	R	-	Bit 4:TX removal is detected. I2C master should power down ext 5V upon interrupt latch
	RX PWR TRANS RP24 NACK LTCH	R	-	Bit 5:Received NACK for normal mode RP24 during power transfer latch
	Reserved	R	-	Bit [7..6]: Reserved
0x0092	RX DTS SEND SUCCESS LTCH	R	-	Bit 0: DTS sending data stream successfully interrupt latch
	RX DTS SEND TO END LTCH	R	-	Bit 1: DTS stopped sending due to timeout error interrupt latch
	RX DTS RCVD SUCCESS LTCH	R	-	Bit 2:DTS received data stream successful interrupt latch
	RX DTS RCVD TO END LTCH	R	-	Bit 3: DTS stopped receiving due to timeout error interrupt latch
	Reserved	R	-	Bit [7..4]: Reserved

Table 15. RX interrupts status

Register address	Register name	R/W	Default	Description
0x009C	RX OVTP STAT	R	-	Bit 0: over temperature protection status
	RX OCP STAT	R	-	Bit 1: over current protection status
	RX OVP STAT	R	-	Bit 2: over voltage protection status
	RX SYS ERROR STAT	R	-	Bit 3: system error status
	RX SCP STAT	R	-	Bit 4: short circuit protection status
	RX MSG RCVD STAT	R	-	Bit 5: message received from TX status
	RX OUTPUT ON STAT	R	-	Bit 6: Output on interrupt status
	RX OUTPUT OFF STAT	R	-	Bit 7: Output off interrupt status
0x009D	RX SENT PACKET STAT	R	-	Bit 0: Packet sent interrupt status
	RX SENT PKT TO STAT	R		Bit 1: Packet sending timeout interrupt status
	RX SIG STR STAT	R	-	Bit 2: Signal Strength sent interrupt status
	RX VRECT RDY STAT	R	-	Bit 3: VRECT ready interrupt status
	RX TX REMOV STAT	R	-	Bit 4:TX removal is detected. I2C master should power down ext 5V upon interrupt status
	RX PWR TRANS RP24 NACK STAT	R	-	Bit 5:Received NACK for normal mode RP24 during power transfer latch
	Reserved	R		Bit [7..6]: RESERVED

Register address	Register name	R/W	Default	Description
0x009E	RX DTS SEND SUCCESS STAT	R	-	Bit 0: DTS sending data stream successfully interrupt status
	RX DTS SEND TO END STAT	R	-	Bit 1: DTS stopped sending due to timeout error interrupt status
	RX DTS RCVD SUCCESS STAT	R	-	Bit 2: DTS received data stream successful interrupt status
	RX DTS RCVD TO END STAT		-	Bit 3: DTS stopped receiving due to timeout error interrupt status
		R	-	Bit [7..4]: Reserved

Table 16. RX commands

Register address	Register name	R/W	Default	Description
0x00A0	RX VOUT ON	RW	-	Bit 0: Turn on the VOUT. If both VOUT_ON and VOUT_OFF are set to 1, this command is ignored and both requests are cleared.
	RX VOUT OFF	RW	-	Bit 1: Turn off the VOUT. If both VOUT_ON and VOUT_OFF are set to 1, this command is ignored and both requests are cleared.
	RX SEND MSG	RW	-	Bit 2 : Write 1 to send custom ASK packet. The message data is defined in the SEND_MSG_DTS registers.
	RX SEND MSG WAIT REPLY	RW	-	Bit 3: Write 1 to send custom ASK packet that expects TX FSK reply. The message data is defined in the SEND_MSG_DTS registers.
	RX SEND EPT	RW	-	Bit 4:Write 1 to send a End of Power Transfer packet to TX. The EPT message is defined in RX_EPT_MSG register.
	RX SEND DTS	RW	-	Bit 5:Write 1 to start DTS sending transaction. DTS data is specified in SEND_MSG_DTS registers and should be kept there until DTS session ends.

Table 17. RX configuration

Register address	Register name	R/W	Default	Description
0x00AA	RX VOUT SET	RW	-	VOUT_SET [7:0] Byte 0
0x00AB		RW	-	VOUT_SET[15:8] Byte 1 Step size 25mV
0x00B2	ILIM SET	RW	-	Program current limit and regulation from 100mA to 2.5A with step of 100mA
0x00B3	ARC THRESH	RW	-	Adaptive rectifier mode auto off threshold setting with step of 100mV

Table 18. **RX LDO configuration**

Register address	Register name	R/W	Default	Description
0x00A5	LDO DROP 0	RW		LDO target voltage drop at 0mA IOUT. Specified in 16mV units, set point 0
0x00A6	LDO DROP 1	RW		LDO target voltage drop at ldo_cur_thres1 IOUT. Specified in 16mV units, set point 1
0x00A7	LDO DROP 2	RW		LDO target voltage drop at ldo_cur_thres2 IOUT. Specified in 16mV units, set point 2
0x00A8	LDO DROP 3			LDO target voltage drop at ldo_cur_thres3 IOUT. Specified in 16mV units, set point 3
0x00A2	LDO CUR TH1	RW		LDO voltage drop IOUT current threshold 1. Specified in 10mA units.
0x00A3	LDO CUR TH2	RW		LDO voltage drop IOUT current threshold 2. Specified in 10mA units.
0x00A4	LDO CUR TH3	RW		LDO voltage drop IOUT current threshold 3. Specified in 10mA units.

Table 19. **RX FOD configuration**

Register address	Register name	R/W	Default	Description
0x0060	FOD CUR THR1	RW	-	FOD current threshold 1 [7..0], in units of 10mA.
0x0061				[15..8]
0x0062	FOD CUR THR2	RW	-	FOD current threshold 2[7..0], in units of 10mA.
0x0063				[15..8]
0x0064	FOD CUR THR3	RW	-	FOD current threshold 3, in units of 10mA.
0x0065				[15..8]
0x0066	FOD CUR THR4	RW	-	FOD current threshold 4, in units of 10mA.
0x0067				[15..8]
0x0068	FOD CUR THR5	RW	-	FOD current threshold 5, in units of 10mA.
0x0069				[15..8]
0x006A	FOD CUR THR6	RW	-	FOD current threshold 6, in units of 10mA.
0x006B				[15..8]
0x006C	FOD CUR THR7	RW	-	FOD current threshold 7, in units of 10mA.
0x006D				[15..8]
0x006E	FOD CUR THR8	RW	-	FOD current threshold 8, in units of 10mA.
0x006F				[15..8]
0x0070	FOD OFFS0	RW	-	Signed FOD offset0 in units of 32mW. 0 - 0mW 1 - 32mW… 127 - 4064mW -1 - -32mW… -128 - 4096mW
0x0071	FOD OFFS1	RW	-	FOD offset 1
0x0072	FOD OFFS2	RW	-	FOD offset 2
0x0073	FOD OFFS3	RW	-	FOD offset 3
0x0074	FOD OFFS4	RW	-	FOD offset 4
0x0075	FOD OFFS5	RW	-	FOD offset 5

Register address	Register name	R/W	Default	Description
0x0076	FOD OFFS6	RW	-	FOD offset 6
0x0077	FOD OFFS7	RW	-	FOD offset 7
0x0078	FOD OFFS8	RW	-	FOD offset 8
0x0079	FOD RSER	RW	-	Coil series resistance, specified in units of 4mOhm.
0x007A	FOD GAIN OFFSET	RW	-	FOD Gain scaler offset 0, at current 0, base is 512, default scaler is 512. Specify this value as signed (2'complement) offset.

Table 20. TX Interrupt enable

Register address	Register name	R/W	Default	Description
0x00C8	TX OVTP EN	RW	-	Bit 0: over temperature protection enable 0: disable 1: enable e
	TX OCP EN	RW	-	Bit 1: over current protection enable 0: disable 1: enable
	TX OVP EN	RW	-	Bit 2: over voltage protection enable 0: disable 1: enable
	TX SYS ERR EN	RW	-	Bit 3: system error enable 0: disable 1: enable
	TX RP PKT RCVD EN	RW	-	Bit 4: RP packet received interrupt enable 0: disable 1: enable
	TX CE PKT RCVD EN	RW	-	Bit 5: CE packet received interrupt enable 0: disable 1: enable
	TX SEND PKT EN	RW	-	Bit 6: Packet sent interrupt enable 0: disable 1: enable
	TX EXT MON EN	RW	-	Bit 7: Ext Tx Detect interrupt enable 0: disable 1: enable
0x00C9	TX CEP TO EN	RW	-	Bit 0: CEP Timeout interrupt enable 0: disable 1: enable
	TX RPP TO EN	RW	-	Bit 1: RPP Timeout interrupt enable 0: disable 1: enable

Register address	Register name	R/W	Default	Description
0x00C9	TX EPT EN	RW	-	Bit 2: AC powered down interrupt enable 0: disable 1: enable
	TX START PING EN	RW	-	Bit 3: Ping started interrupt enable 0: disable 1: enable
	TX SS PKT RCVD EN	RW	-	Bit 4: SS ID packet received interrupt enable 0: disable 1: enable
	TX ID PKT RCVD EN	RW	-	Bit 5: ID packet received interrupt enable 0: disable 1: enable
	TX CFG PKT RCVD EN	RW	-	Bit 6: Configuration packet received interrupt 0: disable 1: enable
	TX PP PKT RCVD EN	RW	-	Bit 7: PP packet received interrupt enable 0: disable 1: enable
0x00CA	TX BRIDGE MD EN	RW	-	Bit 0: Bridge mode (half/full) changed interrupt. 0: disable 1: enable
	TX FOD DET EN	RW	-	Bit 1: Tx FOD detect interrupt enable 0: disable 1: enable
	TX PP PKT UPDATE EN	RW	-	Bit 2: the power transfer contract is successfully updated after negotiation/renegotiation 0: disable 1: enable
	TX DTS SEND SUC EN	RW	-	Bit 3: DTS sending data stream successfully interrupt enable 0: disable 1: enable
	TX DTS SEND END TO EN	RW	-	Bit 4:DTS stopped sending due to timeout error interrupt enable 0: disable 1: enable

Table 21. TX Interrupt clear

Register address	Register name	R/W	Default	Description
0x00C4	TX OVTP CLR	R	-	Bit 0: over temperature protection clear 1: clear
	TX OCP CLR	R	-	Bit 1: over current protection clear

Register address	Register name	R/W	Default	Description
0x00C4				1: clear
	TX OVP CLR	R	-	Bit 2: over voltage protection clear 1: clear
	TX SYS ERR CLR	R	-	Bit 3: system error clear 1: clear
	TX RP PKT RCVD CLR	R	-	Bit 4: RP packet received interrupt clear 1: clear
	TX CE PKT RCVD CLR	R	-	Bit 5: CE packet received interrupt clear 1: clear
	TX PKT SENT CLR	R	-	Bit 6: Packet sent interrupt clear 1: clear
	TX EXT MON CLR	R	-	Bit 7: Ext Tx Detect interrupt clear 1: clear
0x00C5	TX CEP TO CLR	R	-	Bit 0: CEP Timeout interrupt clear 1: clear
	TX RPP TO CLR	R	-	Bit 1: RPP Timeout interrupt clear 1: clear
	TX EPT CLR	R	-	Bit 2: AC powered down interrupt clear 1: clear
	TX START PING CLR	R	-	Bit 3: Ping started interrupt clear 1: clear
	TX SS PKT RCVD CLR	R	-	Bit 4: SS ID packet received interrupt clear 1: clear
	TX ID PKT RCVD CLR	R	-	Bit 5: ID packet received interrupt clear 1: clear
	TX CFG PKT RCVD CLR	R	-	Bit 6: Configuration packet received interrupt clear 1: clear
	TX PP PKT RCVD CLR	R	-	Bit 7: PP packet received interrupt clear 1: clear
0x00C6	TX BRIDGE MD CLR	R	-	Bit 0: Bridge mode (half/full) changed interrupt clear
	TX FOD DET CLR	R	-	Bit 1: Tx FOD detect interrupt clear
	TX PP PKT UPDATE CLR	R	-	Bit 2: the power transfer contract is successfully updated after negotiation/renegotiation clear
	TX DTS SEND SUC CLR	R	-	Bit 3: DTS sending data stream successfully interrupt clear
	TX DTS SEND END TO CLR	R	-	Bit 4:DTS stopped sending due to timeout error interrupt clear

Table 22. **TX interrupt latch**

Register address	Register name	R/W	Default	Description
0x00C0	TX OVTP LTCH	R	-	Bit 0: over temperature protection latch 1: latch
	TX OCP LTCH	R	-	Bit 1: over current protection latch 1: latch
	TX OVP LTCH	R	-	Bit 2: over voltage protection latch 1: latch
	TX SYS ERR LTCH	R	-	Bit 3: system error latch 1: latch
	TX RP PKT RCVD LTCH	R	-	Bit 4: RP packet received interrupt latch 1: latch
	TX CE PKT RCVD LTCH	R	-	Bit 5: CE packet received interrupt latch 1: latch
	TX SENT PKT LTCH	R	-	Bit 6: Packet sent interrupt latch 1: latch
	TX EXT MON LTCH	R	-	Bit 7: Ext Tx Detect interrupt latch 1: latch
0x00C1	TX CEP TO LTCH	R	-	Bit 0: CEP Timeout interrupt latch 1: latch
	TX RPP TO LTCH	R	-	Bit 1: RPP Timeout interrupt latch 1: latch
	TX EPT LTCH	R	-	Bit 2: AC powered down interrupt latch 1: latch
	TX START PING LTCH	R	--	Bit 3: Ping started interrupt latch 1: latch
	TX SS PKT RCVD LTCH	R	-	Bit 4: SS ID packet received interrupt latch 1: latch
	TX ID PKT RCVD LTCH	R	-	Bit 5: ID packet received interrupt latch 1: latch
	TX CFG PKT RCVD LTCH	R	-	Bit 6: Configuration packet received interrupt latch 1: latch
	TX PP PKT RCVD LTCH	R	-	Bit 7: PP packet received interrupt latch 1: latch
0x00C2	TX BRIDGE MD LTCH	R	-	Bit 0: Bridge mode (half/full) changed interrupt latch
	TX FOD DET LTCH	R	-	Bit 1: Tx FOD detect interrupt latch
	TX PP PKT UPDATE LTCH	R	-	Bit 2: the power transfer contract is successfully updated after negotiation/renegotiation latch
	TX DTS SEND SUC LTCH	R	-	Bit 3: DTS sending data stream successfully interrupt latch
	TX DTS SEND END TO LTCH	R	-	Bit 4:DTS stopped sending due to timeout error interrupt latch

Table 23. **TX Interrupt status**

Register address	Register name	R/W	Default	Description
0x00CC	TX OVTP STAT	R	-	Bit 0: over temperature protection status
	TX OCP STAT	R	-	Bit 1: over current protection status
	TX OVP STAT	R	-	Bit 2: over voltage protection status
	TX SYS ERR STAT	R	-	Bit 3: system error status
	TX RP PKT RCVD STAT	R	-	Bit 4: RP packet received interrupt status
	TX CE PKT RCVD STAT	R	-	Bit 5: CE packet received interrupt status
	TX SENT PKT STAT	R	-	Bit 6: Packet sent interrupt status
	TX EXT MON STAT	R	-	Bit 7: Ext Tx Detect interrupt status
0x00CD	TX CEP TO STAT	R	-	Bit 0: CEP Timeout interrupt status
	TX RPP TO STAT	R	-	Bit 1: RPP Timeout interrupt status
	TX EPT STAT	R	-	Bit 2: AC powered down interrupt status
	TX START PING STAT	R	-	Bit 3: Ping started interrupt status
	TX SS PKT RCVD STAT	R	-	Bit 4: SS ID packet received interrupt status
	TX ID PKT RCVD STAT	R	-	Bit 5: ID packet received interrupt status
	TX CFG PKT RCVD STAT	R	-	Bit 6: Configuration packet received interrupt status
	TX PP PKT RCVD STAT	R	-	Bit 7: PP packet received interrupt status
0x00CE	TX BRIDGE MD STAT	R	-	Bit 0: Bridge mode (half/full) changed interrupt status
	TX FOD DET STAT	R	-	Bit 1: Tx FOD detect interrupt status
	TX PP PKT UPDATE STAT	R	-	Bit 2: the power transfer contract is successfully updated after negotiation/renegotiation status
	TX DTS SEND SUC STAT	R	-	Bit 3: DTS sending data stream successfully interrupt status
	TX DTS SEND END TO STAT	R	-	Bit 4:DTS stopped sending due to timeout error interrupt status

Table 24. **TX configuration**

Register address	Register name	R/W	Default	Description
0x00D2,0x00D3	TX FREQ MAX	RW	-	Bits [7…0] Max frequency specified in units of 16Hz
				Bit [15..8]
0x00D4,0x00D5	TX FREQ MIN	RW	-	Bits [7…0] Min frequency specified in units of 16Hz
				Bit [15..8]
0x00D6,0x00D7	TX FREQ PING	RW	-	Bits [7…0] Ping frequency specified in units of 16Hz
				Bit [15..8]
0x00D8	TX DC MAX	RW	-	Bits [7…0] Max Tx duty cycle %. Max value is 50. Must be >= TX_MIN_DC
0x00D9	TX DC MIN	RW	-	Bits [7…0] Min Tx duty cycle %. Must be <= TX_MAX_DC

Register address	Register name	R/W	Default	Description
0x00DA	TX DC PING	RW	-	Bits [7…0] Ping duty cycle in percentage
0x00DB	TX PING INTVAL	RW	-	Bits [7…0] Ping interval , step size 10ms.
0x00DC	TX PING DURATION	RW	-	Bits [7…0] Tx ping duration in ms.
0x00E0	TX PLOSS FOD THR	RW	-	Bits [7…0] Tx PLOSS FOD detection threshold in 32mW units. 0 - Disable 1 - 32mW … 255 - 8160mW
0x00E1	TX FOD DBNC CNT	RW	-	Bits [7…0] Continuous PLOSS based RP de bounce count before FOD EPT. 0 - EPT immediately
0x00E2	TX CE TO MAX	RW	-	Bits [7…0] Max count TX retries with different frequency after failing to listen to CE packet within time frame.
0x00E3	TX RP TO MAX	RW	-	Bits [7…0] Max count TX retries after failing to listen to RP packet within time frame.
0x00E4	TX FHOP	RW	-	Bits [7…0] Define the step size (in Hz) for every frequency hop. Internally it is multiplied with 128 1: 128Hz step size 2: 256Hz step size 3: 384Hz step size ….

Table 25. TX EPT reason

Register address	Register name	R/W	Default	Description
0x0E7	TX OVP	R	-	Bit 0: over voltage protection triggered
	TX OCP	R	-	Bit 1: over current protection triggered
	TX OVTP	R	-	Bit 2: over temperature protection triggered
	TX FOD	R	-	Bit 3: Foreign object detected
	TX HOST	R	-	Bit 4: Host issued EPT command
	TX RX EPT	R	-	Bit 5: EPT Source Rx EPT packet
	TX CEP TO	R	-	Bit 6: Control error packet timeout
	TX RPP TO	R	-	Bit 7: Received power packet timeout
0x00E8	TX RX RST	R	-	Bit 0: Rx send SS/ID/CFG at wrong time , probably because of RX RESET
	TX SYS ERR	R	-	Bit 1: System error
	TX SS TO	R	-	Bit 2: Signal strength timeout
	TX SS ERR	R	-	Bit 3: Signal strength packet error
	TX ID ERR	R	-	Bit 4: Identification packet error
	TX CFG	R	-	Bit 5: Error in configuration packet
	TX CFG CNT	R	-	Bit 6: Number optional packets received doesn't match with number in configuration packet
	TX PCH ERR	R	-	Bit 7: Power control hold-off packet error
0x00E9	TX XID ERR	RW	-	Bit 0: Extended identification packet error
	TX NEG ERR	RW	-	Bit 1:Negotiation error
	TX NEGO TO	RW	-	Bit 2 :Negotiation time out

Table 26. **TX protections**

Register address	Register name	R/W	Default	Description
0x00DD	TX OVP THRES	RW	-	Bit [7…0] Specify Tx OVP threshold in 500mV units.
0x00DE	TX OCP THRES	RW	-	Bit [7…0] Specify Tx OCP current in 100mA units.0 - Disable1 - 100mA…
0x00DF	TX OVTP THRES	RW	-	Bit [7 …0] Over temperature protection threshold in degree C. If transmitter die temperature rises above this value, then OTP triggered.

Table 27. **Auxiliary Data**

Register address	Register name	R/W	Default	Description
0x0100	AUX DATA 00	RW	-	auxiliary data 000 / send dts 000
…..				
0x017F	AUX DATA 127	RW	-	auxiliary data 127 / send dts 127
0x0180	AUX DATA 128	R	-	auxiliary data 128 / receive dts 000
….				
0x01FF	AUX DATA 255	R	-	auxiliary data 255 / receive dts 127
0x0200	AUX DATA 256	RW	-	auxiliary data 256 / send message 00
….				
0x0215	AUX DATA 277	RW	-	auxiliary data 277 / send message 21
0x0216	AUX DATA 278	R	-	auxiliary data 278/ receive message 00
….				
0x22B	AUX DATA 299	R	-	auxiliary data 299/ receive message 21
0x022C	AUX DATA 300	RW	-	auxiliary data 300/mi2c write buffer 00
….				
0x023B	AUX DATA 315	RW	-	auxiliary data 315/mi2c write buffer 15
0x023C	AUX DATA 316	R	-	auxiliary data 316/mi2c read buffer 00
….				
0x024B	AUX DATA 331	R	-	auxiliary data 331/mi2c read buffer 15

8 Application information

This chapter is aimed to provide some application hints. The reference schematic, the PCB layout guidelines, the minimum components to properly run the application and other aspects.

8.1 Reference application

STWLC99 typical application schematic for Rx and Tx modes are shown below.

Typical component values for a power receiver capable of 100W output power are listed in the tables below.

Figure 8. STWLC99 basic application diagram in Rx Tx mode

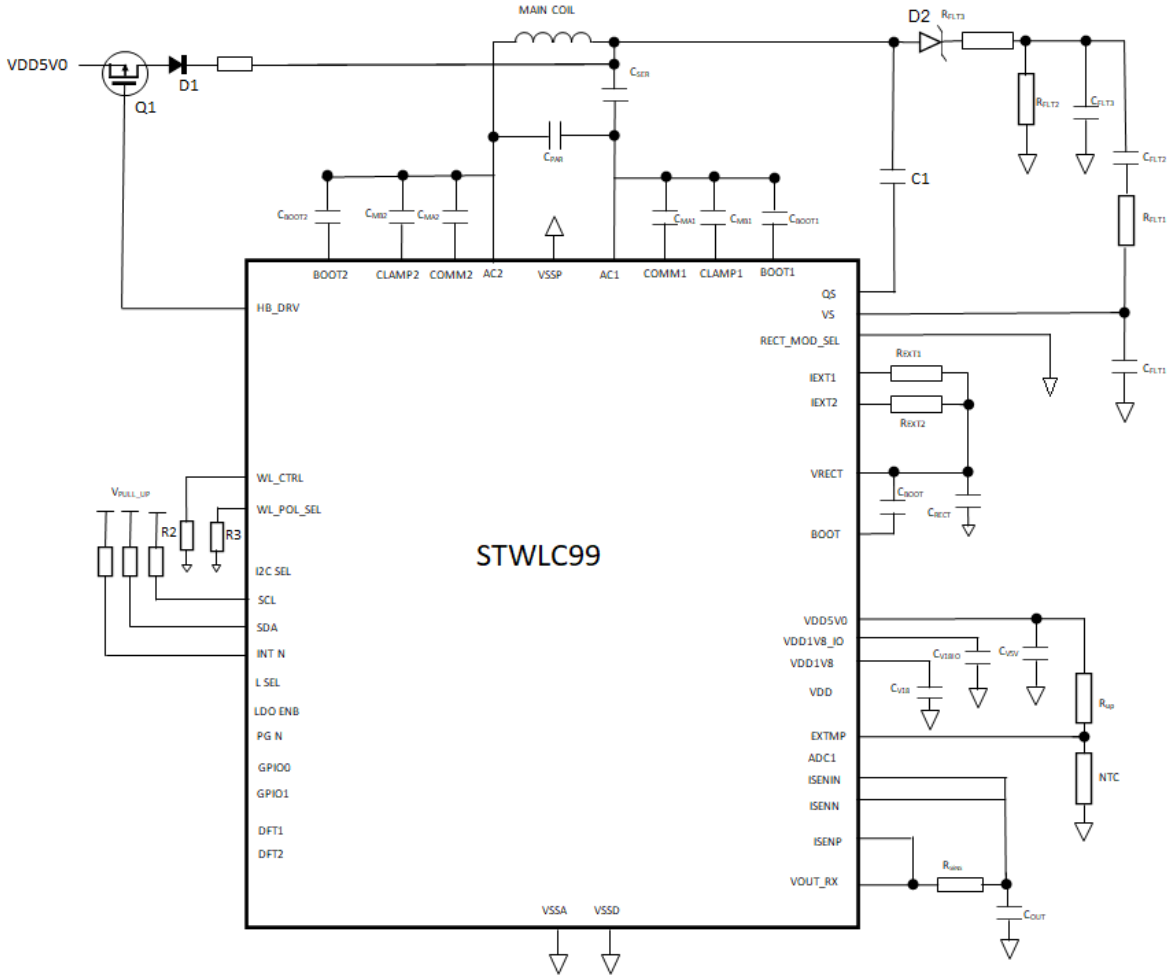


Table 28. Typical components list for a 100 W RTx application

Component	Value	Manufacturer	Part Number	Notes
LS	4µH	Luxshare		Receiving coil
CSER	220nF/50V	Murata	9x GRM188R71H224KAC4D	Series resonant capacitor
CPAR	3.3nF/50V	SEMCO	CL10B332KB8NNND	Parallel resonant capacitor
CBOOT1, CBOOT2	47nF/50V	SEMCO	CL10B473KB8NNND	Boot strap capacitor
CBOOT	4.7nF/50V	SEMCO	CL10B472KB8NNND	Boot strap capacitor

Component	Value	Manufacturer	Part Number	Notes
COMM1,COMM2	22nF/50V	SEMCO	CL10B223KB8NNND	ASK modulation capacitors
CLAMP1,CLAMP2	47nF/50V	SEMCO	CL10B473KB8NNND	ASK modulation capacitors
CV5V0	4.7uF/16V	SEMCO	CL10A475KO8NNNC	V5V0 filtering capacitor
CV1V8	1µF/25V	SEMCO	CL10B105KQ8NNND	V1V8 filtering capacitors
CV1V8IO	0.1µF/50V	SEMCO	CL10B104KB8NNND	V1V8IO filtering capacitors
CRECT	10µF/50V	SEMCO	6x CL31B106KBHNNNE	VRECT filter capacitor, rating depending on application
COUT	10µF/50V	SEMCO	3 x CL31B106KBHNNNE	OUT filter capacitor, rating depending on application
REXT1	200R		2x RS-05K2000FT	clamping resistor
REXT2	200R		2x RS-05K0910FT	clamping resistor
RUP	30K		30K	
RNTC			100K	Optional
Q1			DMP6350S	
RFLT1,2,3			6K8,220K,10K	ASK demod filter resistors
D1,D2			BAT41KFILM	ASK demod , Q factor circuit,
D8			APHD1608LCGCK	LED
D9			APHD1608LSURCK	LED
CFLT1,2,3			3.3nF,22nF,1.5nF	ASK demod filter capacitors
C1			470pF	
RSENSE			5 mohm	CFN0603-FZ-R005ELF

Note: All of the components listed above refer to a typical application. Operation in the application may be limited by a choice of these external components (voltage ratings, current and power dissipation capability, etc.).

The basic application schematic is relatively simple, since STWLC99 does not require many external parts to operate. Anyway, there are different aspects that must be carefully considered to properly design a customized application. In most cases the main constrains are limited PCB size/room and thickness, that unavoidably lead to crowded solutions with a far-from-optimal electrical and thermal performance.

8.2 External components selection

RX series resonant circuit components

Series resonant circuit, both Cs and Cd should show excellent quality factor, relatively high RMS current capability and superior capacitance stability in the frequency range of interest.

Multi-Layer Ceramic capacitors (MLCCs) are inherently good devices in terms of RMS current capability and quality factor. Capacitance tolerance and stability strongly depend on the dielectric type.

Dielectrics such as X5R ,X7R,COG are used to achieve higher capacitance per volume at the cost of lower accuracy and undesired dependencies (e.g. DC-biasing, temperature, etc.).

In practice, the C_S(most critical) usually consists of a few smaller, low-profile X5R/X7R capacitors connected in parallel. The parallel connection also helps to increase RMS current capability and mitigate the effect of capacitance tolerance due to production spread.

The voltage rating for these capacitors is usually maximized to take into account the voltage developed in proximity to resonance: 50V-rated capacitors are generally a good choice.

ASK modulation capacitors

The capacitors at the COMMx/CLAMPx pins are connected to the AC1-AC2 terminals through controlled switches (ASK modulator): the de-tuning effect of closing these switches results in an amplitude modulation detected by the transmitter and also visible at the rectified voltage.

Positive or negative modulation may occur, depending on the operating frequency and other factors.

The ASK modulation index clearly depends on the capacitance value of these capacitors, whose value has to be adjusted in case of a heavy negative modulation at VRECT (that is generally undesirable).

The same considerations made above for the resonant capacitors is also applicable here, where capacitance tolerance is less critical: X5R dielectric-type are a good choice and an initial value of 22 nF and 47nF is typically doing the job.

VRECT over-voltage clamping resistor

The voltage at the VRECT pin is primarily dictated by the transmitter, whose operating point is linked to the feedback information received via ASK modulation.

Unexpected conditions, however, may increase the VRECT voltage to dangerous values (close to AMR levels). A sudden change in relative alignment between the transmitting and receiving coils, for example, could result in a dramatic change in coupling factor and, in turn, a fast-rising voltage.

Since the reaction of the transmitter is relatively slow, the STWLC99 protects itself by closing the switch internally connected to the IEXT1,IEXT2 pins. The switch is externally connected to VRECT via a resistor ($R_{EXT1,EXT2}$) to implement an active clamper.

The value of $R_{EXT1,EXT2}$ is selected so that most of the power is dissipated in the clamper circuit rather than inside of the chip. Special resistors (surge resistors) capable of withstanding higher energy pulses are recommended.

ESD protection diodes

Since the receiving coil is a easy entry point for ESD (relatively large area with remarkable capacitive coupling), a good application design should consider protections for the most exposed pins: AC1 and AC2.

Uni-directional Transient Voltage Suppression (TVS) diodes at both pins are recommended.

ESDs have essentially a common-mode nature and, although the receiving coil has low DC-resistance, its AC impedance may appear quite high to fast voltage spikes: independent clamping at AC1 and AC2 pins is thus mandatory.

The knee-voltage of the TVS diodes should be selected considering the maximum VRECT voltage plus some margin to avoid non-negligible leakage current at higher temperature, while their energy dissipation capability should be maximized considering the size of the package.

Coil thermal protection

Maximizing the amount of transferred power is ofter desirable, but also limited by operating conditions : applications in which the wireless power receiver has poor power dissipation capability and/or the power loss in the receiving coil is relevant (e.g. very tiny and slim coils with relatively high DC-resistance) may require some thermal protection.

This feature is implemented with STWLC99 thanks to its NTC pin. A channel of the internal ADC is routed to the NTC pin, allowing the user to read the voltage across an external NTC thermistor.

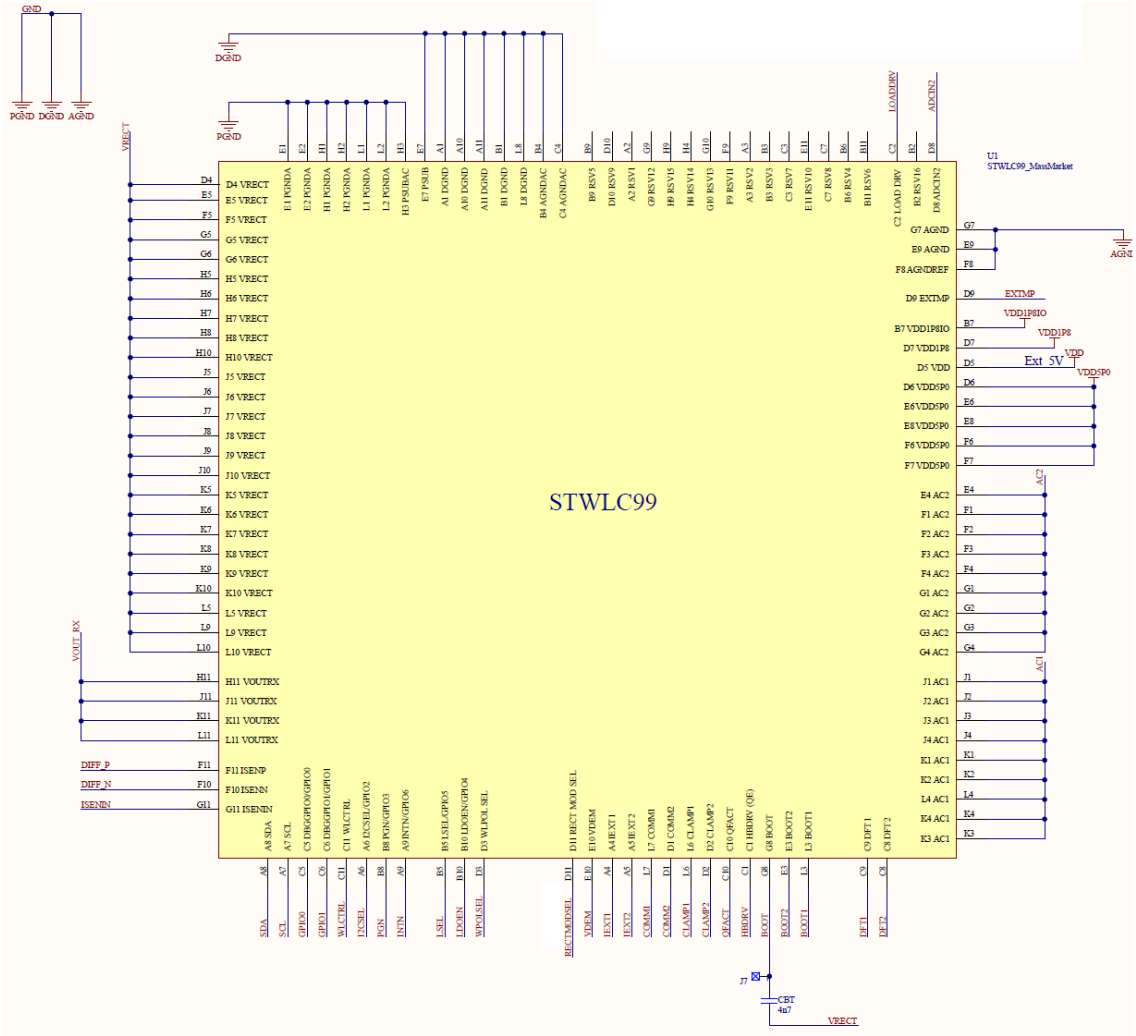
8.3 PCB routing guidelines

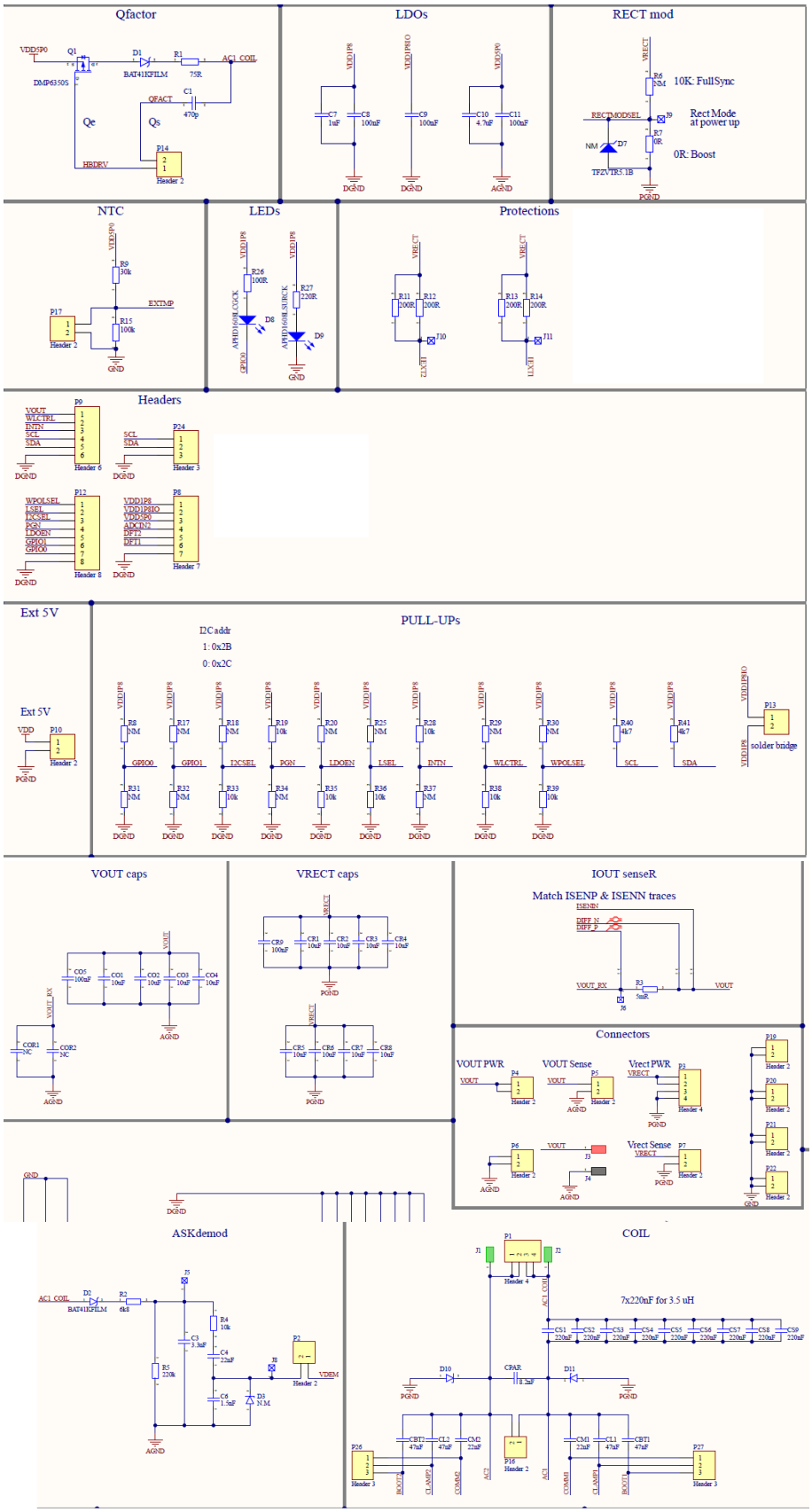
1. Power traces (AC1, AC2, VRECT, VOUT) and power ground traces should be kept wide enough to sustain high current. Duplicating these traces in inner layers , adding vias is advisable wherever possible to lower impedance as low as possible.
2. AC1, AC2, BOOT1, BOOT2, COMx, CLAMPx are some source of noise in the board Good Shielding of these traces (by running ground planes below).
3. Power ground(VSSP) will carry the sum of ripple current from V_{RECT}/$C_{RECT}$and DC current from VOUT/ Load, return paths from LDO caps should avoid these high currents.
4. AC1 and AC2 tracks should be routed closely to minimize the area of the resulting loop.
5. Communication signals (I2C), Sensing and Input monitoring signals to be routed away from High di/dt (AC1,AC2, COMMx, CLAMPx, BOOT) switching signals , to Minimize interference.
6. COMM1,COMM2,BOOT1,BOOT2 capacitors should be placed close to the device.
7. CRECT and COUT capacitors should be placed close to device , to avoid large current loops.
8. Auxiliary LDO capacitors C5v0 ,C1v8 and Cv1P8IO should be placed as close as possible to the device.
9. Tracks connection should be short and placed in top layer. Capacitors ground can be connected directly into GND plane.
10. Thermal performance and grounding should be optimized by preserving bottom layer (usually assigned to ground) integrity.
11. current sensing resistor to be placed as close possible to the device, ensure differential Positive and Negative current traces are balanced and use short traces.

8.4 Reference schematic

Typical application schematic for the STWLC99 is shown below. The values reported in and refer to typical Wireless Power Receiver applications capable of an output power of 100W respectively.

Figure 9. STWLC99 basic schematic diagram





Note: All the above components refer to a typical application. Operation of the device in the application may be limited by the choice of these external components (voltage ratings, current and power dissipation capability, etc.).

8.5 Glossary/Abbreviations

- ADC: Auxiliary Data Control
- ADT : Auxiliary Data Transport
- ASK: Amplitude Shift Keying
- BPP : Baseline Power Profile
- CHS : Charge Status
- CEP: Control Error Packets
- CFG : Configuration
- DSR : Data Stream Response
- DTS : Data Transport Stream
- EPP: Extended Power Profile
- EPT: End Power Transfer
- FOD : Foreign Object Detection
- FSK: Frequency Shift Keying
- ID: Identification
- PCH: Power Control Hold-off
- PP: Proprietary Packet
- RP/RP8: Received Power Packet
- SRQ : Specific Request
- SS/SIG : Signal Strength Packet
- XID : Extended Identification

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Package information

Figure 10. WLCSP121 4.859mmx4.859mm 0.4 Pitch 0.25 Ball package outline

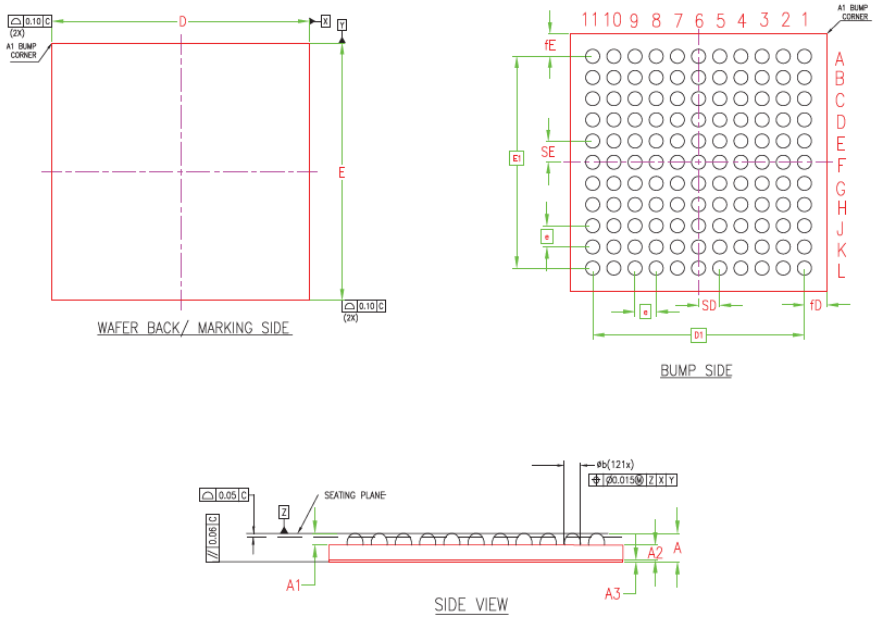
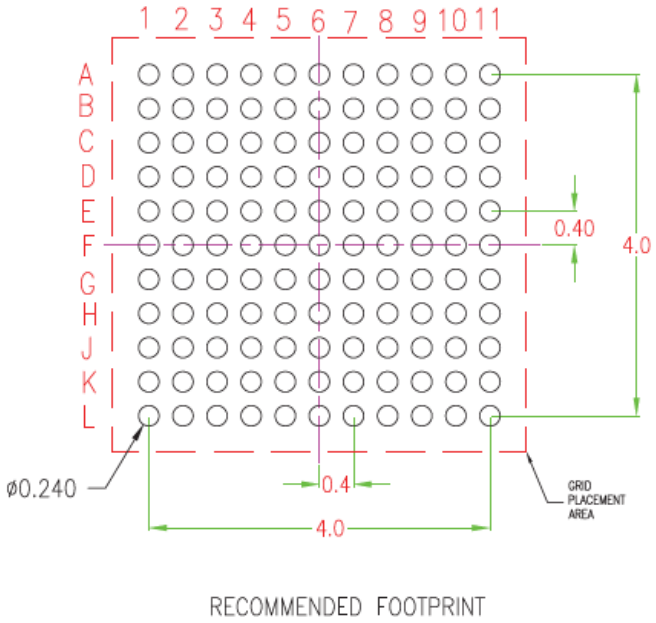


Table 29. **WLCSP121 4.859mmx4.859mm 0.4 Pitch 0.25 Ball mechanical data**

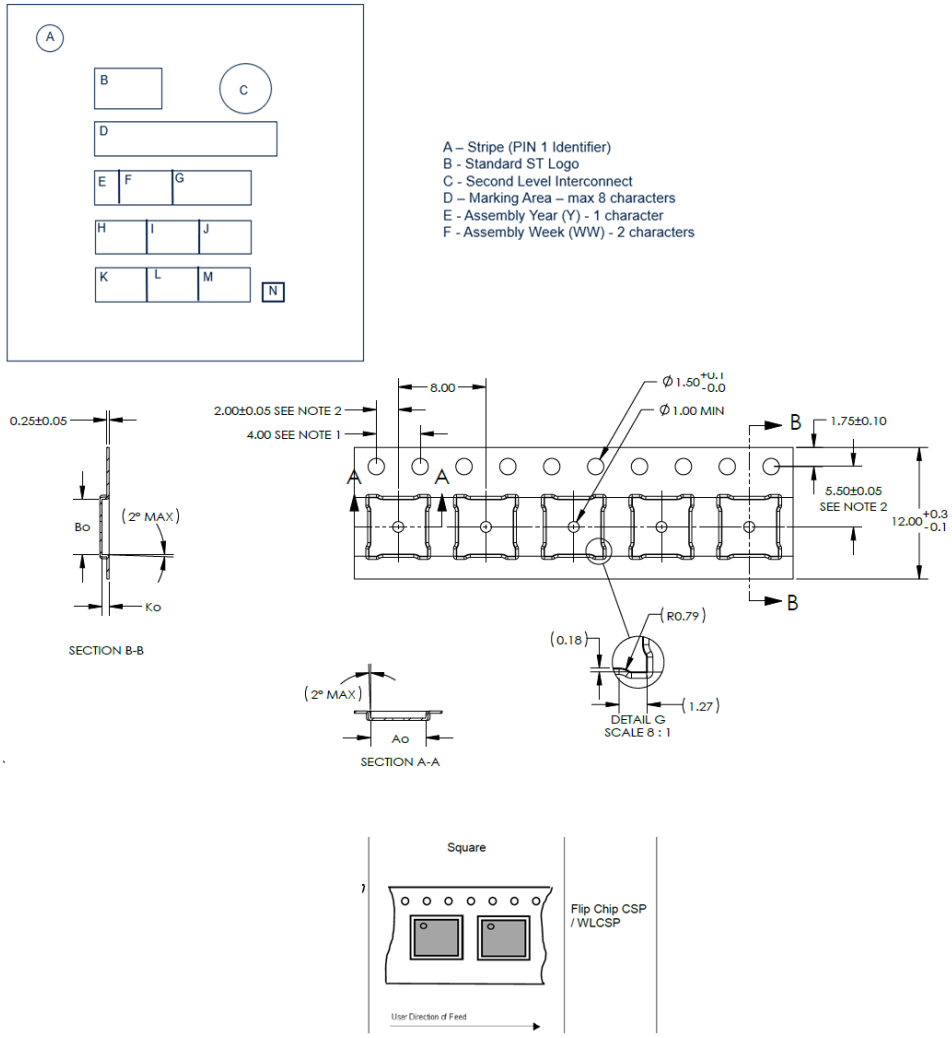
Ref	Data range (mm)		
	Min	Typ	Max
A	0.450	0.471	0.492
A1	0.181	0.196	0.211
A2	0.235	0.250	0.265
A3	0.022	0.025	0.028
b	0.243	0.268	0.293
D	4.839	4.859	4.879
D1		4.0	
E	4.839	4.859	4.879
E1		4.0	
e		0.400	
SE		0.400	
SD		0.400	
fD		0.4295	
fE		0.4295	
ccc		0.03	

Figure 11. **Recommended footprint**



RECOMMENDED FOOTPRINT

Figure 12. **Device marking , Tape and reel information**



Revision history

Table 30. **Document revision history**

Date	Version	Changes
15-June-2023	1	Initial release.

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