

TCD2711DG

The diagram illustrates the internal architecture of a CCD sensor, organized into four main horizontal sections. Each section contains a series of components connected to a common vertical bus on the left and a common vertical bus on the right.

- Top Section:** Contains "CCD analog shift register 1", "TG gate", "CCD analog shift register 2", and "Shift gate". Below these is a row of diodes labeled D26, D27, D28, ..., D125, D126, D127, S1, S2, "Photo ...diode... (B)", S7498, S7499, S7500, D128, ..., D143.
- Second Section:** Contains "CCD analog shift register 4" and "Shift gate". Below these is a row of diodes labeled D26, D27, D28, ..., D125, D126, D127, S1, S2, "Photo ...diode...", S7498, S7499, S7500, D128, ..., D143.
- Third Section:** Contains "Shift gate" and "CCD analog shift register 3". Below these is a row of diodes labeled D26, D27, D28, ..., D125, D126, D127, S1, S2, "Photo ...diode... (R)", S7498, S7499, S7500, D128, ..., D143.
- Bottom Section:** Contains "Shift gate", "CCD analog shift register 6", "TG gate", and "CCD analog shift register 5".

On the left, a vertical bus connects to pins: OD (63), OS1 (64), OS2 (65), OD (66), OS4 (67), OS3 (68), OD (3), OS6 (1), OS5 (2), and OD (5). On the right, a vertical bus connects to pins: 39 (OD), 38 (TG), 37 (SH), and 36 (SS). At the top, a series of pins are labeled: CP (62), RS (61), $\phi 2B$ (60), SS (59), SS (57), SS (55), $\phi 1A1$ (58), $\phi 2A1$ (56), OD (51), SS (50), $\phi 2A2$ (49), $\phi 2A3$ (48), SS (47), $\phi 1A2$ (46), $\phi 1A3$ (45), SS (44), $\phi 1A4$ (43), $\phi 1A5$ (42), $\phi 2A4$ (41), and $\phi 2A5$ (40). Arrows indicate signal flow from these top pins to the internal components.

Pin Names

ピン No.	記 号	名 称	ピン No.	記 号	名 称
1	OS6	Output signal 6 (Red(Even))	35	NC	No connect
2	OS5	Output signal 5 (Red(Odd))	36	SS	Ground
3	OD	Power supply	37	SH	Shift gate
4	SS	Ground	38	TG	Transfer Gate
5	OD	Power supply	39	OD	Power supply
6	NC	No connect	40	ϕ 2A5	Transfer clock (phase 2) 5
7	NC	No connect	41	ϕ 2A4	Transfer clock (phase 2) 4
8	NC	No connect	42	ϕ 1A5	Transfer clock (phase 1) 5
9	NC	No connect	43	ϕ 1A4	Transfer clock (phase 1) 4
10	NC	No connect	44	SS	Ground
11	NC	No connect	45	ϕ 1A3	Transfer clock (phase 1) 3
12	NC	No connect	46	ϕ 1A2	Transfer clock (phase 1) 2
13	NC	No connect	47	SS	Ground
14	NC	No connect	48	ϕ 2A3	Transfer clock (phase 2) 3
15	NC	No connect	49	ϕ 2A2	Transfer clock (phase 2) 2
16	NC	No connect	50	SS	Ground
17	NC	No connect	51	OD	Power supply
18	NC	No connect	52	NC	No connect
19	NC	No connect	53	NC	No connect
20	NC	No connect	54	NC	No connect
21	NC	No connect	55	SS	Ground
22	NC	No connect	56	ϕ 2A1	Transfer clock (phase 2)1
23	NC	No connect	57	SS	Ground
24	NC	No connect	58	ϕ 1A1	Transfer clock (phase 1)1
25	NC	No connect	59	SS	Ground
26	NC	No connect	60	ϕ 2B	Last stage clock (phase 2)
27	NC	No connect	61	RS	Reset gate
28	NC	No connect	62	CP	Clamp gate
29	NC	No connect	63	OD	Power supply
30	NC	No connect	64	OS1	Output signal 1 (Blue(Odd))
31	NC	No connect	65	OS2	Output signal 2 (Blue(Even))
32	NC	No connect	66	OD	Power supply
33	NC	No connect	67	OS4	Output signal 4 (Green(Even))
34	NC	No connect	68	OS3	Output signal 3 (Green(Odd))

Optical/Electrical Characteristics

(Ta = 25°C, V_{OD} = 10 V, V_φ = V_{RS} = V_{SH} = V_{CP} = 5 V (pulse), f_φ = 1.0 MHz, load resistance = 100 kΩ, t_{INT} (integration time) = 10 ms, light source = light source A + CM500S (t = 1.0 mm))

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R (R)	13.2	18.9	24.6	V/(lx·s)	(Note 2)
	Green	R (G)	14.2	20.4	26.6		
	Blue	R (B)	9.3	13.4	17.5		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage		V _{SAT}	1.2	1.5	—	V	(Note 5)
Saturation exposure		SE	0.04	0.07	—	lx·s	(Note 6)
Dark signal voltage		V _{DRK}	—	3	6	mV	(Note 7)
Dark signal non uniformity		DSNU	—	8	12	mV	(Note 8)
DC power dissipation		P _D	—	590	900	mW	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z _O	—	0.2	0.5	kΩ	—
DC signal output voltage		V _{OS}	3.5	5.0	6.5	V	(Note 9)
Random noise		N _{Dσ}	—	0.9	—	mV	(Note 10)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature, and the incident light is 50% of SH (typ.).

$$\text{PRNU (1)} = \frac{\Delta X}{\bar{X}} \times 100 (\%)$$

$\bar{X}$: Average of total signal outputs
 ΔX : The maximum deviation from $\bar{X}$.

Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (typ.).

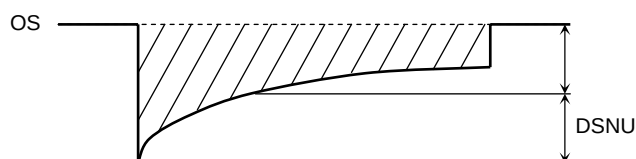
Note 5: V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

Note 6: Definition of SE:

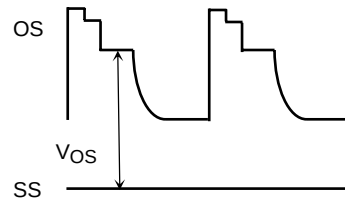
$$\text{SE} = \frac{V_{\text{SAT}}}{R_G}$$

Note 7: V_{DRK} is defined as average dark signal voltage of all effective pixels.

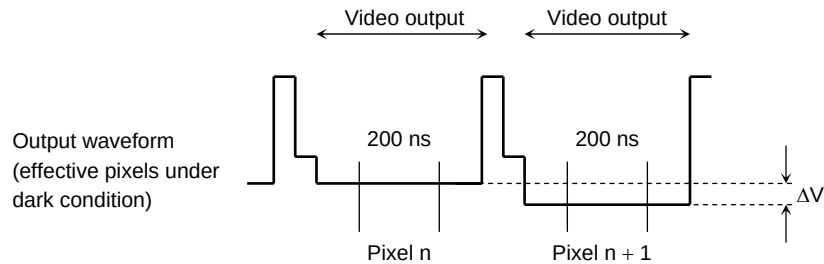
Note 8: DSNU is defined by the difference between average value (V_{DRK}) and the maximum value of the dark voltage.



Note 9: DC signal output voltage is defined as follows:



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



- (1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
- (2) Each of the output levels at video output periods averaged over 200 nanosecond period to get V_n and V_{n+1} .
- (3) V_{n+1} is subtracted from V_n to get ΔV .

$$\Delta V = V(n) - V(n+1)$$
- (4) The standard deviation of ΔV is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i| \quad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

- (5) Procedure (2), (3) and (4) are repeated 10 times to get 10 sigma values.

$$\bar{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

- (6) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$ND_{\sigma} = \frac{1}{\sqrt{2}} \bar{\sigma}$$

Operating Condition (Ta = 25°C)

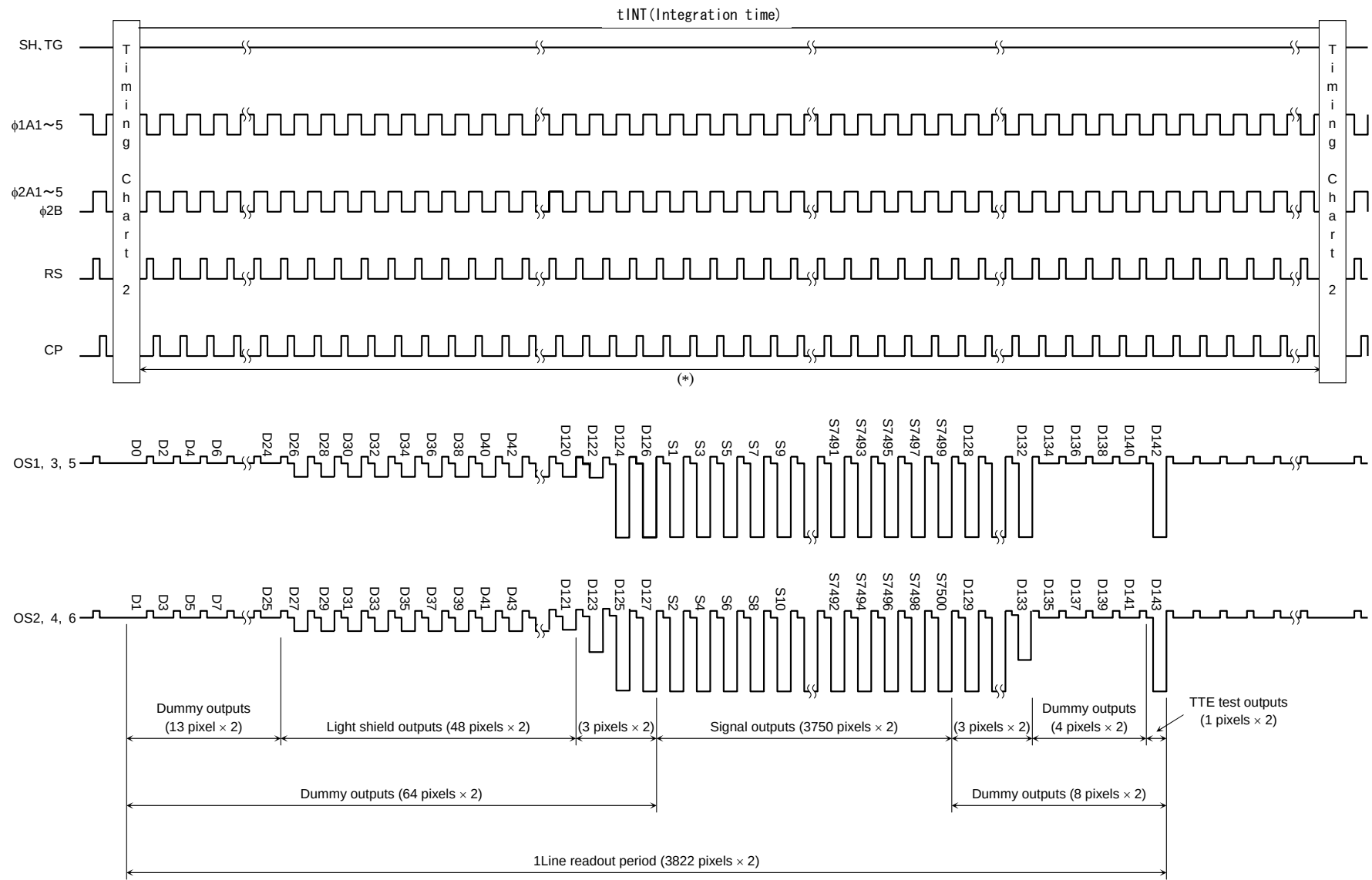
Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	High level	$V_{\phi 1A}, V_{\phi 2A}$	4.75	5.0	5.5	V
	Low level		0	—	0.25	
Last stage clock pulse voltage	High level	$V_{\phi 2B}$	4.75	5.0	5.5	V
	Low level		0	—	0.25	
Shift pulse voltage	High level	V_{SH}	4.75	5.0	5.5	V
	Low level		0	—	0.25	
Reset pulse voltage	High level	V_{RS}	4.75	5.0	5.5	V
	Low level		0	—	0.25	
Clamp pulse voltage	High level	V_{CP}	4.75	5.0	5.5	V
	Low level		0	—	0.25	
TG pulse voltage	High level	V_{TG}	4.75	5.0	5.5	V
	Low level		0	—	0.25	
Power supply voltage		V_{OD}	9.5	10.0	10.5	V

Clock Characteristics (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	0.2	1	35	MHz
Reset pulse frequency	f_{RS}	0.2	1	35	MHz
Clamp pulse frequency	f_{CP}	0.2	1	35	MHz
Clock capacitance (Note 12)	$C_{\phi 1A}$	—	153	—	pF
	$C_{\phi 2A}$	—	162	—	
Last stage clock capacitance	$C_{\phi B}$	—	3	—	pF
Shift gate capacitance	C_{SH}	—	32	—	pF
Reset gate capacitance	C_{RS}	—	5	—	pF
Clamp gate capacitance	C_{CP}	—	3	—	pF
TG gate capacitance	C_{TG}	—	5	—	pF

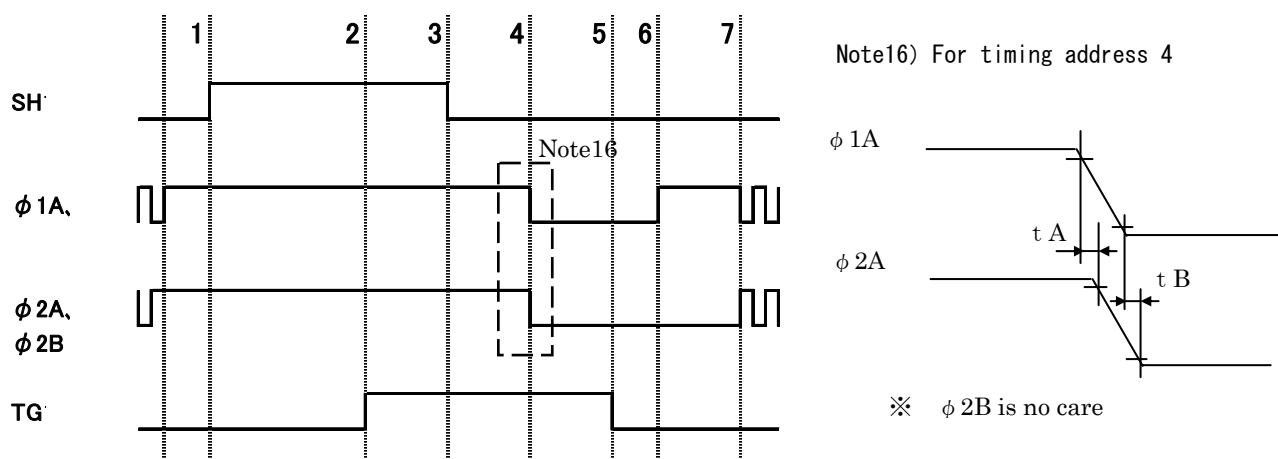
Note12: $V_{OD} = 10\text{ V}$

Timing Chart 1



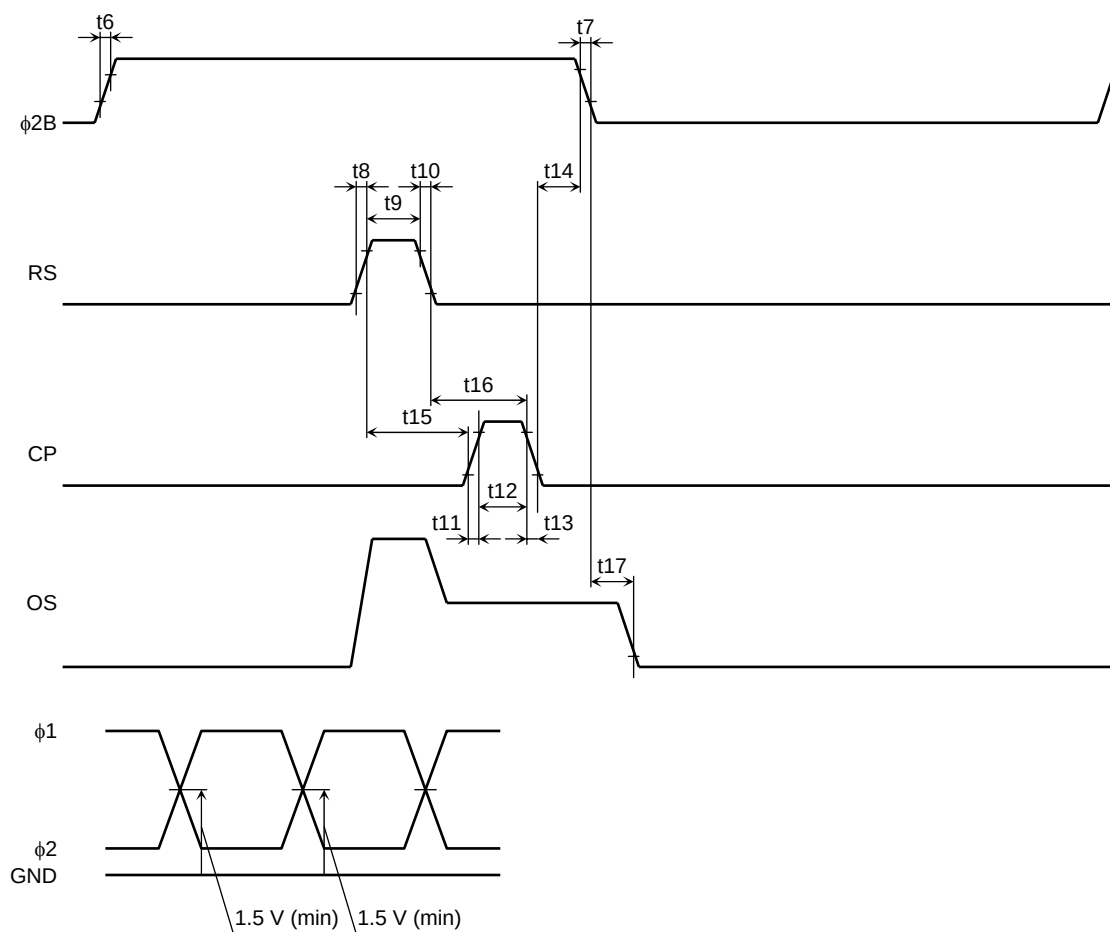
* Hold the SH and TG pins at Low level during this period.

Timing Chart 2(Vertical transfer period)



Note 13: Each RS and CP pins put to Low level during of the above mentioned address 1-7

Timing Requirements 1



Characteristics	Symbol	Min	Typ. (Note 14)	Max	Unit
$\phi 1$, $\phi 2$ Pulse rise time, fall time	t6, t7	0	50	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	6	100	—	ns
CP pulse rise time, fall time	t11, t13	0	20	—	ns
CP pulse width	t12	6	200	—	ns
Pulse timing of $\phi 2B$ and CP	t14	0	40	—	ns
Pulse timing of RS and CP	t15	0	0	—	ns
	t16	6	100	—	
Video data delay time (Note 15)	t17	—	7	—	ns

Note 14: Measured with $f_{RS} = 1$ MHz.

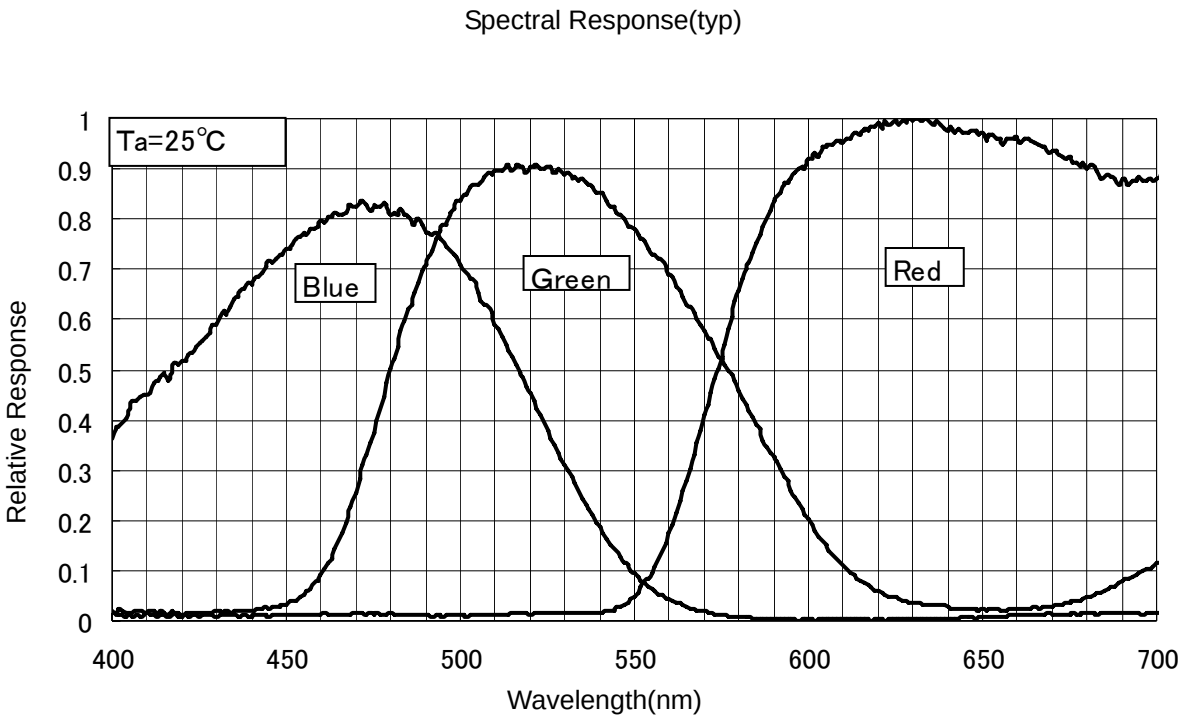
Note 15: Load resistance is 100 k Ω .

Timing Requirements 2 (Vertical transfer period)

Timing Address	Min	Typ.	Max	Unit
1	250	500	—	ns
2	1000	2000	—	ns
3	500	1000	—	ns
4	500	1000	—	ns
5	500	1000	—	ns
6	250	500	—	ns
7	500	1000	—	ns
Vertical Transfer Time	3. 5	7	—	μ s

Timing Address 4		Min	Typ.	Max	Unit
$\phi 1A$, $\phi 2A$	tA	—0. 5	0	0. 5	ns
	tB	—0. 5	0	0. 5	ns

Typical Spectral Response



Cautions**1. Electrostatic Breakdown**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting pliers or pincer.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Mounting on a PCB

This package is sensitive to mechanical stress.

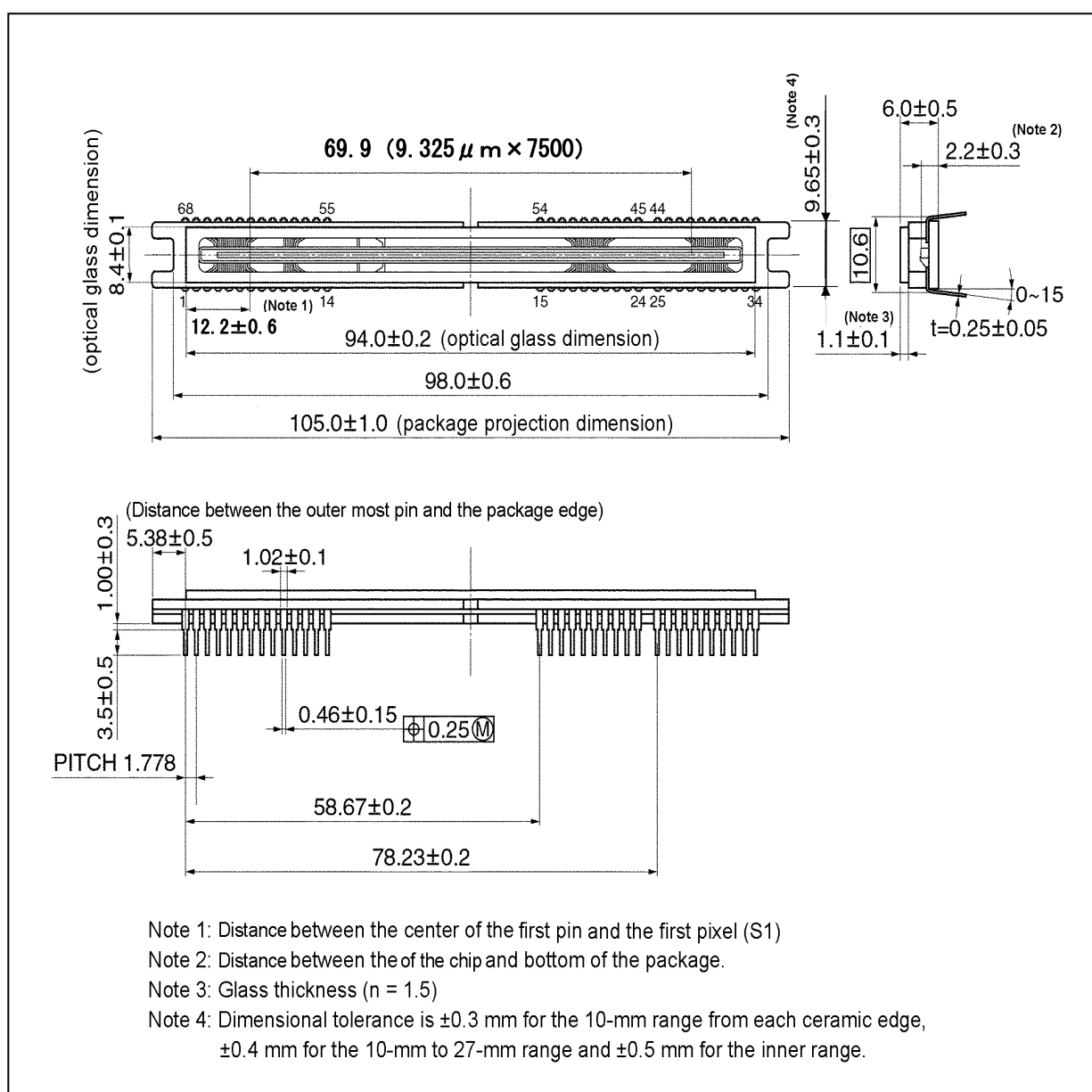
Toshiba recommends using IC inserters for mounting, instead of using lead forming equipment.

5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.

Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

Package Dimensions



Weight: 16.0 g (typ.)

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before creating and producing designs and using, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application that Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- Product is intended for use in general electronics applications (e.g., computers, personal equipment, office equipment, measuring equipment, industrial robots and home electronics appliances) or for specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact ("Unintended Use"). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for Unintended Use unless specifically permitted in this document.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Product is subject to foreign exchange and foreign trade control laws.
- The technical information described in this document is subject to foreign exchange and foreign trade control laws.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. TOSHIBA assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.

History

Rev.	Date	History
0	2009-06-30	Newly
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		