2.5-V PHASE-LOCKED-LOOP CLOCK DRIVER

FEATURES

- **Spread-Spectrum Clock Compatible**
- **Operating Frequency: 60 MHz to 220 MHz**
- **Low Jitter (Cycle-Cycle): ±60 ps (±40 ps at 200 MHz)**
- **Low Static Phase Offset: ±50 ps**
- **Low Jitter (Period): ±60 ps (±30 ps at 200 MHz)**
- **1-to-4 Differential Clock Distribution (SSTL2)**
- **Best in Class for $V_{OX} = V_{DD}/2 \pm 0.1$ V**
- **Operates From Dual 2.6-V or 2.5-V Supplies**
- **Available in a 28-Pin TSSOP Package**
- **Consumes < 100-µA Quiescent Current**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**
- **Meets/Exceeds JEDEC Standard (JESD82-1) For DDRI-200/266/333 Specification**
- **Meets/Exceeds Proposed DDRI-400 Specification (JESD82-1A)**
- **Enters Low-Power Mode When No CLK Input Signal Is Applied or $\overline{\text{PWRDWN}}$ Is Low**

APPLICATIONS

- **DDR Memory Modules (DDR400/333/266/200)**
- **Zero-Delay Fan-Out Buffer**

DESCRIPTION

The CDCVF855 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to 4 differential pairs of clock outputs (Y[0:3], $\overline{\text{Y[0:3]}}$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency-detection circuit detects the low-frequency condition and, after applying a >20-MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF855 is also able to track spread-spectrum clocking for reduced EMI.

Because the CDCVF855 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF855 is characterized for both commercial and industrial temperature ranges.

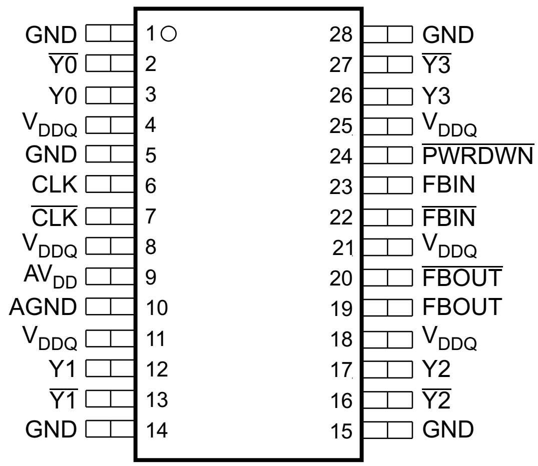
AVAILABLE OPTIONS

T_A	TSSOP (PW)
–40°C to 85°C	CDCVF855PW

FUNCTION TABLE
(Select Functions)

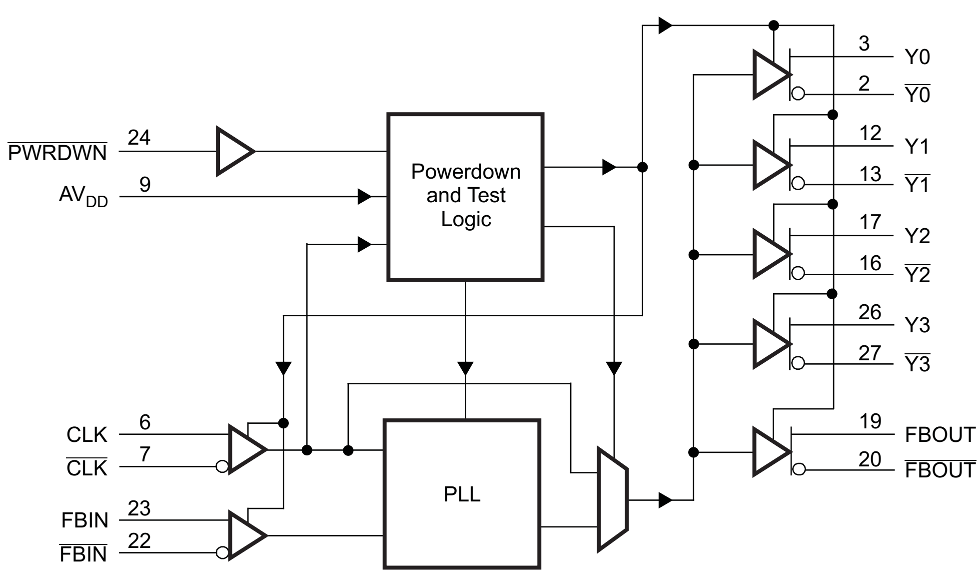
INPUTS				OUTPUTS				PLL
AVDD	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y[0:3]	$\overline{Y[0:3]}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

PW PACKAGE
(TOP VIEW)



P0043-02

FUNCTIONAL BLOCK DIAGRAM



B0196-02

Table 2. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	10	–	Ground for 2.5-V analog supply
AV_{DD}	9	–	2.5-V analog supply
CLK, $\overline{CLK}$	6, 7	I	Differential clock input
$\overline{FBIN}$, FBIN	22, 23	I	Feedback differential clock input
FBOUT, $\overline{FBOUT}$	19, 20	O	Feedback differential clock output
GND	1, 5, 14, 15, 28	–	Ground
$\overline{PWRDWN}$	24	I	Output enable for Y and $\overline{Y}$
V_{DDQ}	4, 8, 11, 18, 21, 25	–	2.5-V supply
$\overline{Y0}$, Y0	2, 3	O	Buffered output copies of input clock, CLK, $\overline{CLK}$
Y1, $\overline{Y1}$	12, 13	O	Buffered output copies of input clock, CLK, $\overline{CLK}$
$\overline{Y2}$, Y2	16, 17	O	Buffered output copies of input clock, CLK, $\overline{CLK}$
Y3, $\overline{Y3}$	26, 27	O	Buffered output copies of input clock, CLK, $\overline{CLK}$

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

V_{DDQ}, AV_{DD}	Supply voltage range		0.5 V to 3.6 V
V_I	Input voltage range (2) (3)		–0.5 V to V_{DDQ} + 0.5 V
V_O	Output voltage range (2) (3)		–0.5 V to V_{DDQ} + 0.5 V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DDQ}$	±50 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DDQ}$	±50 mA
I_O	Continuous output current	V_O = 0 to V_{DDQ}	±50 mA
I_{DDS}	Continuous current to GND or V_{DDQ}		±100 mA
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
(3) This value is limited to 3.6 V maximum.

THERMAL CHARACTERISTICS

$R_{\theta JA}$ for TSSOP Package (1)	
Airflow	**High K**
0 ft/min (0 m/min)	94.4°C/W
150 ft/min (45.72 m/min)	82.8°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS

					MIN	NOM	MAX	UNIT
	Supply voltage	V_{DDQ}	PC1600 – PC3200		2.3		2.7	V
		AVDD			V_{DDQ} – 0.12		2.7	
V_{IL}	Low-level input voltage	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$					V_{DDQ}/2 – 0.18	V
		$\overline{PWRDWN}$			–0.3		0.7	
V_{IH}	High-level input voltage	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$			V_{DDQ}/2 + 0.18			V
		$\overline{PWRDWN}$			1.7		V_{DDQ} + 0.3	
	DC input signal voltage (1)				–0.3		V_{DDQ} + 0.3	V
V_{ID}	Differential input signal voltage (2)	DC	CLK, FBIN	V_{DDQ} = 2.3 V – 2.7V	0.36		V_{DDQ} + 0.6	V
				V_{DDQ} = 2.425 V – 2.7 V	0.25		V_{DDQ} + 0.6	
		AC	CLK, FBIN	V_{DDQ} = 2.3 V – 2.7 V	0.7		V_{DDQ} + 0.6	
				V_{DDQ} = 2.425 V – 2.7 V	0.49		V_{DDQ} + 0.6	
V_{IX}	Input differential pair cross voltage (3) (4)				V_{DDQ}/2 – 0.2		V_{DDQ}/2 + 0.2	V
I_{OH}	High-level output current						–12	mA
I_{OL}	Low-level output current						12	mA
SR	Input slew rate				1		4	V/ns
T_A	Operating free-air temperature				–40		85	°C

(1) The unused inputs must be held high or low to prevent them from floating.
(2) The dc input signal voltage specifies the allowable dc execution of the differential input.
(3) The differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
(4) The differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must cross.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{IK}	Input voltage, all inputs	V_{DDQ} = 2.3 V, I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage	V_{DDQ} = min to max, I_{OH} = –1 mA	V_{DDQ} – 0.1			V
		V_{DDQ} = 2.3 V, I_{OH} = –12 mA	1.7			
V_{OL}	Low-level output voltage	V_{DDQ} = min to max, I_{OL} = 1 mA			0.1	V
		V_{DDQ} = 2.3 V, I_{OL} = 12 mA			0.6	
V_{OD}	Output voltage swing (2)	Differential outputs are terminated with 120 Ω, C_L = 14 pF (See Figure 3)	1.1		V_{DDQ} – 0.4	V
V_{OX}	Output differential cross-voltage (3)		V_{DDQ}/2 – 0.1	V_{DDQ}/2	V_{DDQ}/2 + 0.1	V
I_I	Input current	V_{DDQ} = 2.7 V, V_I = 0 V to 2.7 V			±10	µA
I_{OZ}	High-impedance-state output current	V_{DDQ} = 2.7 V, V_O = V_{DDQ} or GND			±10	µA
I_{DDPD}	Power-down current on V_{DDQ} + AV_{DD}	CLK and $\overline{CLK}$ = 0 MHz; $\overline{PWRDWN}$ = Low; Σ of I_{DD} and AI_{DD}		20	100	µA
AI_{DD}	Supply current on AV_{DD}	f_O = 170 MHz		6	8	mA
		f_O = 200 MHz		8	10	
C_I	Input capacitance	V_{DDQ} = 2.5 V, V_I = V_{DDQ} or GND	2	2.5	3.5	pF

(1) All typical values are at a nominal V_{DDQ}.
(2) The differential output signal voltage specifies the differential voltage |VTR – VCP|, where VTR is the true output level and VCP is the complementary output level.
(3) The differential cross-point voltage tracks variations of V_{DDQ} and is the voltage at which the differential signals must cross.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [(1)]	MAX	UNIT
I_{DD}	Dynamic current on V_{DDQ}	Without load	f_O = 170 MHz		65	80	mA
			f_O = 200 MHz		75	90	
		Differential outputs terminated with 120 Ω, C_L = 0 pF	f_O = 170 MHz		110	140	
			f_O = 200 MHz		120	150	
		Differential outputs terminated with 120 Ω, C_L = 14 pF	f_O = 170 MHz		130	160	
			f_O = 200 MHz		140	170	
ΔC	Part-to-part input capacitance variation	V_{DDQ} = 2.5 V, V_I = V_{DDQ} or GND				1	pF
$C_{I(\Delta)}$	Input capacitance difference between CLK and $\overline{CLK}$, FBIN and $\overline{FBIN}$	V_{DDQ} = 2.5 V, V_I = V_{DDQ} or GND				0.25	pF

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		MIN	MAX	UNIT
f_{CLK}	Operating clock frequency	60	220	MHz
	Application clock frequency	90	220	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time (PLL mode)[(1)]		10	µs
	Stabilization time (bypass mode)[(2)]		30	ns

(1) The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V_{DD} must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.
(2) A recovery time is required when the device goes from power-down mode into bypass mode (AV_{DD} at GND).

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} (1)	Low- to high-level propagation delay time	Test mode/CLK to any output		3.5		ns
t_{PHL} (1)	High- to low-level propagation delay time	Test mode/CLK to any output		3.5		ns
$t_{jit(per)}$ (2)	Jitter (period), see Figure 7	100/133/167 MHz (PC1600/2100/2700)	–65		65	ps
		200 MHz (PC3200)	–30		30	
$t_{jit(cc)}$ (2)	Jitter (cycle-to-cycle), see Figure 4	100/133/167 MHz (PC1600/2100/2700)	–60		60	ps
		200 MHz (PC3200)	–40		40	
$t_{jit(hper)}$ (2)	Half-period jitter, see Figure 8	100/133/167 MHz (PC1600/2100/2700)	–100		100	ps
		200 MHz (PC3200)	–75		75	
$t_{slr(o)}$	Output clock slew rate, see Figure 9	Load: 120 Ω, 14 pF	1		2	V/ns
$t_{(\phi)}$	Static phase offset, see Figure 5	100/133/167/200 MHz	–50		50	ps
$t_{sk(o)}$	Output skew, see Figure 6	Load: 120 Ω, 14 pF; 100/133/167/200 MHz			40	ps

(1) Refers to the transition of the noninverting output.
(2) This parameter is assured by design but cannot be 100% production tested.

PARAMETER MEASUREMENT INFORMATION

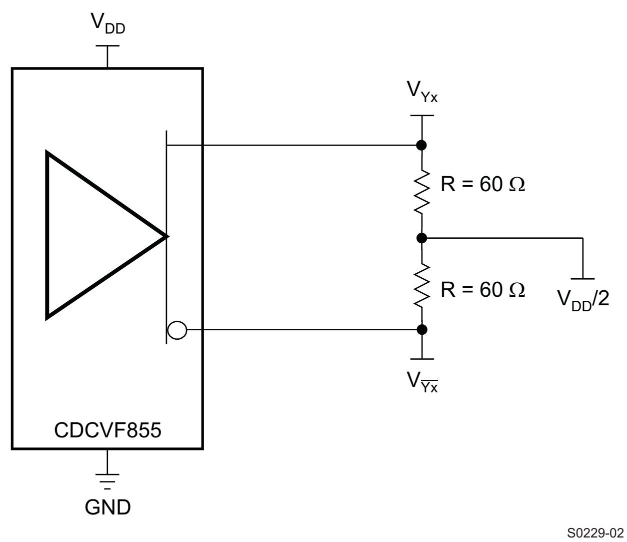


Figure 1. IBIS Model Output Load

PARAMETER MEASUREMENT INFORMATION (continued)

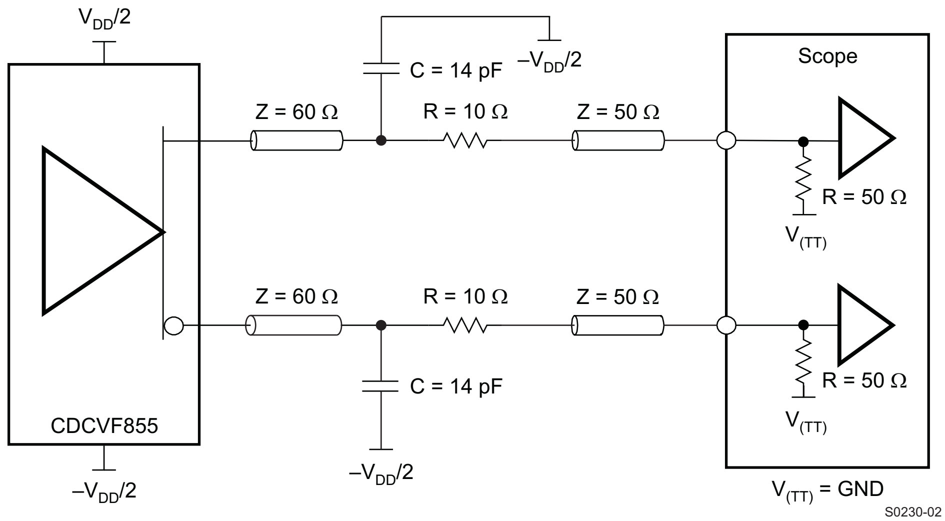


Figure 2. Output Load Test Circuit

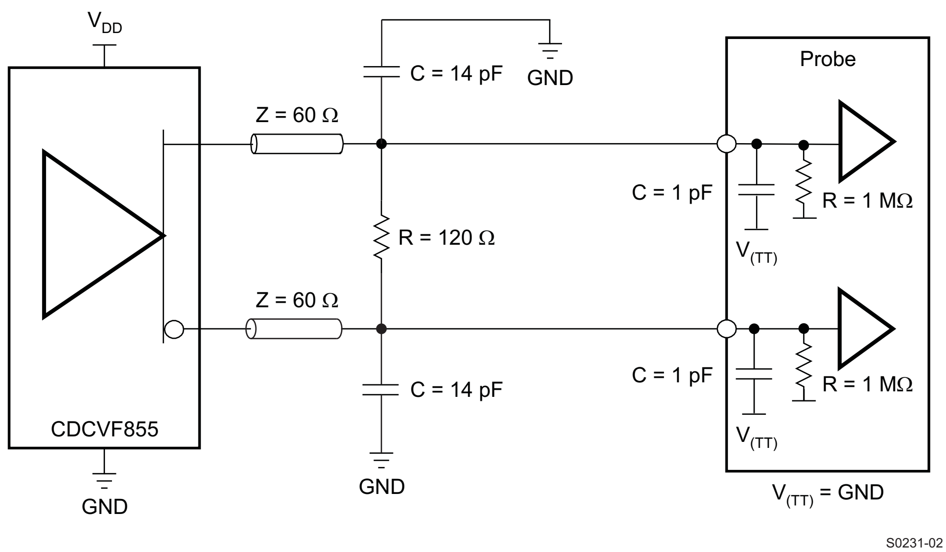


Figure 3. Output Load Test Circuit for Crossing Point

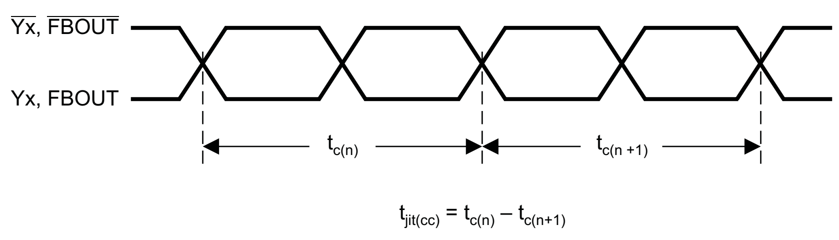


Figure 4. Cycle-to-Cycle Jitter

TEXAS INSTRUMENTS
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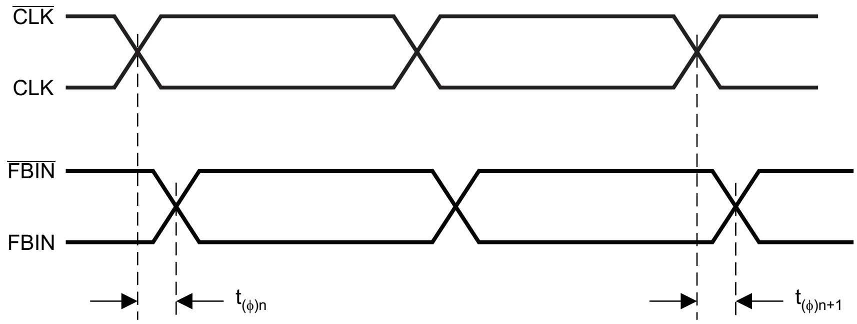
PARAMETER MEASUREMENT INFORMATION (continued)

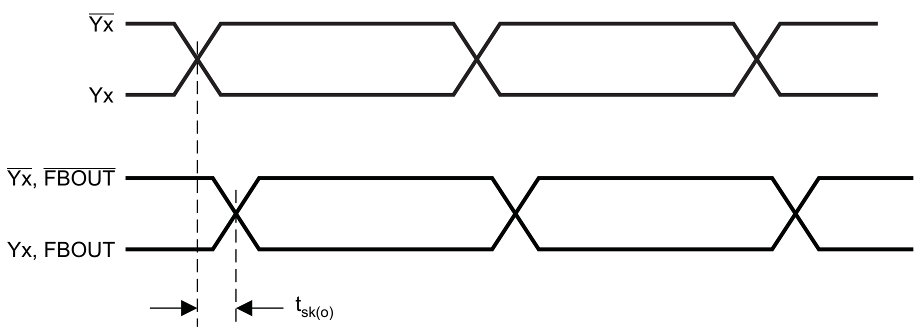


$$t_{(\phi)} = \frac{\sum_{1}^{n=N} t_{(\phi)n}}{N}$$

(N > 1000 Samples)

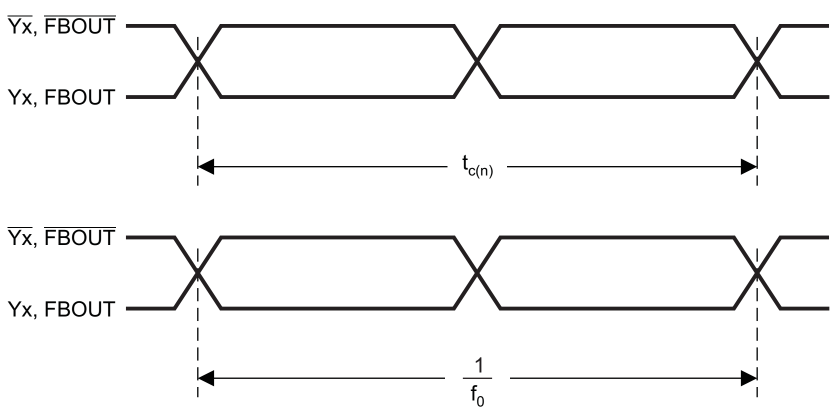
T0175-01

Figure 5. Phase Offset



T0176-01

Figure 6. Output Skew

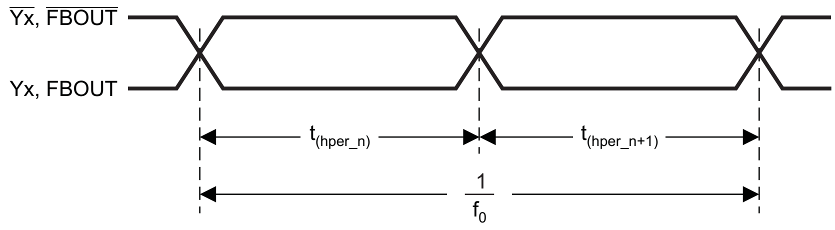


$t_{jit(per)} = t_{c(n)} - \frac{1}{f_0}$ f_0 = Average Input Frequency Measured at CLK/$\overline{CLK}$

T0177-01

Figure 7. Period Jitter

PARAMETER MEASUREMENT INFORMATION (continued)



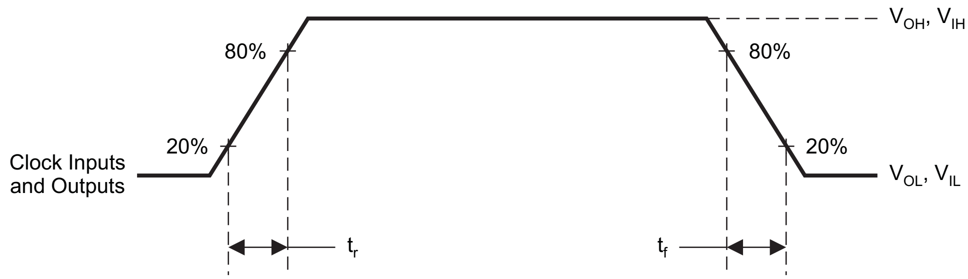
$$t_{jit(hper)} = t_{(hper\_n)} - \frac{1}{2 \times f_0}$$

n = Any Half Cycle

f_0 = Average Input Frequency Measured at CLK/$\overline{CLK}$

T0178-01

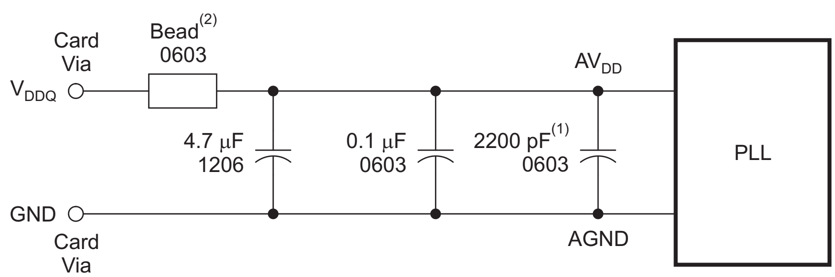
Figure 8. Half-Period Jitter



$$t_{slr(I/O)} = \frac{V_{80\%} - V_{20\%}}{t_r} \qquad t_{slf(I/O)} = \frac{V_{80\%} - V_{20\%}}{t_f}$$

T0179-01

Figure 9. Input and Output Slew Rates



S0232-01

(1) Place the 2200-pF capacitor close to the PLL.

(2) Recommended bead: Fair-Rite P/N 2506036017Y0 or equilvalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

NOTE: Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).

Figure 10. Recommended AV_{DD} Filtering

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF855PW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF855	Samples
CDCVF855PWG4	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF855	Samples
CDCVF855PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCVF855	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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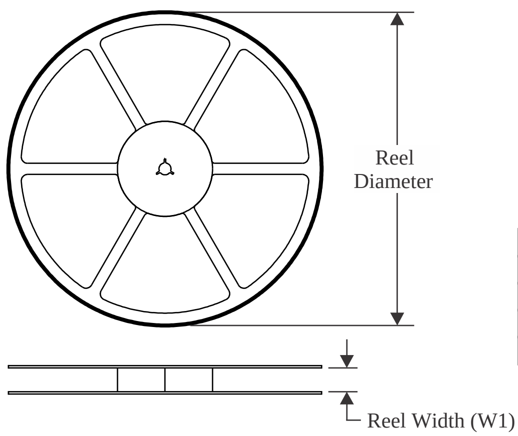
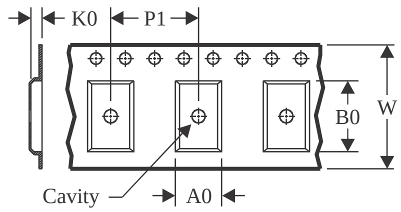
TAPE AND REEL INFORMATION

REEL DIMENSIONS

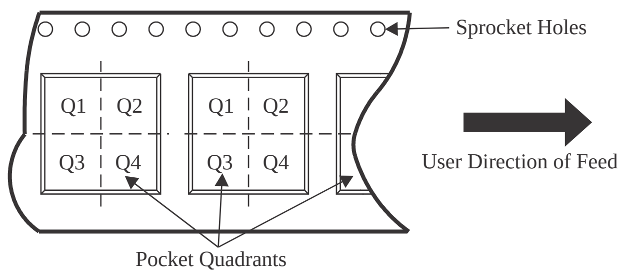


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

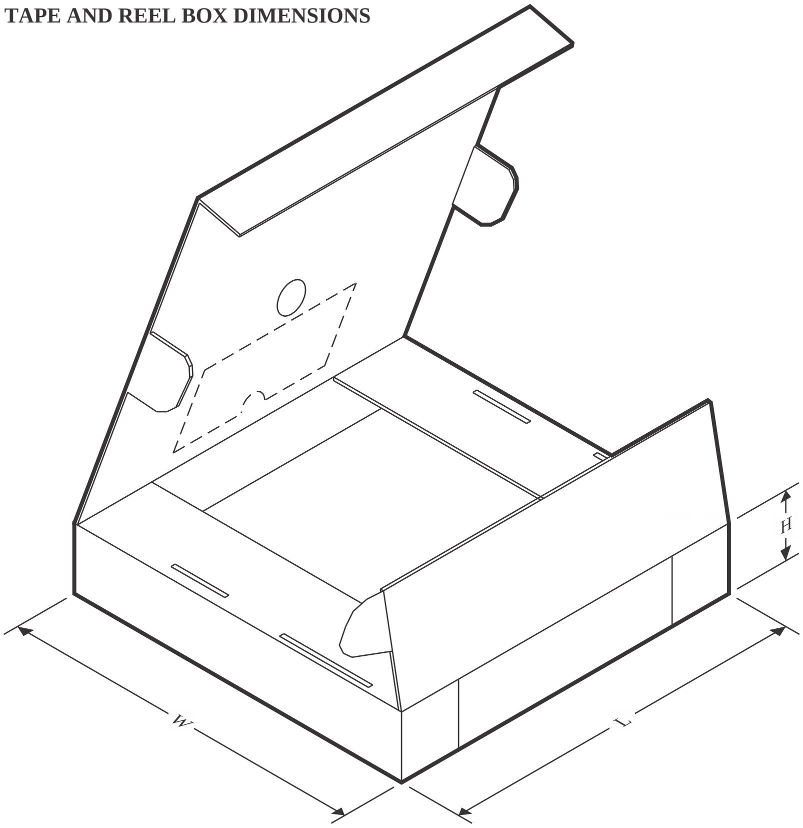
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF855PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

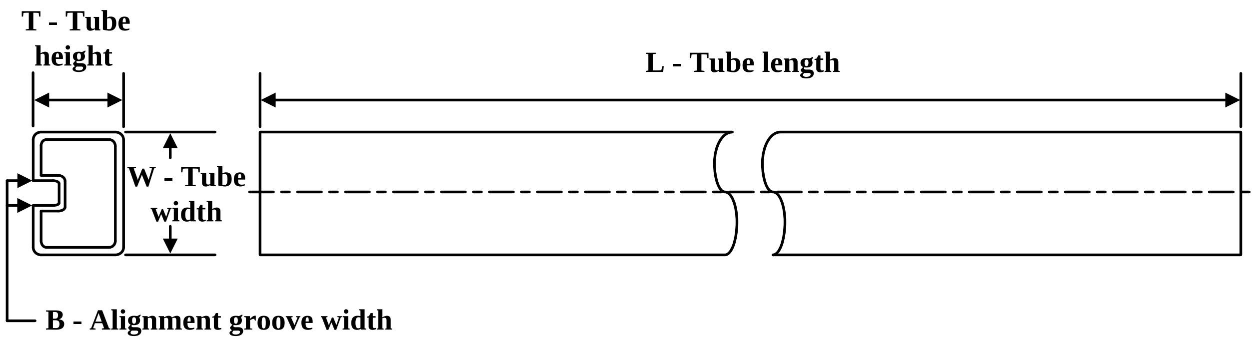
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF855PWR	TSSOP	PW	28	2000	356.0	356.0	35.0

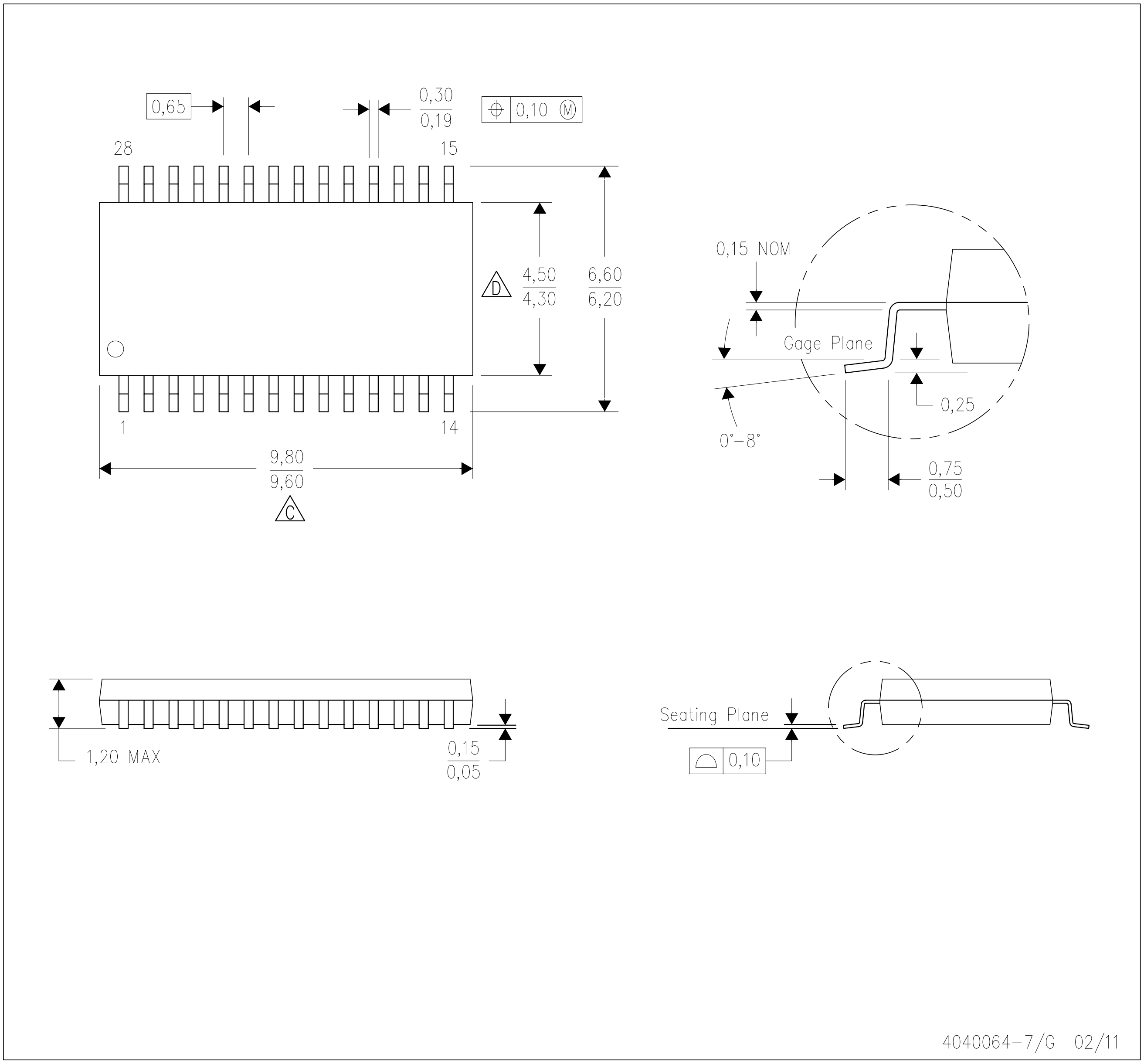
TUBE



*All dimensions are nominal

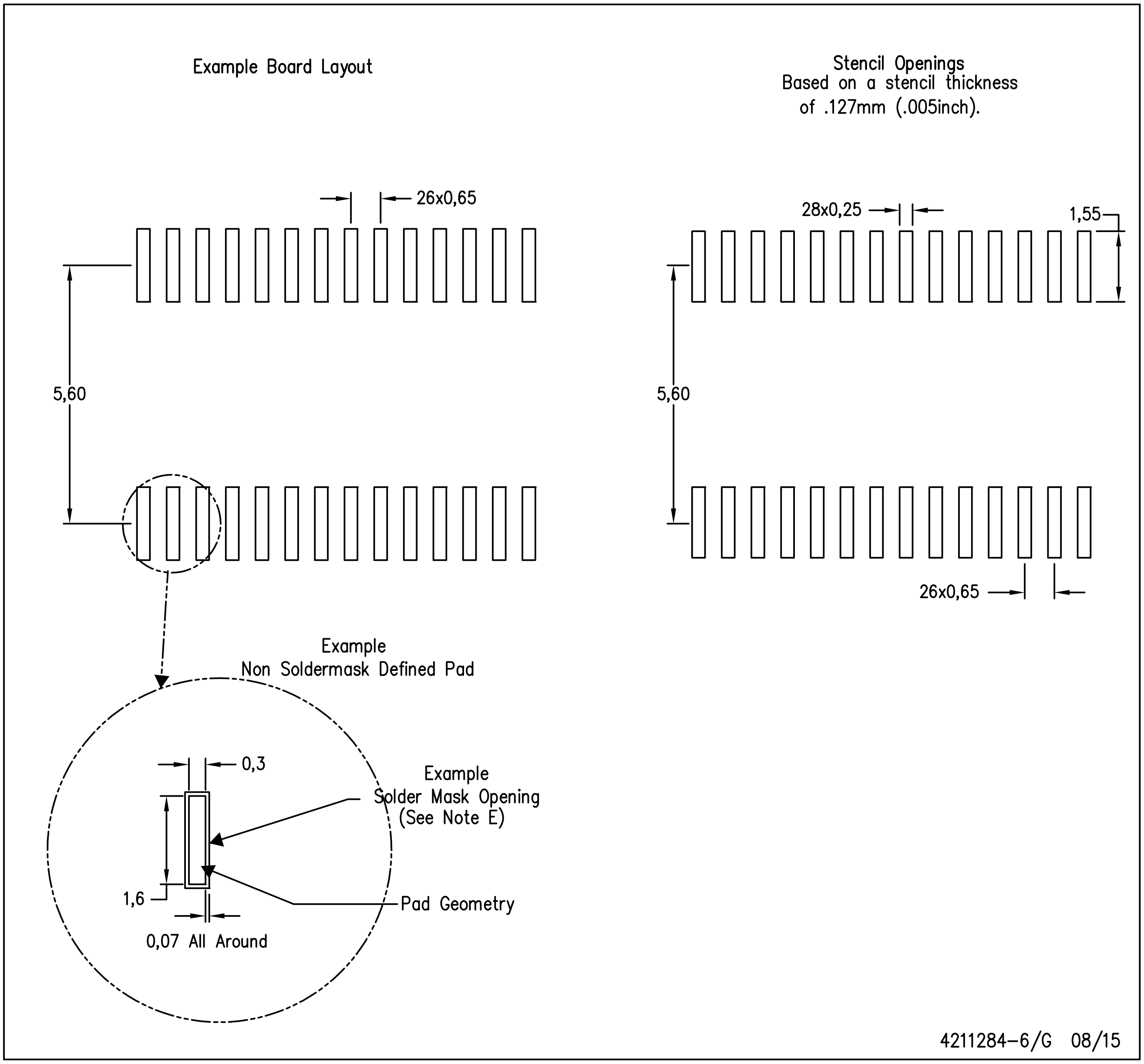
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDCVF855PW	PW	TSSOP	28	50	530	10.2	3600	3.5
CDCVF855PWG4	PW	TSSOP	28	50	530	10.2	3600	3.5

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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