S-19110JxxA to S-19110RxxA Series

AUTOMOTIVE, 125°C OPERATION, 36 V, SENSE-INPUT VOLTAGE DETECTOR WITH DELAY FUNCTION (EXTERNAL DELAY TIME SETTING)

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The S-19110 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage and release voltage are fixed internally with an accuracy of ±2.5%. It operates with current consumption of 600 nA typ.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared in the SENSE detection product, so the output is stable even if the SENSE pin falls to 0 V.
The detection signal and release signal can be delayed by setting a capacitor externally, and the detection delay time accuracy is ±20% (C_N = 3.3 nF, Ta = –40°C to +125°C), the release delay time accuracy is ±20% (C_P = 3.3 nF, Ta = –40°C to +125°C).
The output form is Nch open-drain output.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Detection voltage: J / K / L / M type (VDD detection product): 3.6 V to 4.95 V (0.05 V step)
  N / P / Q / R type (SENSE detection product): 3.0 V to 4.95 V (0.05 V step)
- Detection voltage accuracy: ±3.0% ($-V_{DET(S)}$ = 3.0 V to 4.15 V, Ta = –40°C to +125°C)
  ±2.5% ($-V_{DET(S)}$ = 4.2 V to 4.95 V, Ta = –40°C to +125°C)
- Detection delay time accuracy: ±20% (C_N = 3.3 nF, Ta = –40°C to +125°C)
- Release voltage: J / K / L / M type (VDD detection product): 3.8 V to 6.4 V (0.05 V step)
  N / P / Q / R type (SENSE detection product): 3.15 V to 6.4 V (0.05 V step)
- Release voltage accuracy: ±3.0% ($-V_{DET(S)}$ = 3.0 V to 4.15 V, Ta = –40°C to +125°C, 5.0% ≤ V_{HYS} ≤ 20.0%)
  ±3.5% ($-V_{DET(S)}$ = 3.0 V to 4.15 V, Ta = –40°C to +125°C, 20.0% < V_{HYS} ≤ 30.0%)
  ±2.5% ($-V_{DET(S)}$ = 4.2 V to 4.95 V. Ta = –40°C to +125°C, 5.0% ≤ V_{HYS} ≤ 20.0%)
  ±3.0% ($-V_{DET(S)}$ = 4.2 V to 4.95 V, Ta = –40°C to +125°C, 20.0% < V_{HYS} ≤ 30.0%)
- Release delay time accuracy: ±20% (C_P = 3.3 nF, Ta = –40°C to +125°C)
- Current consumption: 600 nA typ.
- Operation voltage range: 1.8 V to 36.0 V
- Hysteresis width*1: "Available" / "unavailable" is selectable.
  5.0% to 30.0% (Ta = –40°C to +125°C)
- Output form: Nch open-drain output
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*2

***1.** When "available" is selected, the hysteresis width can be set in the range of 5.0% to 30.0%.
***2.** Contact our sales representatives for details.

■ Applications

- Power supply monitor for microcomputer and reset for CPU
- Automotive battery voltage detection
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

■ Package

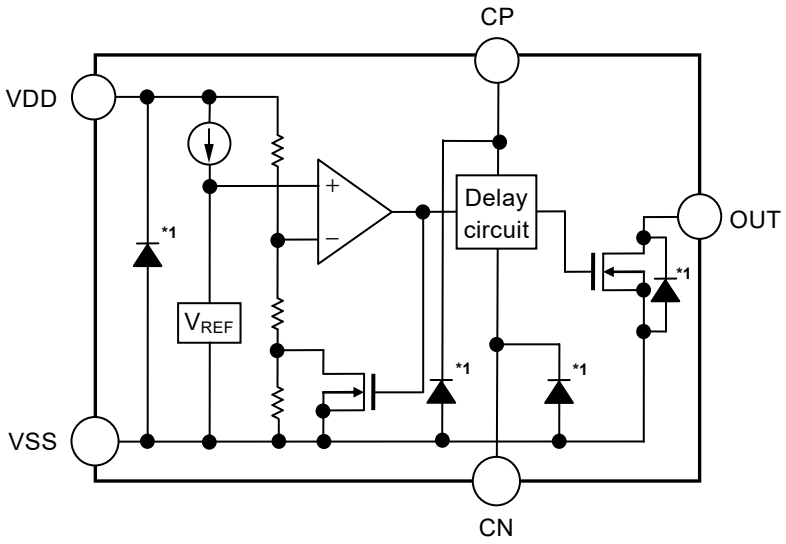
- SOT-23-6

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■ Block Diagrams

1. S-19110 Series J / K type (VDD detection product)

Function	Status
Voltage detection	VDD detection
Hysteresis width	Available

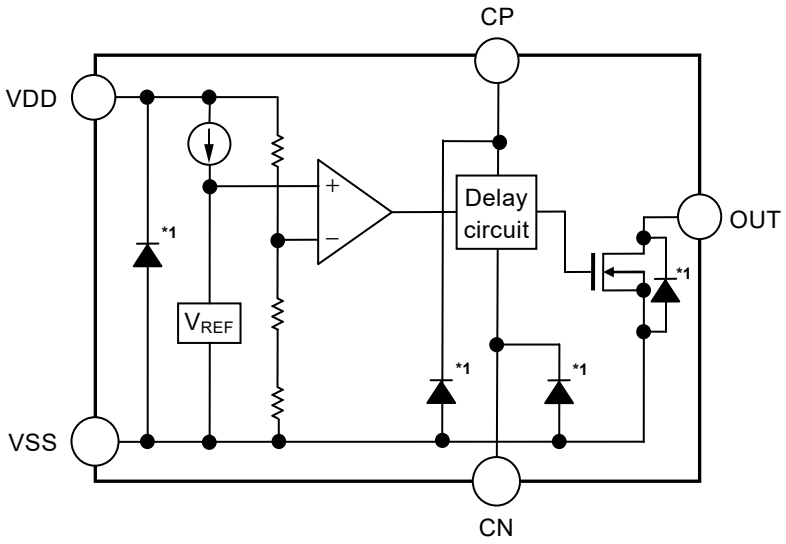


***1.** Parasitic diode

Figure 1

2. S-19110 Series L / M type (VDD detection product)

Function	Status
Voltage detection	VDD detection
Hysteresis width	Unavailable

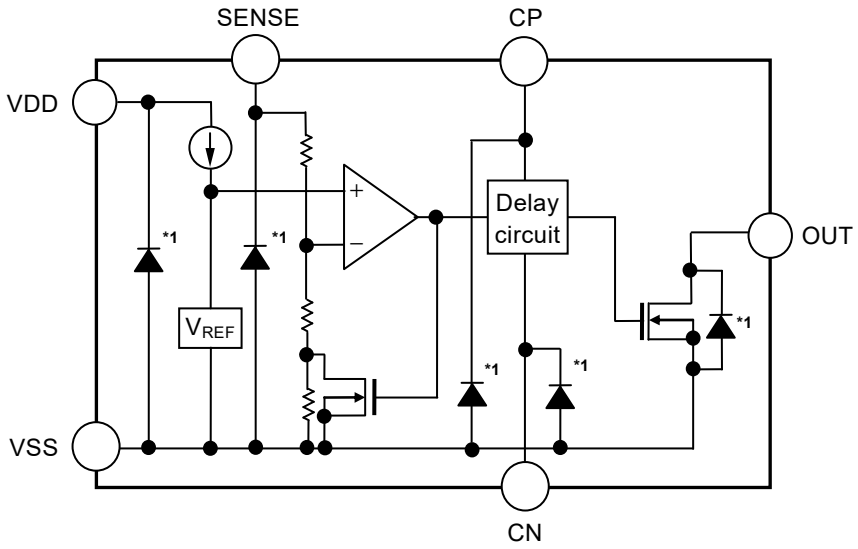


***1.** Parasitic diode

Figure 2

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3. S-19110 Series N / P type (SENSE detection product)

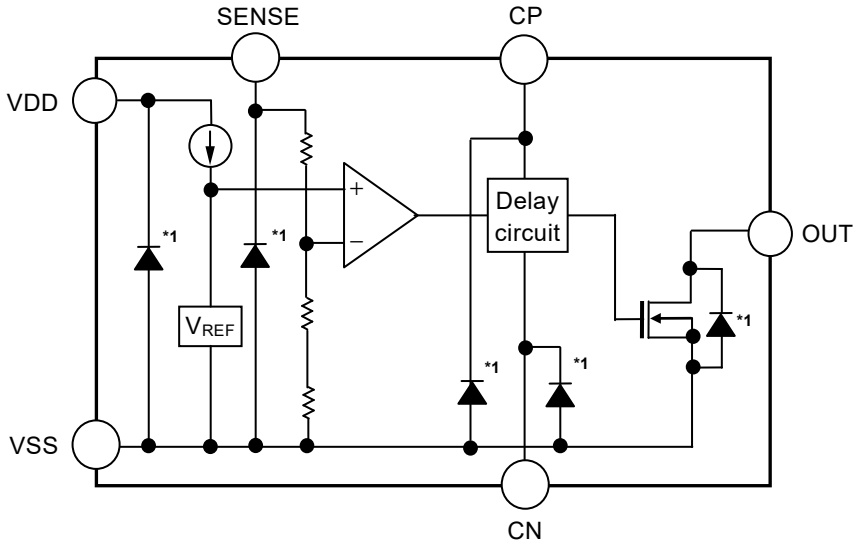


Function	Status
Voltage detection	SENSE detection
Hysteresis width	Available

*1. Parasitic diode

Figure 3

4. S-19110 Series Q / R type (SENSE detection product)



Function	Status
Voltage detection	SENSE detection
Hysteresis width	Unavailable

*1. Parasitic diode

Figure 4

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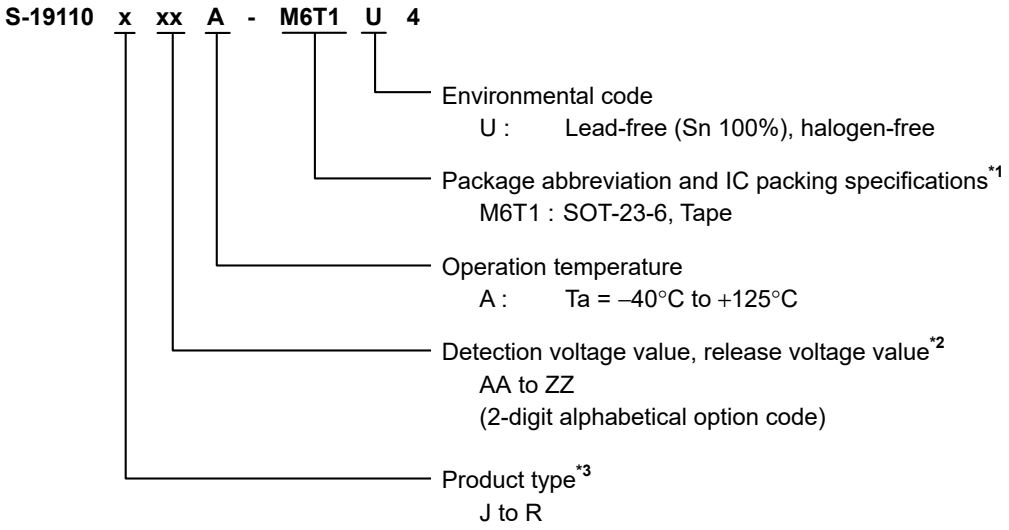
■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the product type, detection voltage value and release voltage value for the S-19110 Series.
Refer to "**1. Product name**" regarding the contents of product name, "**2. Function list of product types**" regarding the product types and "**3. Package**" regarding the package drawings.

1. Product name



***1.** Refer to the tape drawing.
***2.** Contact our sales representatives for details on combination of detection voltage value and release voltage value.
***3.** Refer to "**2. Function list of product types**".

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Remark The difference (hysteresis width) of detection voltage ($-V_{DET}$) and release voltage ($+V_{DET}$) can be set in the range of 5.0% to 30.0%. The detection voltage and release voltage combination can be selected from the A area shown in **Figure 5**.

Example: If $-V_{DET}$ = 3.0 V, the release voltage can be set in the range of 3.15 V to 3.9 V in 50 mV step.

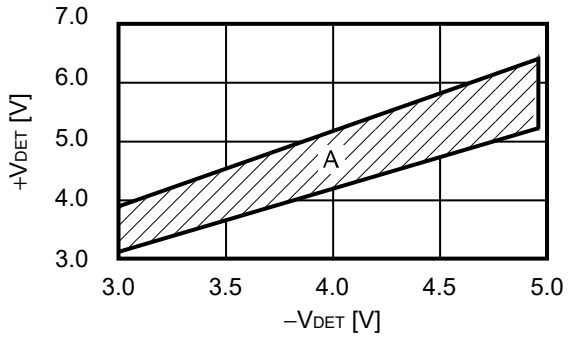


Figure 5 Detection Voltage and Release Voltage Possible Setting Area

2. Function list of product types

Table 1

Product Type	Voltage Detection	Output Logic	Hysteresis Width
J	VDD detection	Active "L"	Available
K	VDD detection	Active "H"	Available
L	VDD detection	Active "L"	Unavailable
M	VDD detection	Active "H"	Unavailable
N	SENSE detection	Active "L"	Available
P	SENSE detection	Active "H"	Available
Q	SENSE detection	Active "L"	Unavailable
R	SENSE detection	Active "H"	Unavailable

3. Package

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD

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■ Pin Configurations

1. S-19110 Series J / K / L / M type (VDD detection product)

1. 1 SOT-23-6

Top view

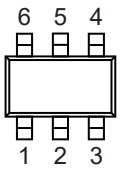


Figure 6

Table 3

Pin No.	Symbol	Description
1	VDD	Voltage input pin
2	NC*1	No connection
3	OUT	Voltage detection output pin
4	CP*2	Connection pin for release delay capacitor
5	VSS	GND pin
6	CN*3	Connection pin for detection delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.
***2.** Connect a capacitor between the CP pin and the VSS pin.
The release delay time can be adjusted according to the capacitance.
Moreover, the CP pin is available even when it is open.
***3.** Connect a capacitor between the CN pin and the VSS pin.
The detection delay time can be adjusted according to the capacitance.
Moreover, the CN pin is available even when it is open.

2. S-19110 Series N / P / Q / R type (SENSE detection product)

2. 1 SOT-23-6

Top view

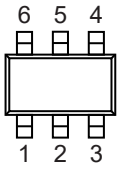


Figure 7

Table 4

Pin No.	Symbol	Description
1	VDD	Voltage input pin
2	SENSE	Detection voltage input pin
3	OUT	Voltage detection output pin
4	CP*1	Connection pin for release delay capacitor
5	VSS	GND pin
6	CN*2	Connection pin for detection delay capacitor

***1.** Connect a capacitor between the CP pin and the VSS pin.
The release delay time can be adjusted according to the capacitance.
Moreover, the CP pin is available even when it is open.
***2.** Connect a capacitor between the CN pin and the VSS pin.
The detection delay time can be adjusted according to the capacitance.
Moreover, the CN pin is available even when it is open.

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■ Absolute Maximum Ratings

Table 5

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD} – V_{SS}	V_{SS} – 0.3 to V_{SS} + 45	V
SENSE pin input voltage	V_{SENSE}	V_{SS} – 0.3 to V_{SS} + 45	V
CP pin input voltage	V_{CP}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
CN pin input voltage	V_{CN}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
Output voltage	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 45	V
Output current	I_{OUT}	25	mA
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-6	Board A	–	159	–	°C/W
			Board B	–	124	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

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■ Electrical Characteristics

1. VDD detection product

Table 7

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	3.6 V ≤ $-V_{DET(S)}$ ≤ 4.15 V		$-V_{DET(S)} \times 0.970$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.030$	V	1
		4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V		$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1
Release voltage*2	$+V_{DET}$	J / K type 5.0% ≤ V_{HYS} ≤ 20.0%*3	3.6 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$+V_{DET(S)} \times 0.970$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.030$	V	1
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$+V_{DET(S)} \times 0.975$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.025$	V	1
		J / K type 20.0% < V_{HYS} ≤ 30.0%*3	3.6 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$+V_{DET(S)} \times 0.965$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.035$	V	1
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$+V_{DET(S)} \times 0.970$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.030$	V	1
		L / M type V_{HYS} = 0%*4	3.6 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$-V_{DET(S)} \times 0.970$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.030$	V	–
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	–
Current consumption	I_{SS}	J / K / L / M type V_{DD} = $-V_{DET}$ – 0.1 V		–	0.60	1.60	µA	2
		J / K type V_{DD} = $+V_{DET}$ + 0.1 V		–	0.60	1.60	µA	2
Operation voltage	V_{DD}	–		1.8	–	36.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*5 = 0.05 V	V_{DD} = 2.9 V, Active "L"	0.31	–	–	mA	3
			V_{DD} = 6.9 V, Active "H"	0.45	–	–	mA	3
Leakage current	I_{LEAK}	Output transistor Nch	V_{DD} = 30.0 V, V_{OUT} = 30.0 V, Active "L"	–	–	2.0	µA	3
			V_{DD} = 2.9 V, V_{OUT} = 30.0 V, Active "H"	–	–	2.0	µA	3
Detection delay time*6	t_{RESET}	C_N = 3.3 nF		8.0	10.0	12.0	ms	4
Release delay time	t_{DELAY}	J / K type*7 C_P = 3.3 nF		8.0	10.0	12.0	ms	4
		L / M type*8 C_P = 3.3 nF		8.0	10.0	12.0	ms	4
CP pin discharge ON resistance	R_{CP}	V_{DD} = 6.9 V, V_{CP} = 0.5 V		0.52	–	2.2	kΩ	–
CN pin discharge ON resistance	R_{CN}	V_{DD} = 2.9 V, V_{CN} = 0.5 V		1.0	–	5.0	kΩ	–

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value

***2.** $+V_{DET}$: Actual release voltage value, $+V_{DET(S)}$: Set release voltage value

***3.** Although the hysteresis width can be set in the range of 5.0% to 30.0%, the release voltage accuracy differs when the setting range exceeds 20.0%.

***4.** The hysteresis width is "unavailable", so release voltage = detection voltage.

***5.** V_{DS}: Drain-to-source voltage of the output transistor

***6.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 0.5 V → $-V_{DET(S)}$ – 0.5 V is applied to the VDD pin to when V_{OUT} reaches V_{DD} / 2, after the power supply voltage (V_{DD}) reaches the release voltage once.

***7.** The time period from when the pulse voltage of $+V_{DET(S)}$ – 0.5 V → $+V_{DET(S)}$ + 0.5 V is applied to the VDD pin to when V_{OUT} reaches V_{DD} / 2.

***8.** The time period from when the pulse voltage of $-V_{DET(S)}$ – 0.5 V → $-V_{DET(S)}$ + 0.5 V is applied to the VDD pin to when V_{OUT} reaches V_{DD} / 2

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2. SENSE detection product

Table 8

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	V_{DD} = 16.0 V	3.0 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$-V_{DET(S)} \times 0.970$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.030$	V	1
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1
Release voltage*2	$+V_{DET}$	N / P type V_{DD} = 16.0 V 5.0% ≤ V_{HYS} ≤ 20.0%*3	3.0 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$+V_{DET(S)} \times 0.970$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.030$	V	1
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$+V_{DET(S)} \times 0.975$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.025$	V	1
		N / P type V_{DD} = 16.0 V 20.0% < V_{HYS} ≤ 30.0%*3	3.0 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$+V_{DET(S)} \times 0.965$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.035$	V	1
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$+V_{DET(S)} \times 0.970$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.030$	V	1
		Q / R type V_{DD} = 16.0 V V_{HYS} = 0%*4	3.0 V ≤ $-V_{DET(S)}$ ≤ 4.15 V	$-V_{DET(S)} \times 0.970$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.030$	V	1
			4.2 V ≤ $-V_{DET(S)}$ ≤ 4.95 V	$-V_{DET(S)} \times 0.975$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025$	V	1
Current consumption*5	I_{SS}	N / P / Q / R type V_{DD} = 16.0 V, V_{SENSE} = $-V_{DET}$ – 0.1 V		–	0.55	1.55	µA	2
		N / P type V_{DD} = 16.0 V, V_{SENSE} = $+V_{DET}$ + 0.1 V		–	0.55	1.55	µA	2
Operation voltage	V_{DD}	–		3.0	–	36.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*6 = 0.05 V	V_{DD} = 5.0 V, V_{SENSE} = 2.9 V, Active "L"	0.45	–	–	mA	3
			V_{DD} = 5.0 V, V_{SENSE} = 6.9 V, Active "H"	0.45	–	–	mA	3
Leakage current	I_{LEAK}	Output transistor Nch	V_{DD} = 30.0 V, V_{OUT} = 30.0 V, V_{SENSE} = 30.0 V, Active "L"	–	–	2.0	µA	3
			V_{DD} = 30.0 V, V_{OUT} = 30.0 V, V_{SENSE} = 2.9 V, Active "H"	–	–	2.0	µA	3
Detection delay time*7	t_{RESET}	C_N = 3.3 nF		8.0	10.0	12.0	ms	4
Release delay time	t_{DELAY}	N / P type*8, C_P = 3.3 nF		8.0	10.0	12.0	ms	4
		Q / R type*9, C_P = 3.3 nF		8.0	10.0	12.0	ms	4
SENSE pin resistance	R_{SENSE}	–		6.8	–	275	MΩ	–
CP pin discharge ON resistance	R_{CP}	V_{DD} = 3.0 V, V_{SENSE} = 6.9 V, V_{CP} = 0.5 V		0.72	–	4.29	kΩ	–
CN pin discharge ON resistance	R_{CN}	V_{DD} = 3.0 V, V_{SENSE} = 2.9 V, V_{CN} = 0.5 V		0.72	–	4.29	kΩ	–

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value

***2.** $+V_{DET}$: Actual release voltage value, $+V_{DET(S)}$: Set release voltage value

***3.** Although the hysteresis width can be set in the range of 5.0% to 30.0%, the release voltage accuracy differs when the setting range exceeds 20.0%.

***4.** The hysteresis width is "unavailable", so release voltage = detection voltage.

***5.** The current flowing through the SENSE pin resistance is not included.

***6.** V_{DS}: Drain-to-source voltage of the output transistor

***7.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 0.5 V → $-V_{DET(S)}$ – 0.5 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2, after voltage of 16.0 V is applied to the VDD pin and the SENSE pin input voltage (V_{SENSE}) reaches the release voltage once.

***8.** The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of $+V_{DET(S)}$ – 0.5 V → $+V_{DET(S)}$ + 0.5 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2.

***9.** The time period from when voltage of 16.0 V is applied to the VDD pin and the pulse voltage of $-V_{DET(S)}$ – 0.5 V → $-V_{DET(S)}$ + 0.5 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2.

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■ Test Circuits

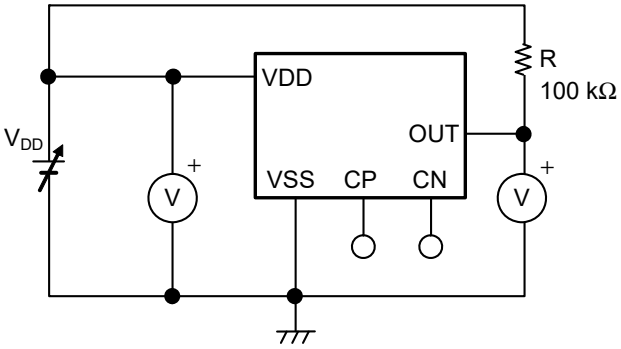


Figure 8 Test Circuit 1 (VDD Detection Product)

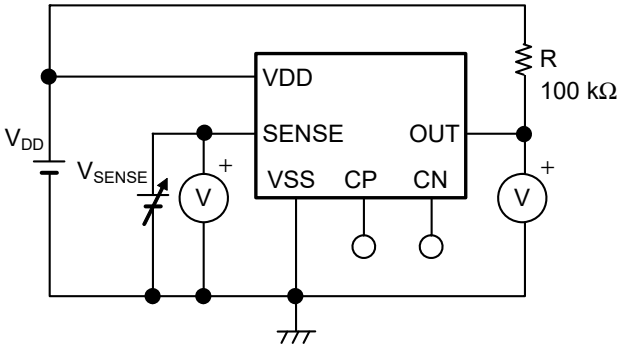


Figure 9 Test Circuit 1 (SENSE Detection Product)

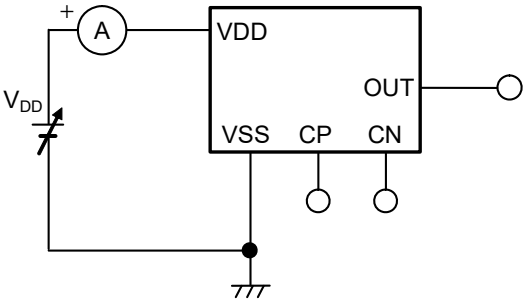


Figure 10 Test Circuit 2 (VDD Detection Product)

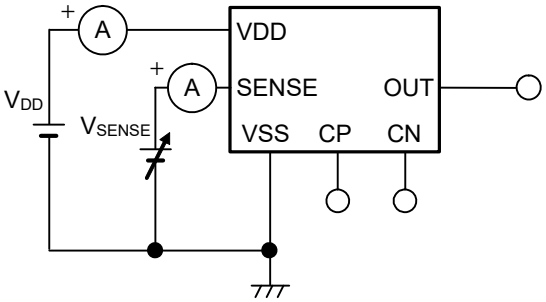


Figure 11 Test Circuit 2 (SENSE Detection Product)

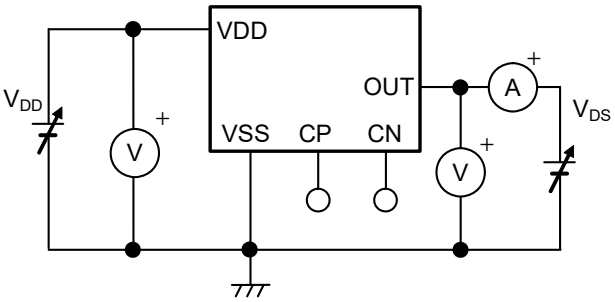


Figure 12 Test Circuit 3 (VDD Detection Product)

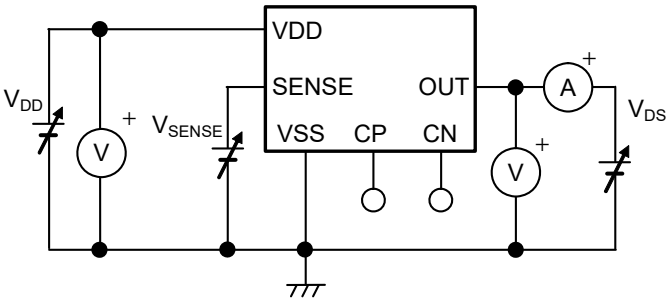


Figure 13 Test Circuit 3 (SENSE Detection Product)

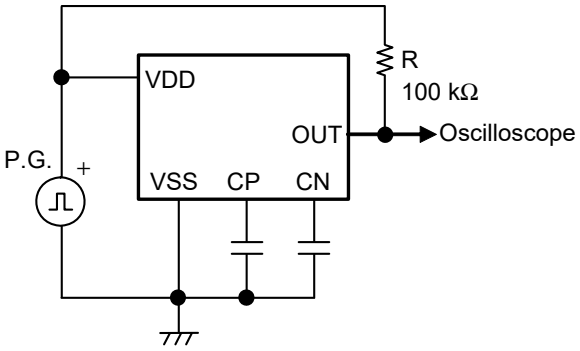


Figure 14 Test Circuit 4 (VDD Detection Product)

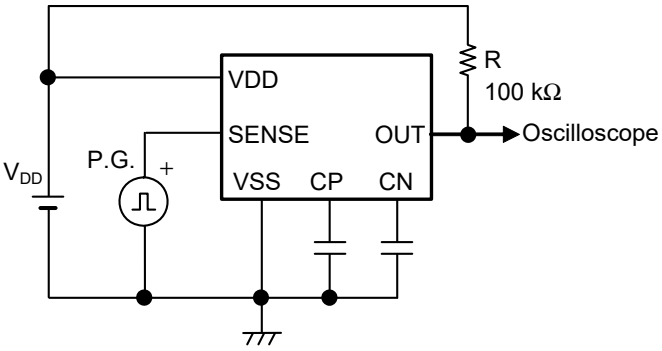
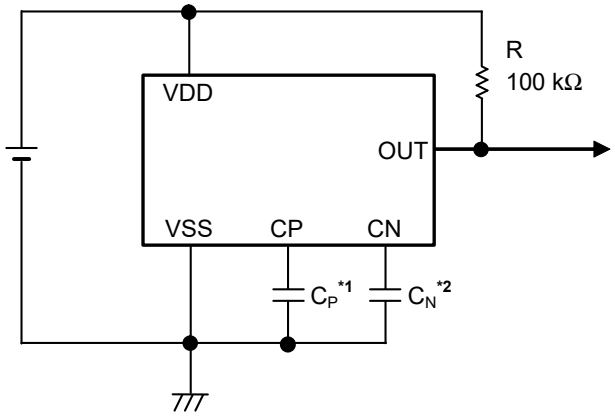


Figure 15 Test Circuit 4 (SENSE Detection Product)

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■ Standard Circuits

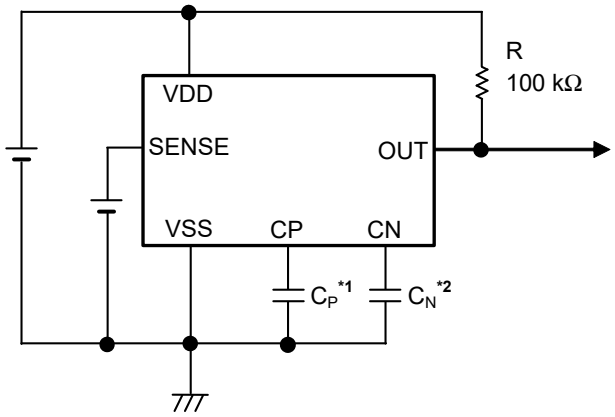
1. VDD detection product



***1.** The delay capacitor (C_P) should be connected directly to the CP pin and the VSS pin.
***2.** The delay capacitor (C_N) should be connected directly to the CN pin and the VSS pin.

Figure 16

2. SENSE detection product



***1.** The delay capacitor (C_P) should be connected directly to the CP pin and the VSS pin.
***2.** The delay capacitor (C_N) should be connected directly to the CN pin and the VSS pin.

Figure 17

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 22** or **Figure 23** turns to "H" for active "H", and "L" for active "L" (VDD detection product: V_{DD}, SENSE detection product: V_{SENSE}). The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 18**, **Figure 20**).

Example: In $-V_{DET}$ = 3.0 V product, the detection voltage is either one in the range of 2.910 V ≤ $-V_{DET}$ ≤ 3.090 V.
This means that some $-V_{DET}$ = 3.0 V product have $-V_{DET}$ = 2.910 V and some have $-V_{DET}$ = 3.090 V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 22** or **Figure 23** turns to "L" for active "H", and "H" for active "L" (VDD detection product: V_{DD}, SENSE detection product: V_{SENSE}).
The difference of detection voltage and release voltage can be set in the range of 5.0% to 30.0% (Refer to "**Figure 5 Detection Voltage and Release Voltage Possible Setting Area**").
The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 19**, **Figure 21**).
Release voltage accuracy is ±2.5% ($-V_{DET(S)}$ = 4.2 V to 4.95 V) or ±3.0% ($-V_{DET(S)}$ = 3.0 V to 4.15 V) when hysteresis width = 5.0% to 20.0%, ±3.0% ($-V_{DET(S)}$ = 4.2 V to 4.95 V) or ±3.5% ($-V_{DET(S)}$ = 3.0 V to 4.15 V) when hysteresis width = 20.0% to 30.0%.
In the S-19110 Series L / M / Q / R type, the release voltage ($+V_{DET}$) is the same value as the actual detection voltage ($-V_{DET}$) of a product.

Example 1: For $-V_{DET}$ = 4.0 V, $+V_{DET}$ = 4.4 V (hysteresis width = 10.0%), the release voltage is either one in the range of 4.268 V ≤ $+V_{DET}$ ≤ 4.532 V.
This means that some $-V_{DET}$ = 4.0 V, $+V_{DET}$ = 4.4 V product have $+V_{DET}$ = 4.268 V and some have $+V_{DET}$ = 4.532 V.

Example 2: For $-V_{DET}$ = 4.0 V, $+V_{DET}$ = 5.2 V (hysteresis width = 30.0%), the release voltage is either one in the range of 5.018 V ≤ $+V_{DET}$ ≤ 5.382 V.
This means that some $-V_{DET}$ = 4.0 V, $+V_{DET}$ = 5.2 V product have $+V_{DET}$ = 5.018 V and some have $+V_{DET}$ = 5.382 V.

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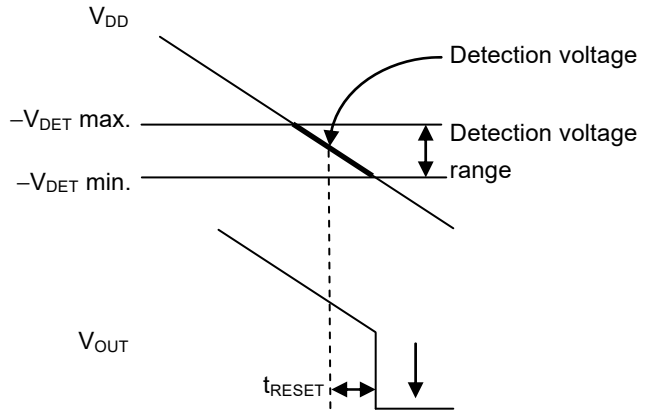


Figure 18 Detection Voltage (VDD Detection Product)

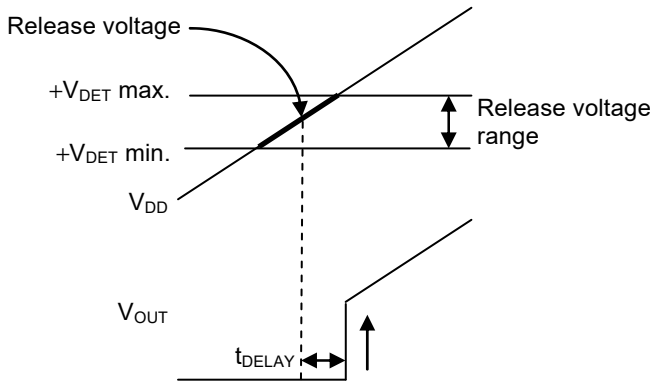


Figure 19 Release Voltage (VDD Detection Product)

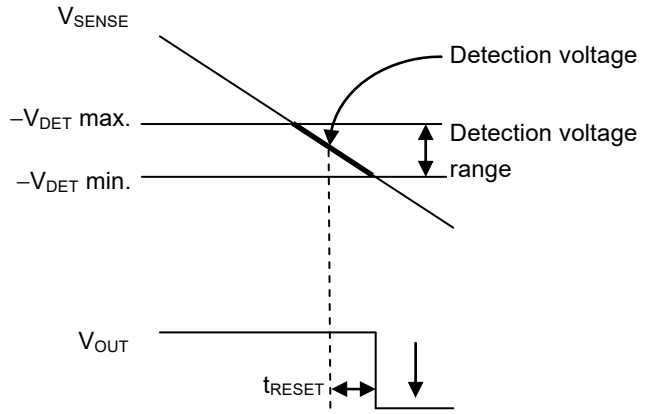


Figure 20 Detection Voltage (SENSE Detection Product)

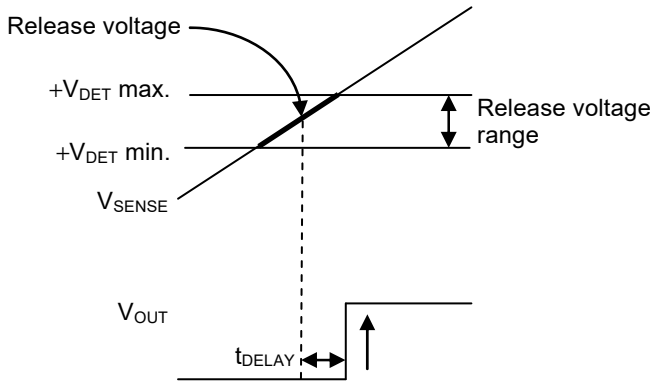


Figure 21 Release Voltage (SENSE Detection Product)

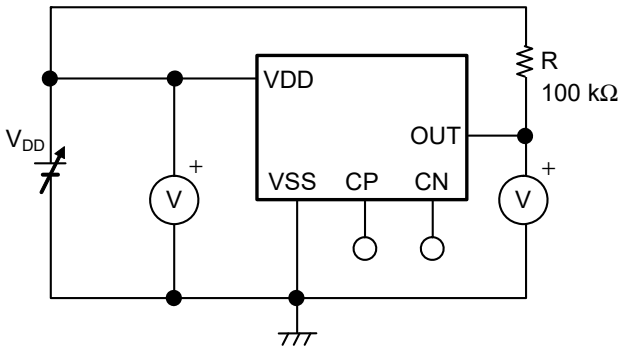


Figure 22 Test Circuit of Detection Voltage and Release Voltage (VDD Detection Product)

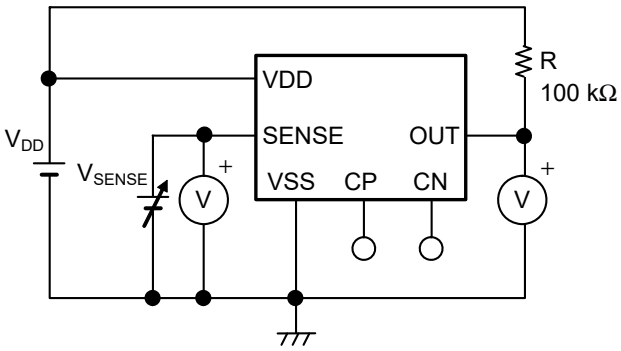


Figure 23 Test Circuit of Detection Voltage and Release Voltage (SENSE Detection Product)

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B – the voltage at point A = V_{HYS} in **Figure 25**, **Figure 27**, **Figure 33** and **Figure 35**). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

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■ Operation

1. Basic operation

1. 1 S-19110 Series J type

(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

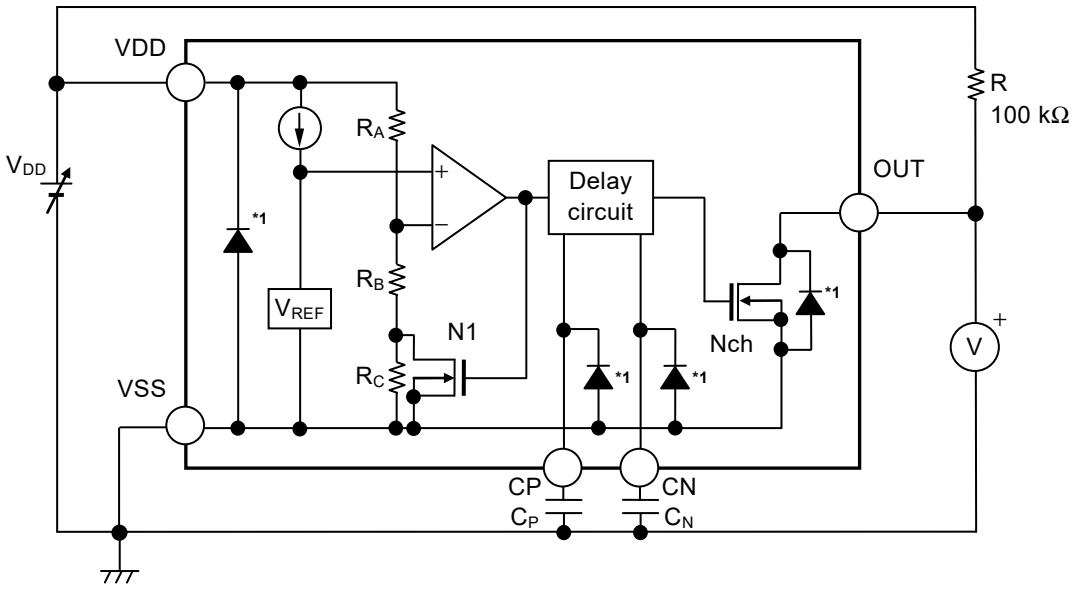
(2) Even if V_{DD} decreases to $+V_{DET}$ or lower, V_{DD} is output when V_{DD} is higher than the detection voltage ($-V_{DET}$). When V_{DD} decreases to $-V_{DET}$ or lower (point A in **Figure 25**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is unstable when V_{DD} decreases to the IC's minimum operation voltage or lower. V_{DD} is output when the output is pulled up.

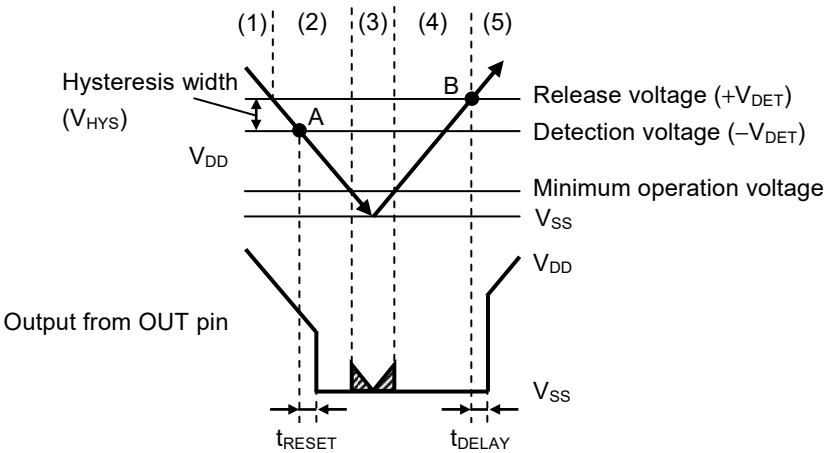
(4) V_{SS} is output by increasing V_{DD} to the minimum operation voltage or higher. Even if V_{DD} exceeds $-V_{DET}$, V_{SS} is output when V_{DD} is lower than $+V_{DET}$.

(5) When V_{DD} increases to $+V_{DET}$ or higher (point B in **Figure 25**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.



***1.** Parasitic diode

Figure 24 Operation of S-19110 Series J Type



Remark When V_{DD} is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

Figure 25 Timing Chart of S-19110 Series J Type

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1. 2 S-19110 Series K type

(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned on to output V_{SS} ("L").

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

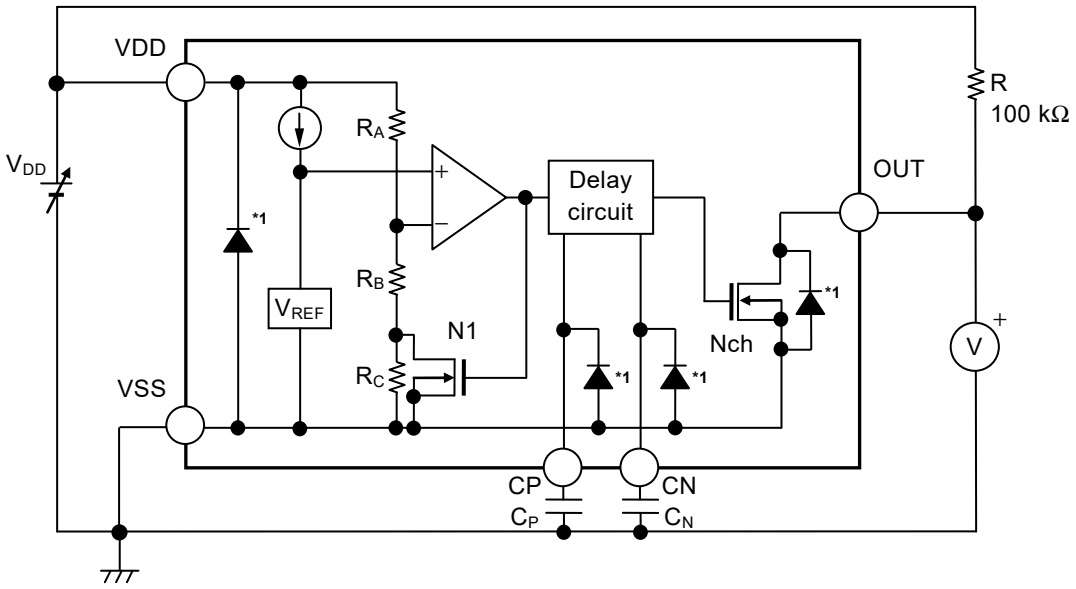
(2) Even if V_{DD} decreases to $+V_{DET}$ or lower, V_{SS} is output when V_{DD} is higher than the detection voltage ($-V_{DET}$). When V_{DD} decreases to $-V_{DET}$ or lower (point A in **Figure 27**), the Nch transistor is turned off. And then V_{DD} ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is unstable when V_{DD} decreases to the IC's minimum operation voltage or lower. V_{DD} is output when the output is pulled up.

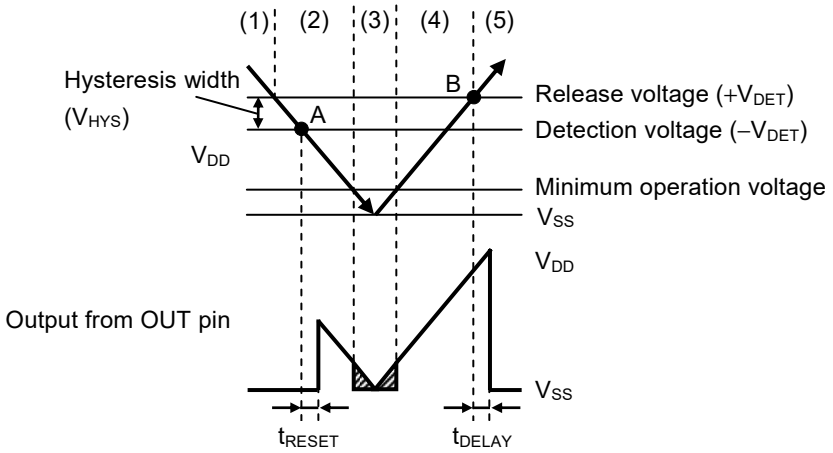
(4) V_{DD} is output by increasing V_{DD} to the minimum operation voltage or higher. Even if V_{DD} exceeds $-V_{DET}$, V_{DD} is output when V_{DD} is lower than $+V_{DET}$.

(5) When V_{DD} increases to $+V_{DET}$ or higher (point B in **Figure 27**), the Nch transistor is turned on. And then V_{SS} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).



1. Parasitic diode

Figure 26 Operation of S-19110 Series K Type



Remark When V_{DD} is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

Figure 27 Timing Chart of S-19110 Series K Type

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1. 3 S-19110 Series L type

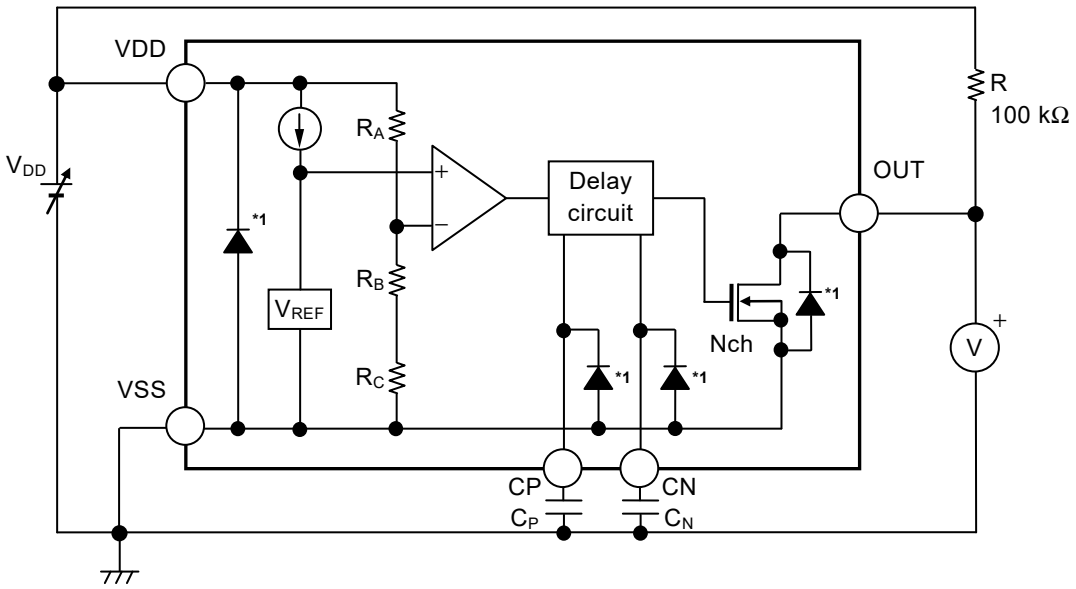
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) When V_{DD} decreases to the detection voltage ($-V_{DET}$) or lower (point A in **Figure 29**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

(3) The output is unstable when V_{DD} decreases to the IC's minimum operation voltage or lower. V_{DD} is output when the output is pulled up.

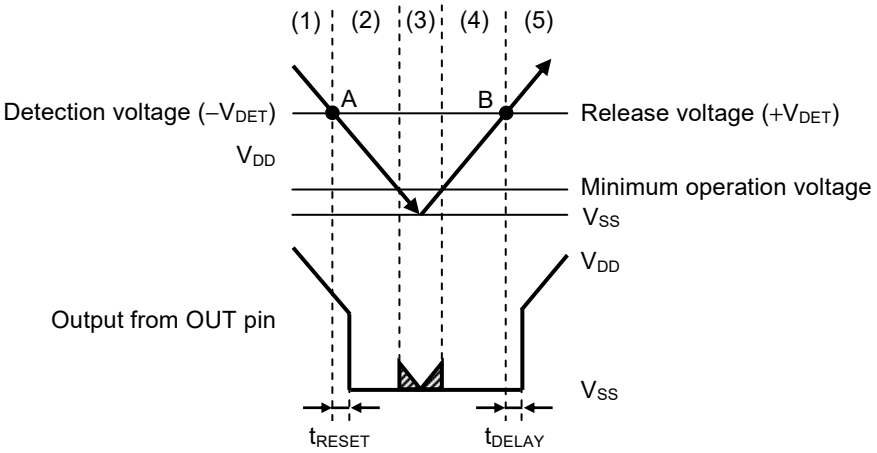
(4) V_{SS} is output by increasing V_{DD} to the minimum operation voltage or higher.

(5) When V_{DD} increases to $+V_{DET}$ or higher (point B in **Figure 29**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.



1. Parasitic diode

Figure 28 Operation of S-19110 Series L Type



Remark 1. When V_{DD} is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

2. The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 29 Timing Chart of S-19110 Series L Type

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1. 4 S-19110 Series M type

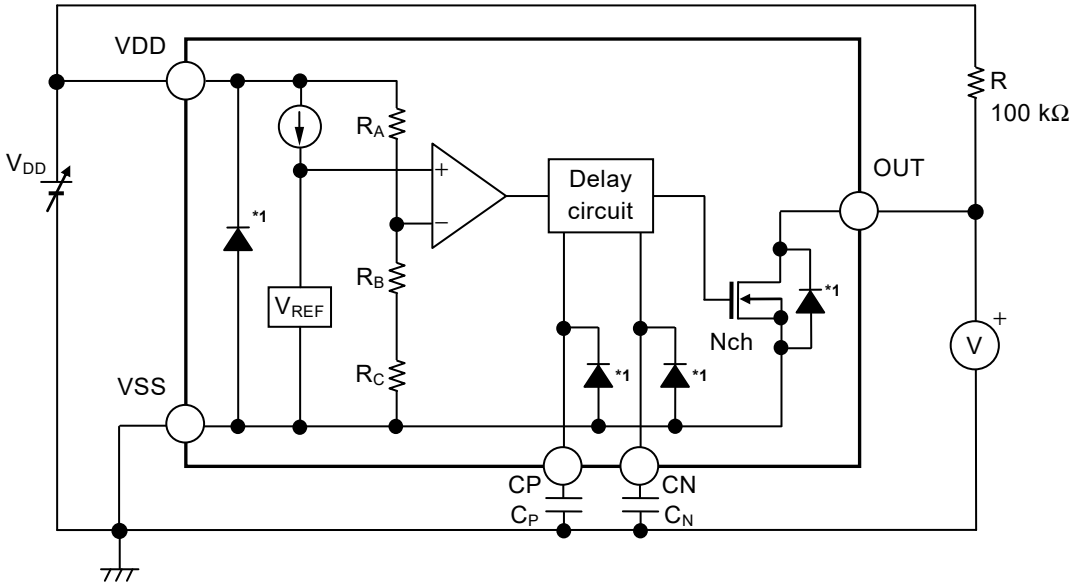
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned on to output V_{SS} ("L").
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) When V_{DD} decreases to the detection voltage ($-V_{DET}$) or lower (point A in **Figure 31**), the Nch transistor is turned off. And then V_{DD} ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}) when the output is pulled up.

(3) The output is unstable when V_{DD} decreases to the IC's minimum operation voltage or lower. V_{DD} is output when the output is pulled up.

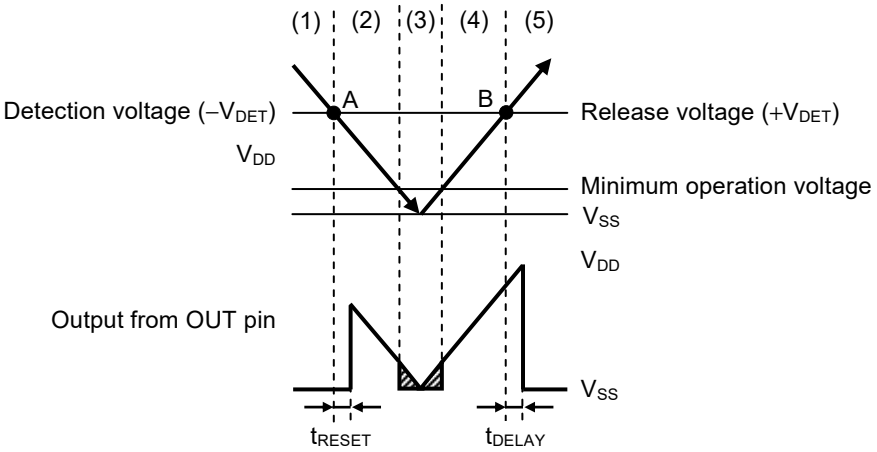
(4) V_{DD} is output by increasing V_{DD} to the minimum operation voltage or higher.

(5) When V_{DD} increases to $+V_{DET}$ or higher (point B in **Figure 31**), the Nch transistor is turned on. And then V_{SS} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).



***1.** Parasitic diode

Figure 30 Operation of S-19110 Series M Type



Remark 1. When V_{DD} is the minimum operation voltage or lower, the output voltage from the OUT pin is unstable in the shaded area.

2. The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 31 Timing Chart of S-19110 Series M Type

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1. 5 S-19110 Series N type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if V_{SENSE} decreases to $+V_{DET}$ or lower, V_{DD} is output when V_{SENSE} is higher than the detection voltage ($-V_{DET}$).

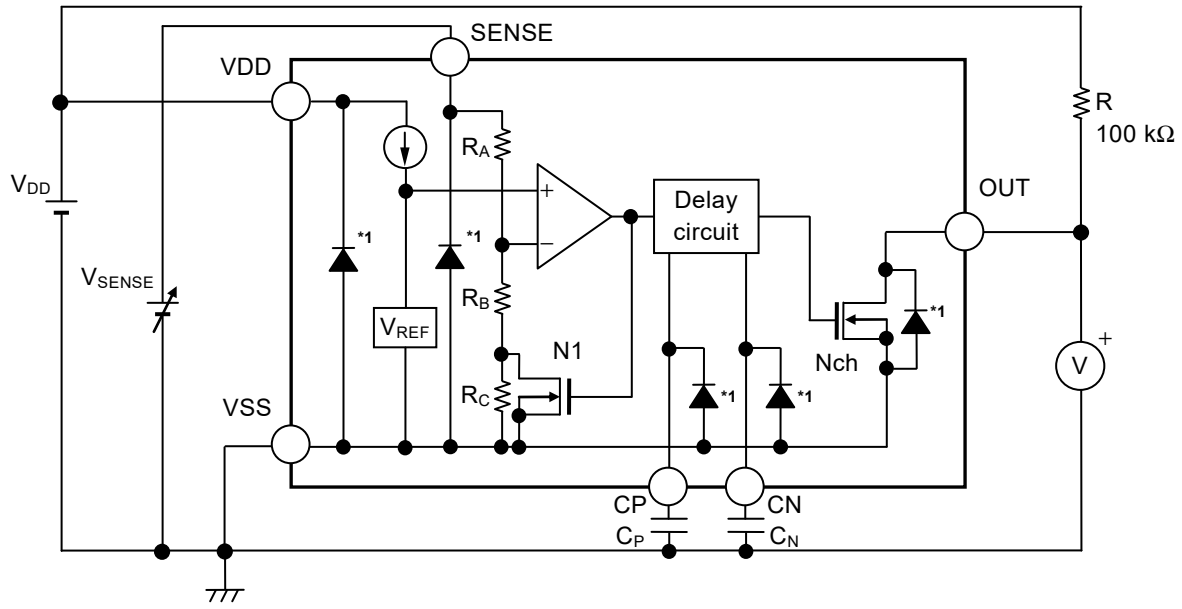
When V_{SENSE} decreases to $-V_{DET}$ or lower (point A in **Figure 33**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} exceeds $-V_{DET}$, V_{SS} is output when V_{SENSE} is lower than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or higher (point B in **Figure 33**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.



1. Parasitic diode

Figure 32 Operation of S-19110 Series N Type

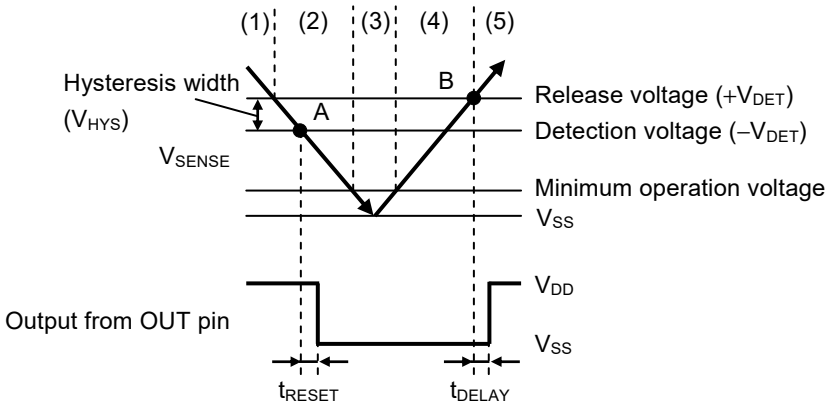


Figure 33 Timing Chart of S-19110 Series N Type

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1. 6 S-19110 Series P type

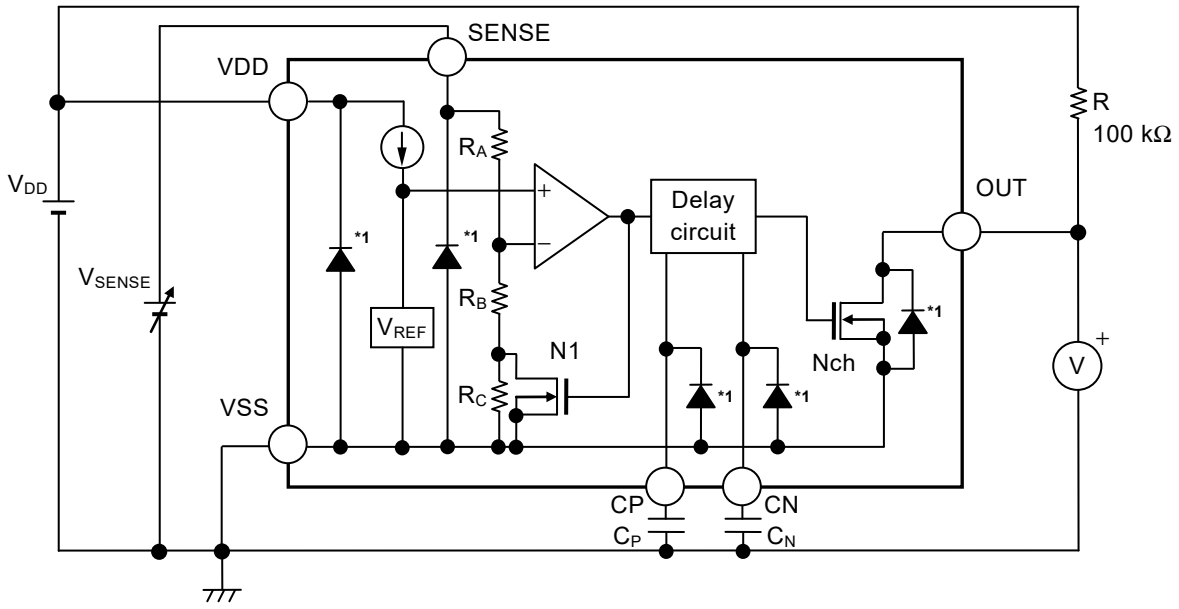
(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned on to output V_{SS} ("L").
Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if V_{SENSE} decreases to $+V_{DET}$ or lower, V_{SS} is output when V_{SENSE} is higher than the detection voltage ($-V_{DET}$).
When V_{SENSE} decreases to $-V_{DET}$ or lower (point A in **Figure 35**), the Nch transistor is turned off. And then V_{DD} ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}) when the output is pulled up.
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} exceeds $-V_{DET}$, V_{DD} is output when V_{SENSE} is lower than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or higher (point B in **Figure 35**), the Nch transistor is turned on. And then V_{SS} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).



***1.** Parasitic diode

Figure 34 Operation of S-19110 Series P Type

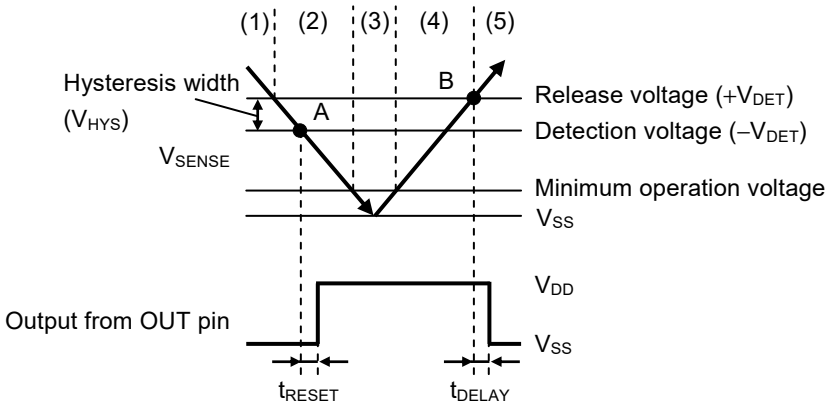


Figure 35 Timing Chart of S-19110 Series P Type

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1. 7 S-19110 Series Q type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

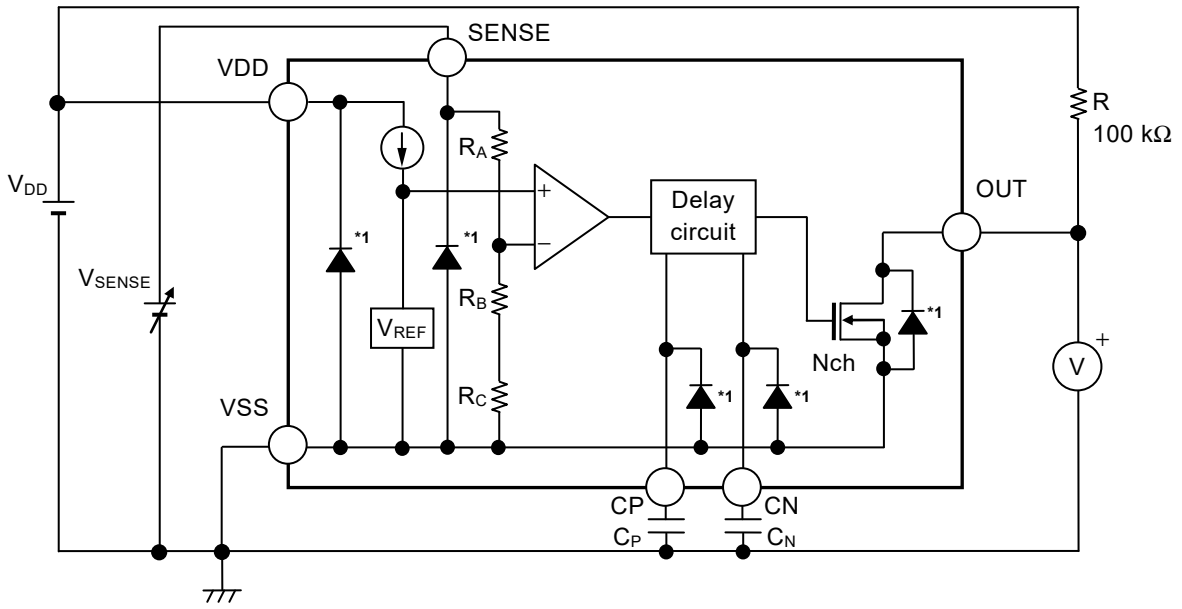
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) When V_{SENSE} decreases to the detection voltage ($-V_{DET}$) or lower (point A in **Figure 37**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}).

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

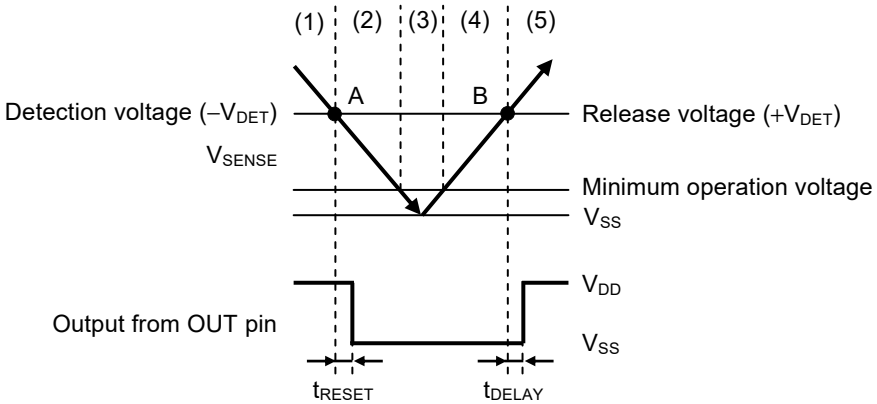
(4) Even if V_{SENSE} increases, V_{SS} is output when V_{SENSE} is lower than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or higher (point B in **Figure 37**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.



1. Parasitic diode

Figure 36 Operation of S-19110 Series Q Type



Remark The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 37 Timing Chart of S-19110 Series Q Type

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1. 8 S-19110 Series R type

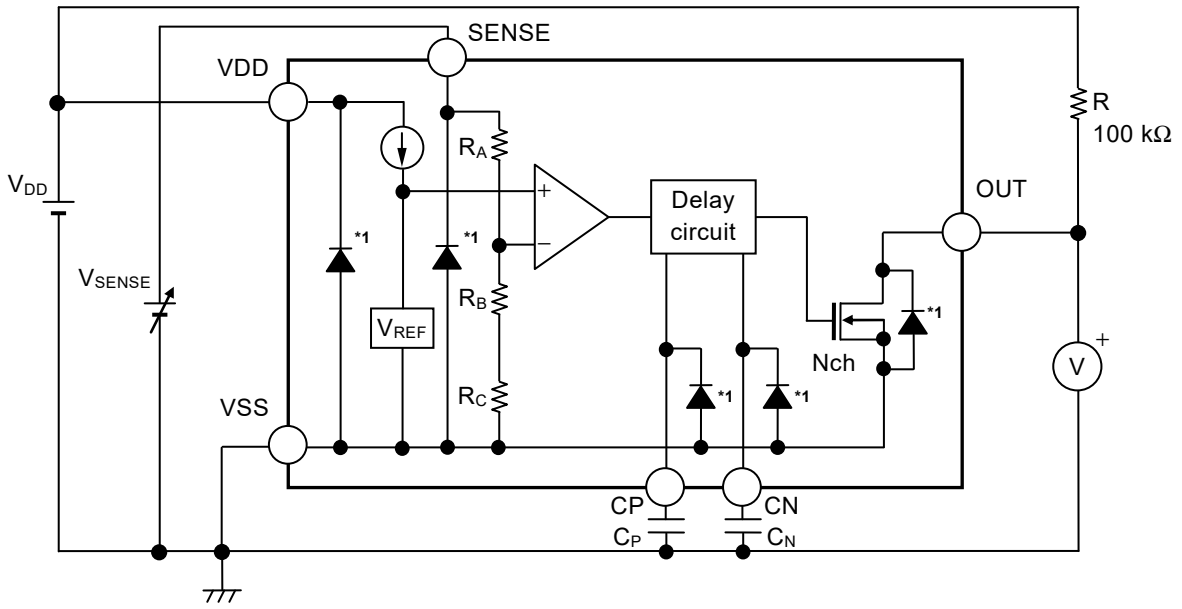
(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned on to output V_{SS} ("L").
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) When V_{SENSE} decreases to the detection voltage ($-V_{DET}$) or lower (point A in **Figure 39**), the Nch transistor is turned off. And then V_{DD} ("H") is output from the OUT pin after the elapse of the detection delay time (t_{RESET}) when the output is pulled up.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

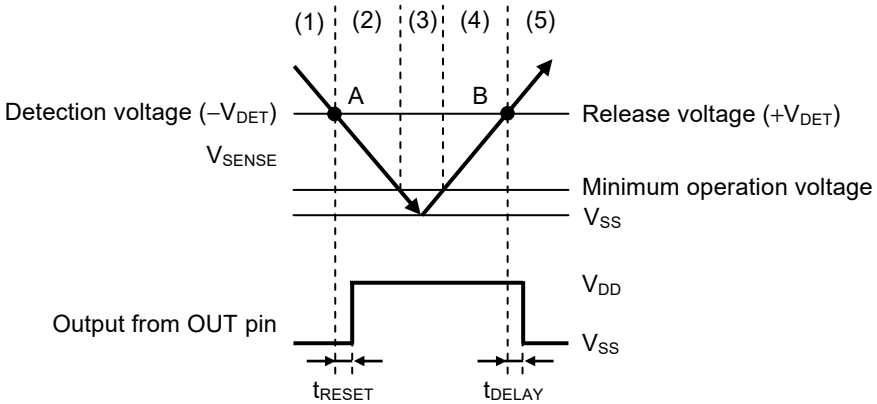
(4) Even if V_{SENSE} increases, V_{DD} is output when V_{SENSE} is lower than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or higher (point B in **Figure 39**), the Nch transistor is turned on. And then V_{SS} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}).



1. Parasitic diode

Figure 38 Operation of S-19110 Series R Type



Remark The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 39 Timing Chart of S-19110 Series R Type

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2. Delay circuit

The delay circuit has a function that adjusts the detection delay time (t_{RESET}) from when the power supply voltage (V_{DD}) or SENSE pin voltage (V_{SENSE}) reaches the detection voltage ($-V_{DET}$) or lower to when the output from OUT pin inverts.
It also has a function that adjusts the release delay time (t_{DELAY}) from when the power supply voltage (V_{DD}) or SENSE pin voltage (V_{SENSE}) reaches the release voltage ($+V_{DET}$) to when the output from OUT pin inverts.
t_{RESET} is determined by the delay coefficient, the delay capacitor (C_N) and the detection delay time when the CN pin is open (t_{RESET0}), and the t_{DELAY} is determined by the delay coefficient, the delay capacitor (C_P) and the release delay time when the CP pin is open (t_{DELAY0}). They are calculated by the equations below.

t_{RESET} [ms] = Delay coefficient $\times$ C_N [nF] + t_{RESET0} [ms]
t_{DELAY} [ms] = Delay coefficient $\times$ C_P [nF] + t_{DELAY0} [ms]

Table 9

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +125°C	2.41	2.85	3.32
Ta = +105°C	2.41	2.85	3.32
Ta = +25°C	2.41	2.86	3.30
Ta = –40°C	2.40	2.83	3.25

Table 10

Operation Temperature	Detection Delay Time when CN Pin is Open (t_{RESET0})	Release Delay Time when CP Pin is Open (t_{DELAY0})
	Typ.	Typ.
Ta = –40°C to +125°C	0.35 ms	0.35 ms

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CN pin or CP pin since the impedance of the CN pin and CP pin are high, otherwise correct delay time cannot be provided.

2. There is no limit for the capacitance of C_N and C_P as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 300 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.

3. The above equations will not guarantee successful operation. Determine the capacitance of C_N and C_P through thorough evaluation including temperature characteristics in the actual usage conditions.
When using an X8R equivalent capacitor, refer to the "2. Detection delay time (t_{RESET}) vs. Temperature (Ta)", "3. Detection delay time (t_{RESET}) vs. Power supply voltage (V_{DD})", "5. Release delay time (t_{DELAY}) vs. Temperature (Ta)" and "6. Release delay time (t_{DELAY}) vs. Power supply voltage (V_{DD})" in "■ Reference Data" for details.

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■ Usage Precautions

1. Feed-through current during detection and release

In the S-19110 Series, the feed-through current flows at the time of detection and release. For this reason, if the input impedance is high, oscillation may occur due to voltage drop caused by the feed-through current.
When using the S-19110 Series in configurations like those shown in **Figure 40** and **Figure 41**, it is recommended that input impedance be set to 1 kΩ or less.
Determine the impedance through thorough evaluation including temperature characteristics.

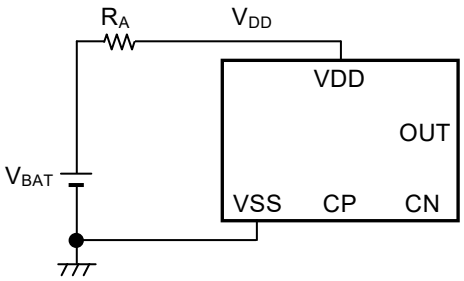


Figure 40 VDD Detection Product

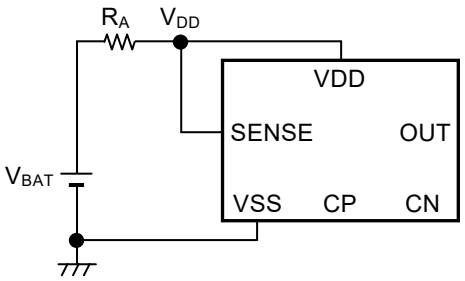


Figure 41 SENSE Detection Product

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2. Power on and shut down sequence

SENSE detection products monitor SENSE pin voltage (V_{SENSE}) while power is being supplied to the VDD pin.
Apply power in the order, the VDD pin then the SENSE pin.
In addition, when shutting down VDD pin, shut down the SENSE pin first, and shut down the VDD pin after the detection delay time (t_{RESET}) has elapsed.

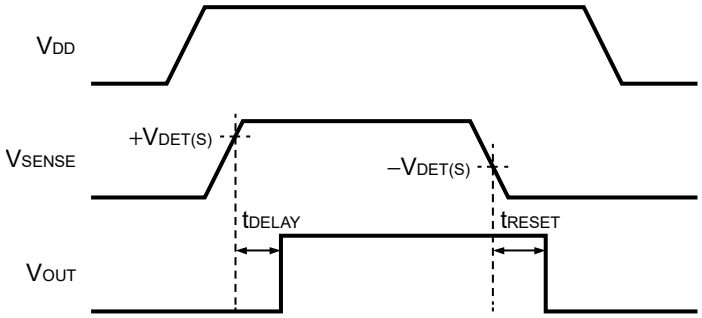


Figure 42

3. Falling power (reference)

Figure 43 shows the relation between V_{DD} amplitude (V_{P-P}) and input voltage falling time (t_F) where the release status can be maintained when the VDD pin (VDD detection product) sharply drops to a voltage equal to or higher than the detection voltage ($-V_{DET}$) during release status.

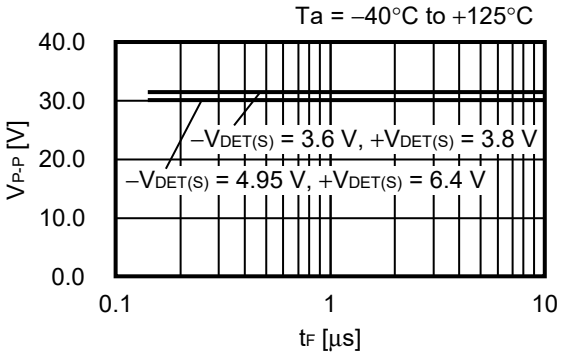
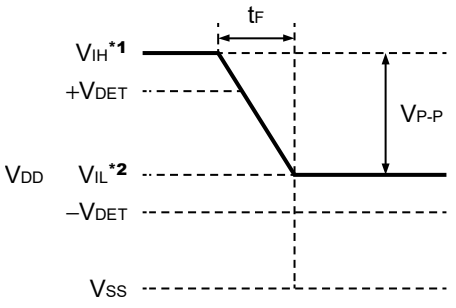


Figure 43



***1.** V_{IH} = 36.0 V
***2.** $V_{IL} = -V_{DET(S)} + 1.0$ V

Figure 44 VDD Pin Input Voltage Waveform

Caution Figure 43 shows the input voltage conditions which can maintain the release status. If the voltage whose V_{P-P} and t_F are larger than these conditions is input to the VDD pin (VDD detection product), the OUT pin may change to a detection status.

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4. VDD pin, SENSE pin voltage glitch (reference)

4. 1 Detection operation

Figure 45 and **Figure 46** show the relation between pulse width and pulse voltage difference (V_{OD}) where the release status can be maintained when a pulse equal to or lower than the detection voltage ($-V_{DET}$) is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product) during release status.

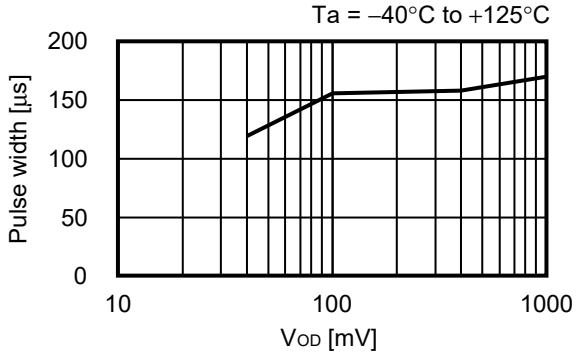


Figure 45 VDD Detection Product

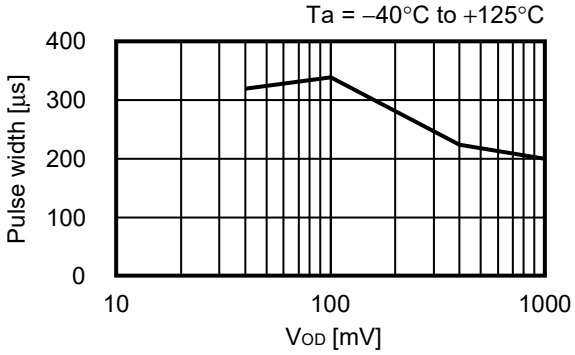
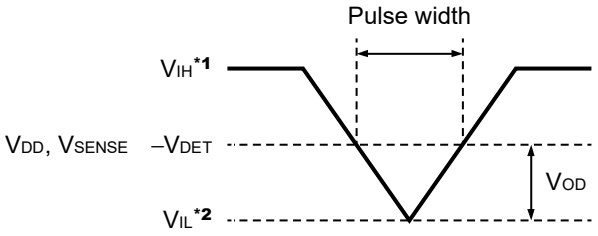


Figure 46 SENSE Detection Product



***1.** V_{IH} = 16.0 V
***2.** $V_{IL} = -V_{DET} - V_{OD}$

Figure 47 VDD Pin, SENSE Pin Input Voltage Waveform

Caution Figure 45 and Figure 46 show the pulse conditions which can maintain the release status. If the pulse whose pulse width and V_{OD} are larger than these conditions is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product), the OUT pin may change to a detection status.

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4. 2 Release operation

Figure 48 and **Figure 49** show the relation between pulse width and pulse voltage difference (V_{OD}) where the detection status can be maintained when a pulse equal to or higher than the release voltage ($+V_{DET}$) is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product) during detection status.

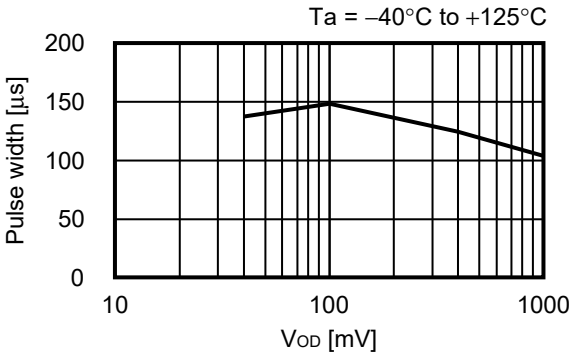


Figure 48 VDD Detection Product

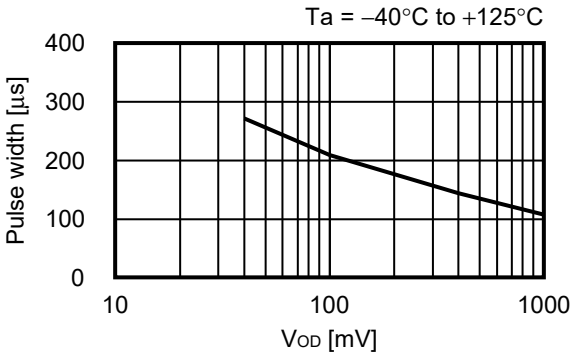
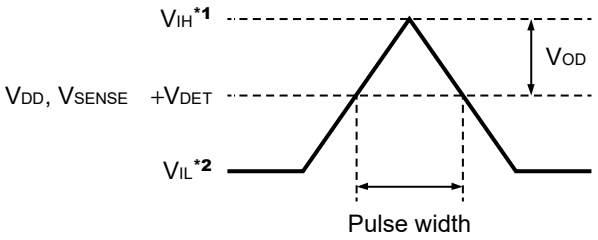


Figure 49 SENSE Detection Product



***1.** $V_{IH} = +V_{DET} + V_{OD}$
***2.** $V_{IL} = +V_{DET} – 1.0$ V

Figure 50 VDD Pin, SENSE Pin Input Voltage Waveform

Caution Figure 48 and Figure 49 show the pulse conditions which can maintain the detection status. If the pulse whose pulse width and V_{OD} are larger than these conditions is input to the VDD pin (VDD detection product) or SENSE pin (SENSE detection product), the OUT pin may change to a release status.

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5. Detection delay time accuracy (reference)

Figure 51 and **Figure 52** show the relation between V_{DD} amplitude (V_{P-P}) and input voltage falling time (t_F) where the arbitrarily set detection delay time accuracy can be maintained when the VDD pin (VDD detection product) sharply drops.

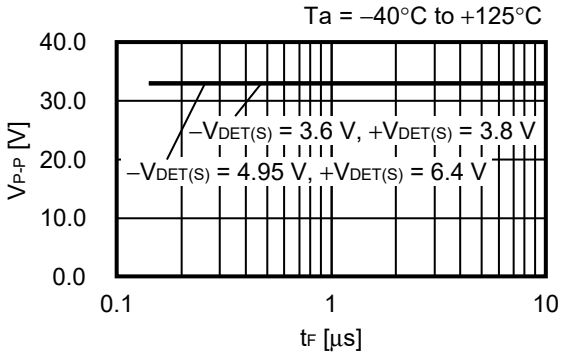


Figure 51 C_N = 3.3 nF

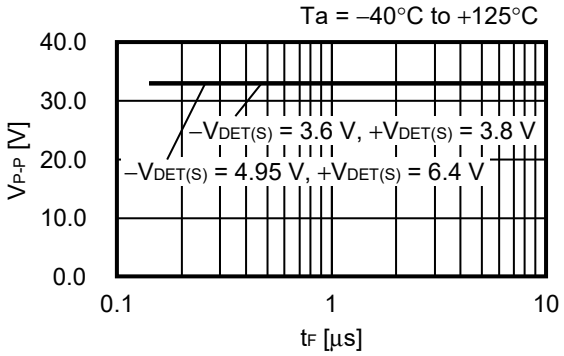
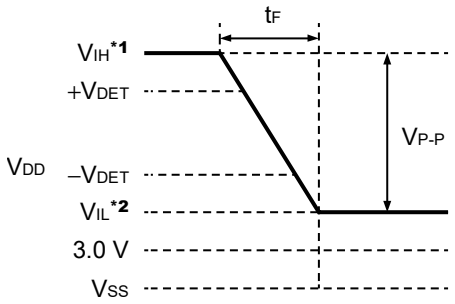


Figure 52 C_N = 100 nF



***1.** V_{IH} = 36.0 V
***2.** $V_{IL} = -V_{DET(S)} - 1.0$ V ($-V_{DET(S)} \geq 4.0$ V)
V_{IL} = 3.0 V ($-V_{DET(S)} < 4.0$ V)

Figure 53 VDD Pin Input Voltage Waveform

Caution Figure 51 and Figure 52 show the input voltage conditions which can maintain the detection delay time accuracy. If the voltage whose V_{P-P} and t_F are larger than these conditions is input to the VDD pin (VDD detection product), the desired detection delay time may not be achieved.

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6. V_{DD} drop during release delay time (reference)

Figure 54 and **Figure 55** show the relation between pulse width (t_{PW}) and V_{DD} lower limit (V_{DROP}) where a release signal can be output after the normal release delay time has elapsed when the VDD pin (VDD detection product) instantaneously drops to the detection voltage ($-V_{DET}$) or lower and then increases to the release voltage ($+V_{DET}$) or higher during release delay time.

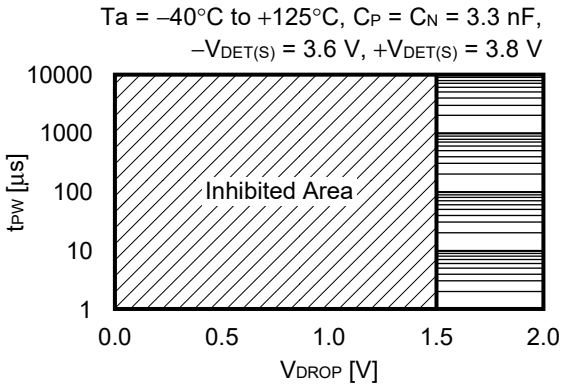


Figure 54

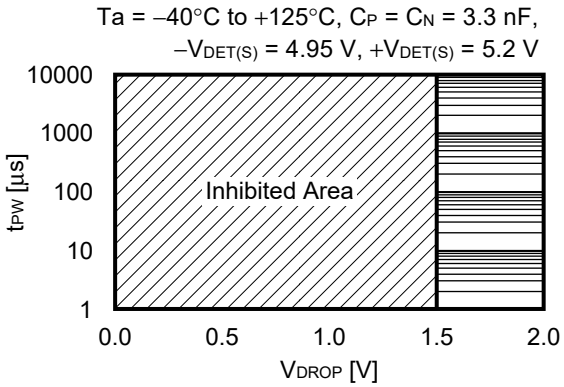
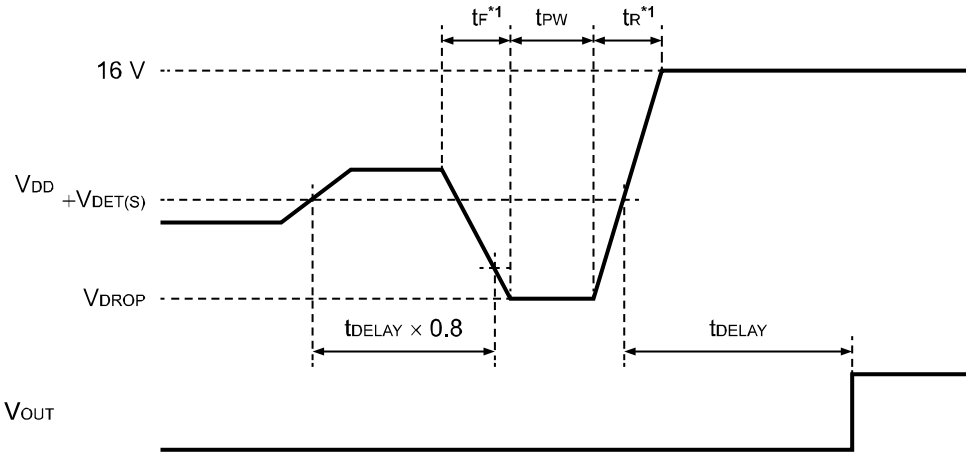


Figure 55



***1.** $t_R = t_F$ = 10 µs

Figure 56 VDD Pin Input Voltage Waveform

Caution 1. Figure 54 and Figure 55 show the input voltage conditions when a release signal is output after the normal release delay time has elapsed. When this is within the inhibited area, release may erroneously be executed before the delay time completes.

2. When the VDD pin voltage is within the inhibited areas shown in Figure 54 and Figure 55 during release delay time, input 0 V to the VDD pin then restart the S-19110 Series.

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■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise.
  Be careful of wiring adjoining SENSE pin wiring in actual applications.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

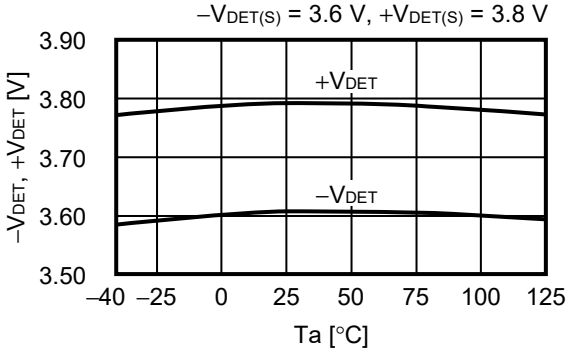
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■ Characteristics (Typical Data)

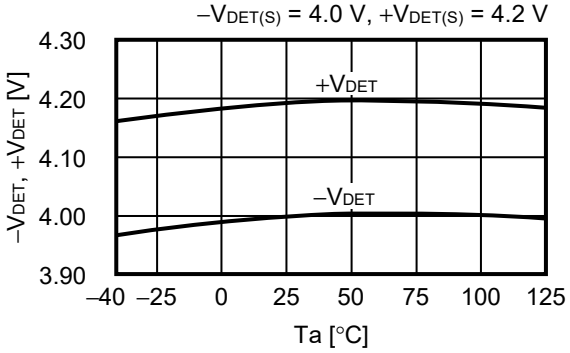
1. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (Ta)

1. 1 VDD detection product

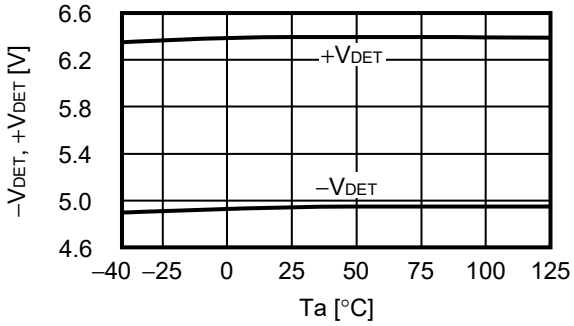
$-V_{DET(S)}$ = 3.6 V, $+V_{DET(S)}$ = 3.8 V



$-V_{DET(S)}$ = 4.0 V, $+V_{DET(S)}$ = 4.2 V

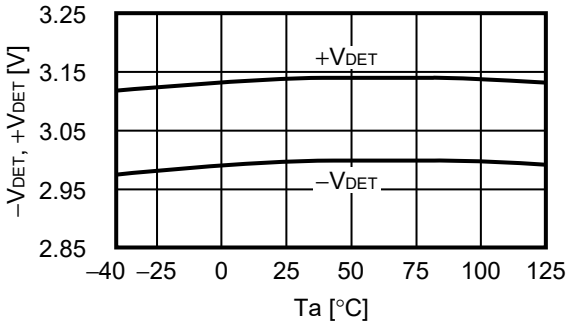


$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V

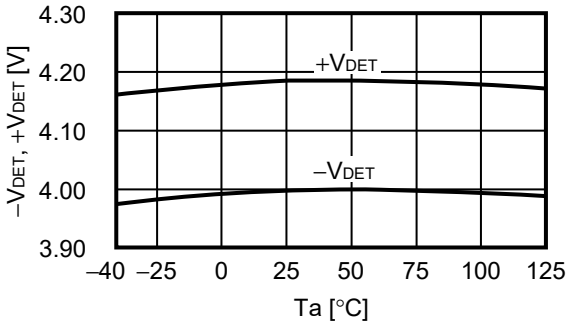


1. 2 SENSE detection product

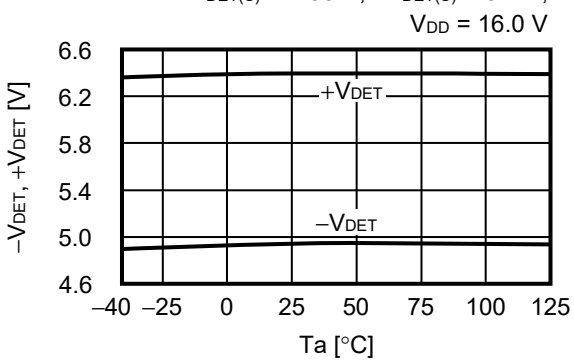
$-V_{DET(S)}$ = 3.0 V, $+V_{DET(S)}$ = 3.15 V, V_{DD} = 16.0 V



$-V_{DET(S)}$ = 4.0 V, $+V_{DET(S)}$ = 4.2 V, V_{DD} = 16.0 V



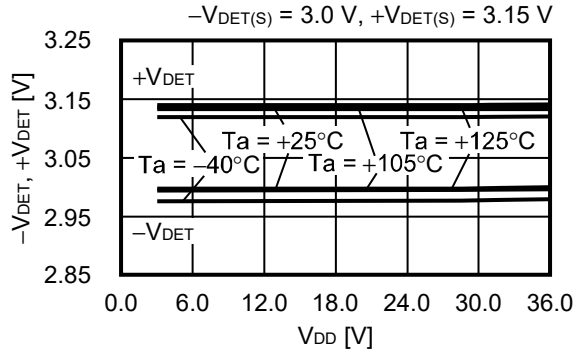
$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V, V_{DD} = 16.0 V

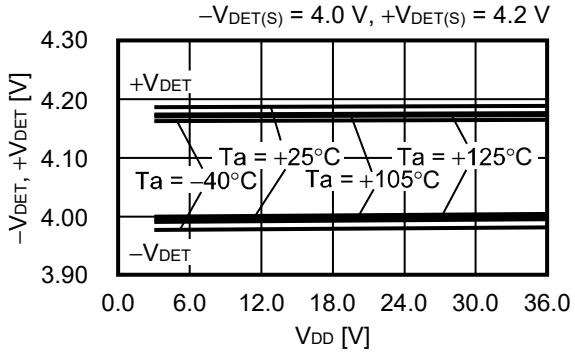


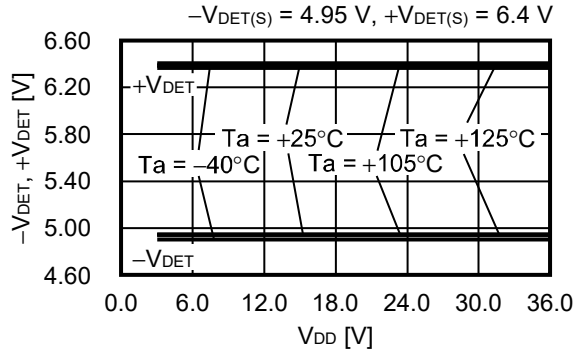
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2. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Power supply voltage (V_{DD})

2. 1 SENSE detection product





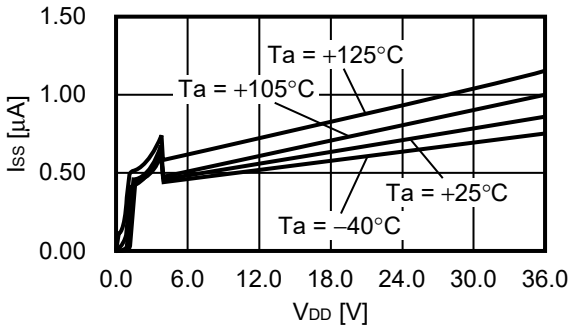


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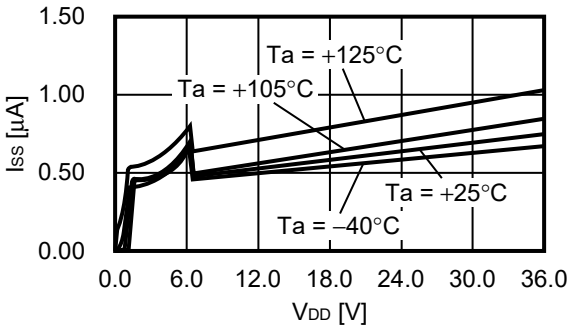
3. Current consumption (I_{SS}) vs. Power supply voltage (V_{DD})

3. 1 VDD detection product

$-V_{DET(S)}$ = 3.6 V, $+V_{DET(S)}$ = 3.8 V,
V_{DD} = 0 V → 36.0 V

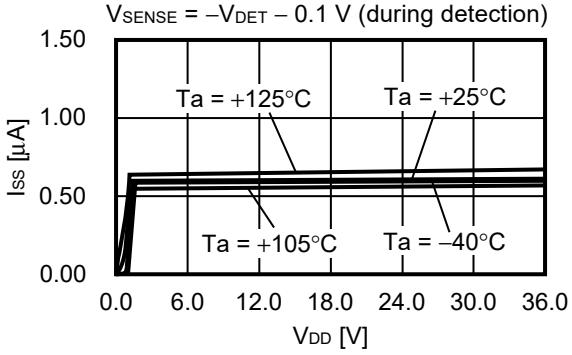


$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{DD} = 0 V → 36.0 V

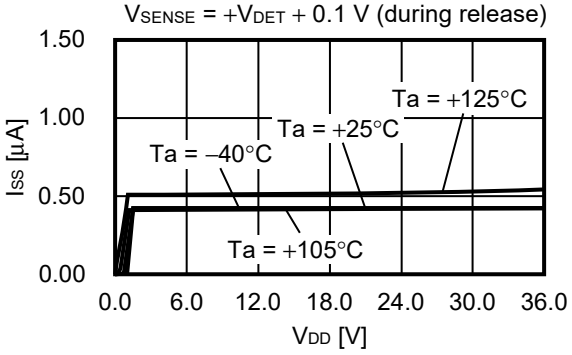


3. 2 SENSE detection product

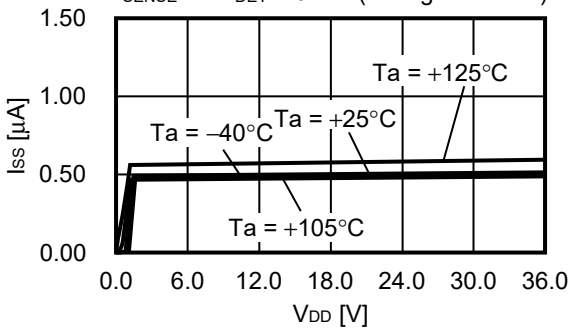
$-V_{DET(S)}$ = 3.0 V, $+V_{DET(S)}$ = 3.15 V,
V_{DD} = 0 V → 36.0 V,
V_{SENSE} = $-V_{DET}$ – 0.1 V (during detection)



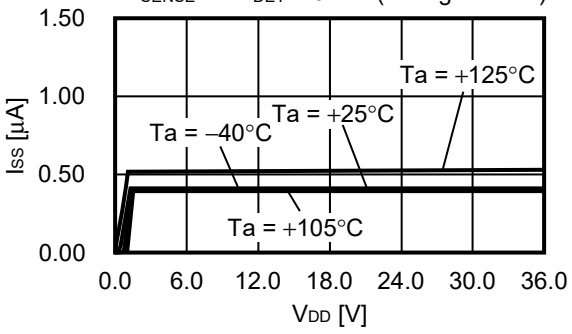
$-V_{DET(S)}$ = 3.0 V, $+V_{DET(S)}$ = 3.15 V,
V_{DD} = 0 V → 36.0 V,
V_{SENSE} = $+V_{DET}$ + 0.1 V (during release)



$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{DD} = 0 V → 36.0 V,
V_{SENSE} = $-V_{DET}$ – 0.1 V (during detection)



$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{DD} = 0 V → 36.0 V,
V_{SENSE} = $+V_{DET}$ + 0.1 V (during release)

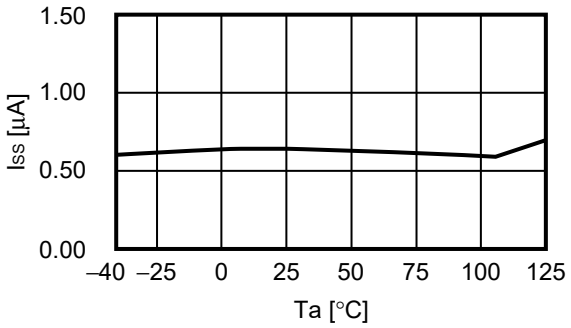


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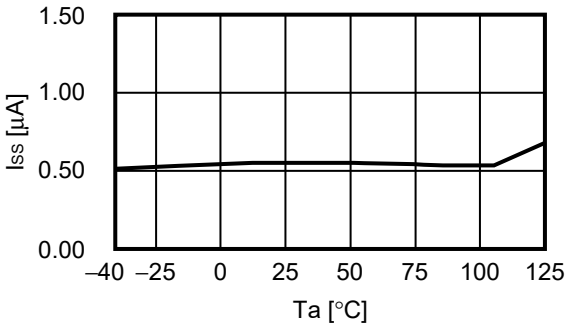
4. Current consumption (I_{SS}) vs. Temperature (Ta)

4. 1 VDD detection product

$-V_{DET(S)}$ = 3.6 V, $+V_{DET(S)}$ = 3.8 V,
$V_{DD} = -V_{DET} - 0.1$ V

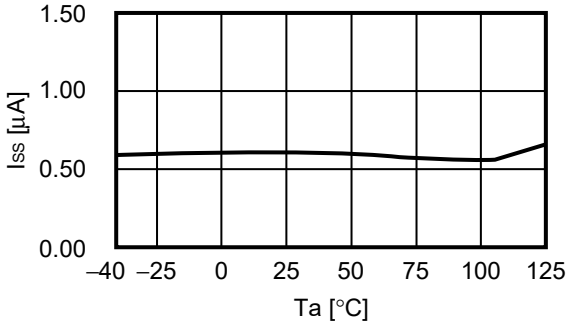


$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
$V_{DD} = -V_{DET} - 0.1$ V

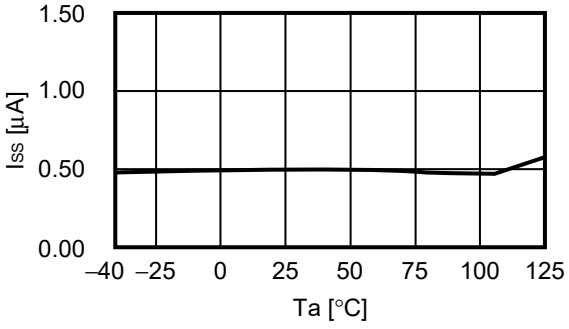


4. 2 SENSE detection product

$-V_{DET(S)}$ = 3.0 V, $+V_{DET(S)}$ = 3.15 V,
V_{DD} = 16.0 V, $V_{SENSE} = -V_{DET} - 0.1$ V



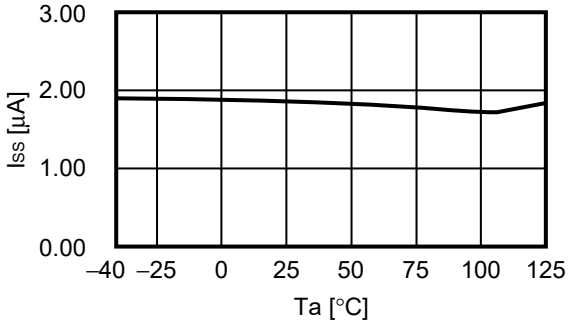
$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{DD} = 16.0 V, $V_{SENSE} = -V_{DET} - 0.1$ V



5. Current consumption during detection delay (I_{SS}) vs. Temperature (Ta)

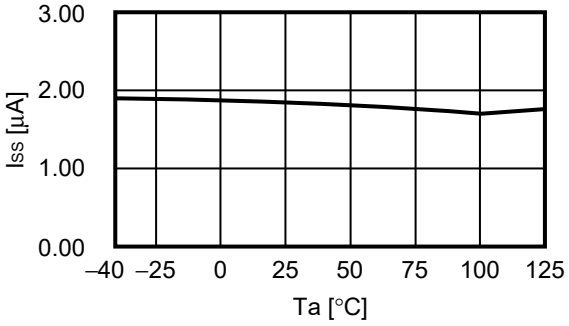
5. 1 VDD detection product

$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{CN} = 0.2 V



5. 2 SENSE detection product

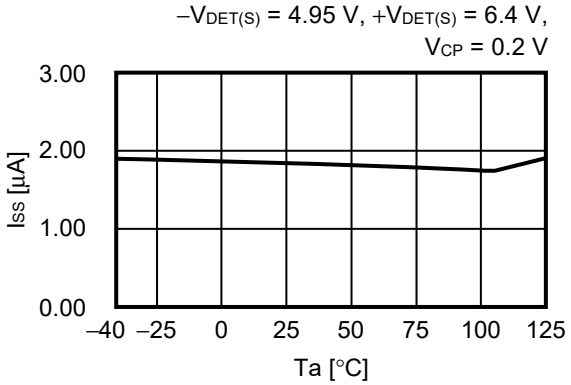
$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{DD} = 16.0 V, V_{CN} = 0.2 V



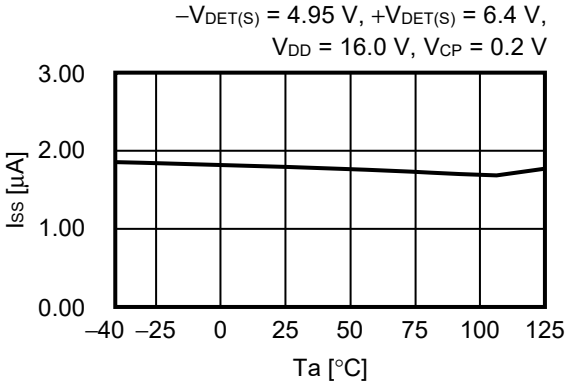
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6. Current consumption during release delay (I_{SS}) vs. Temperature (Ta)

6. 1 VDD detection product

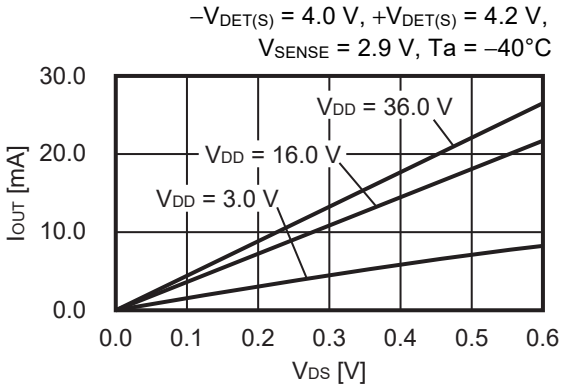


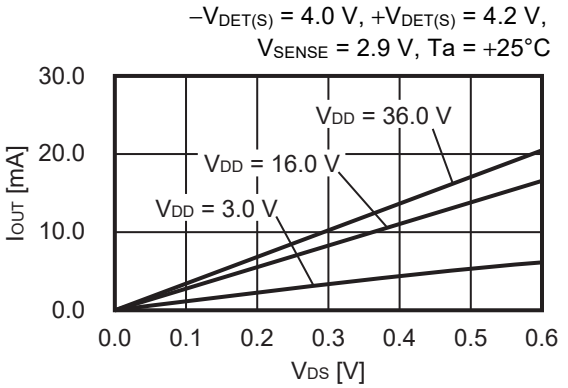
6. 2 SENSE detection product

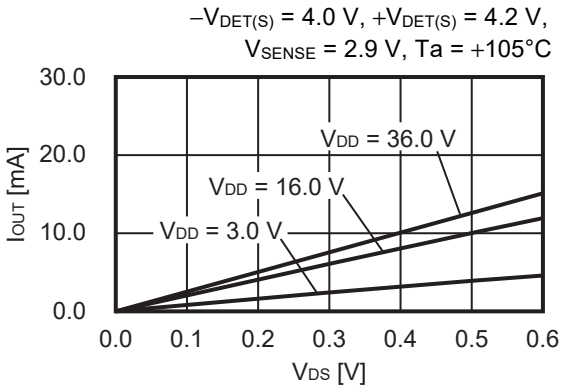


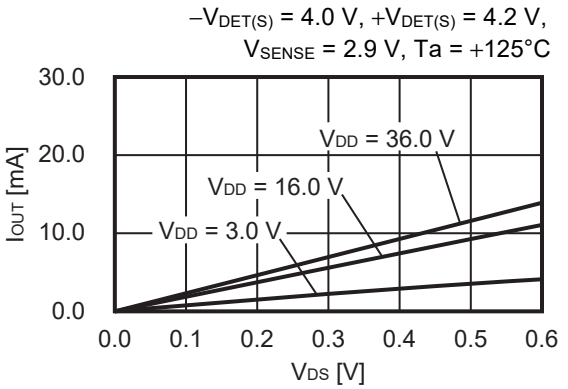
7. Nch transistor output current (I_{OUT}) vs. V_{DS}

7. 1 SENSE detection product









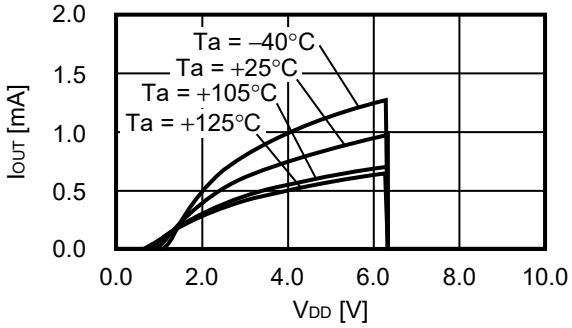
Remark V_{DS}: Drain-to-source voltage of the output transistor

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8. Nch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})

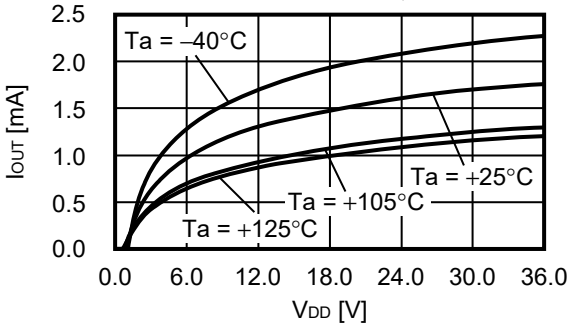
8. 1 VDD detection product

$-V_{DET(S)}$ = 4.95 V, $+V_{DET(S)}$ = 6.4 V,
V_{DS} = 0.05 V



8. 2 SENSE detection product

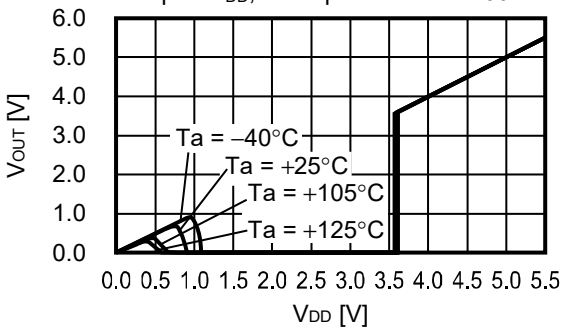
$-V_{DET(S)}$ = 4.0 V, $+V_{DET(S)}$ = 4.2 V,
V_{SENSE} = 2.9 V, V_{DS} = 0.05 V



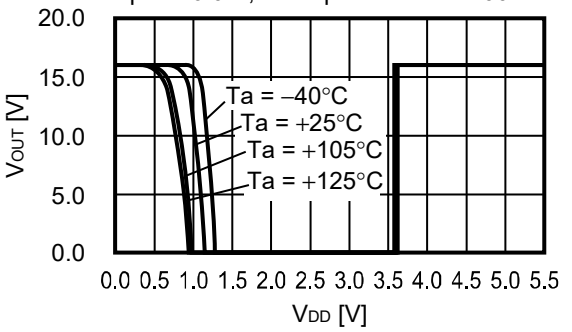
9. Minimum operation voltage (V_{OUT}) vs. Power supply voltage (V_{DD})

9. 1 VDD detection product

$-V_{DET(S)}$ = 3.6 V, $+V_{DET(S)}$ = 3.8 V,
Pull-up to V_{DD}, Pull-up resistance: 100 kΩ

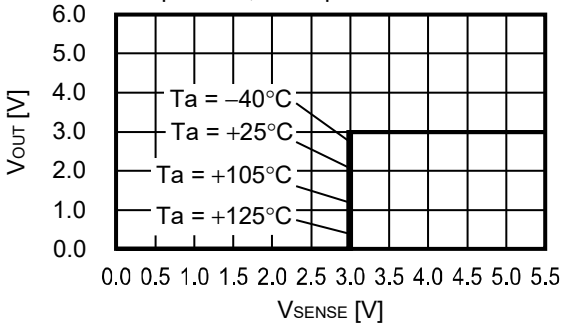


$-V_{DET(S)}$ = 3.6 V, $+V_{DET(S)}$ = 3.8 V,
Pull-up to 16.0 V, Pull-up resistance: 100 kΩ

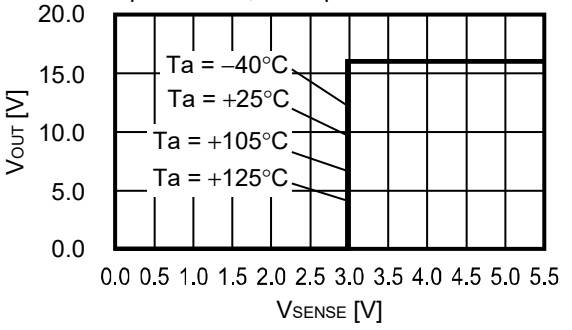


9. 2 SENSE detection product

$-V_{DET(S)}$ = 3.0 V, $+V_{DET(S)}$ = 3.15 V, V_{DD} = 3.0 V,
Pull-up to V_{DD}, Pull-up resistance: 100 kΩ



$-V_{DET(S)}$ = 3.0 V, $+V_{DET(S)}$ = 3.15 V, V_{DD} = 3.0 V,
Pull-up to 16.0 V, Pull-up resistance: 100 kΩ

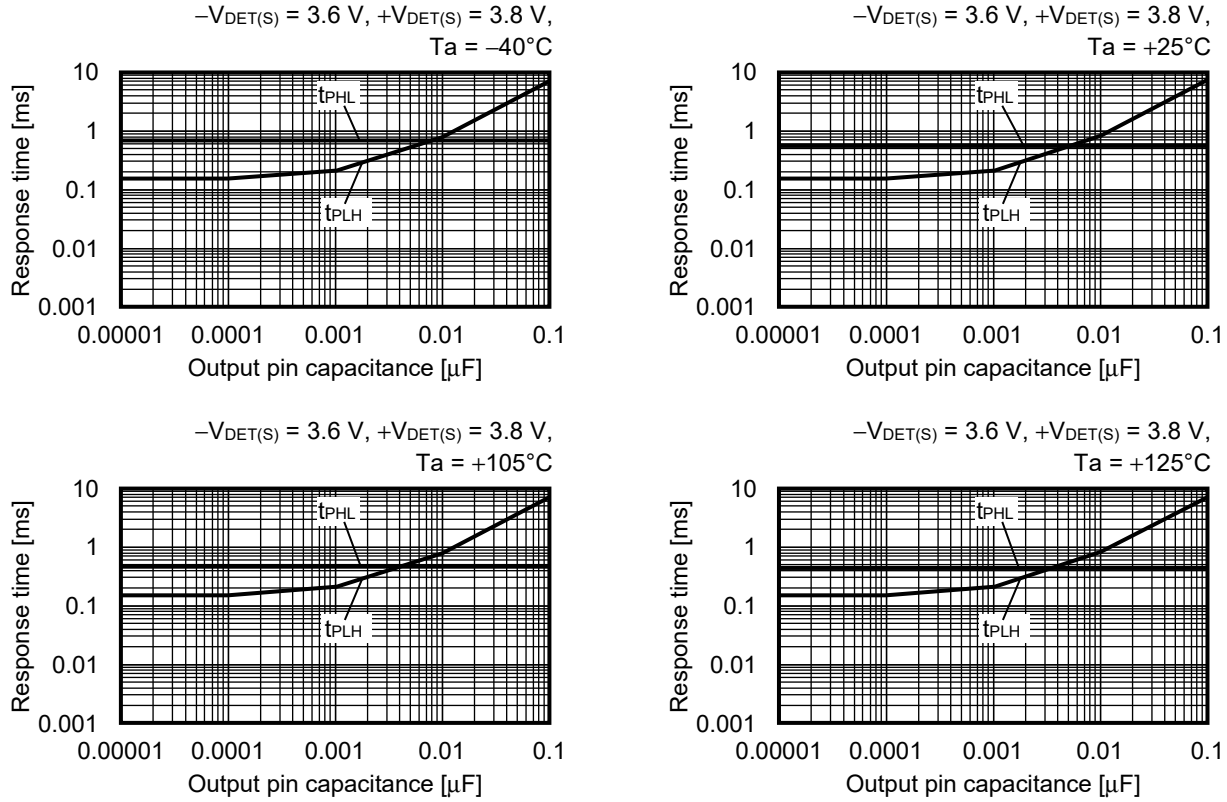


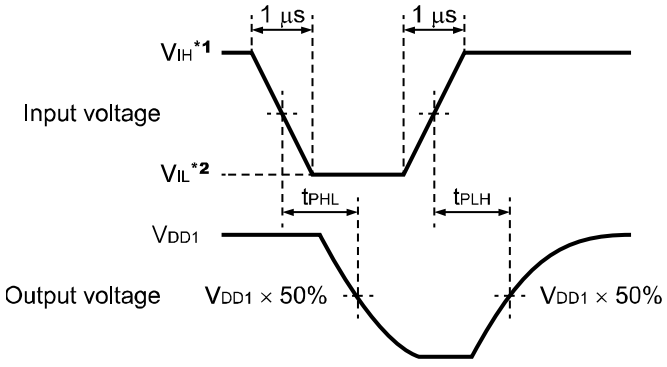
Remark V_{DS}: Drain-to-source voltage of the output transistor

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10. Dynamic response vs. Output pin capacitance (C_{OUT}) (CP pin, CN pin; open)

10. 1 VDD detection product





*1. V_{IH} = 36.0 V
*2. V_{IL} = 3.0 V

Figure 57 Test Condition of Response Time

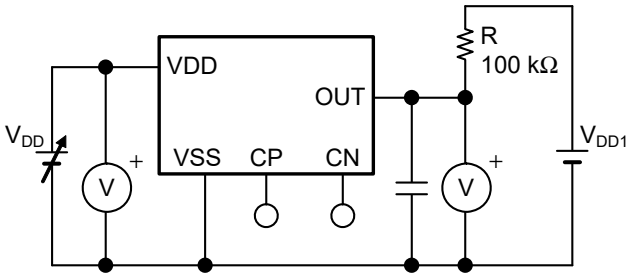


Figure 58 Test Circuit of Response Time

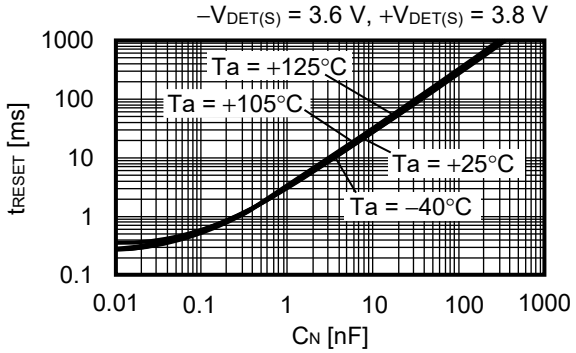
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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■ Reference Data

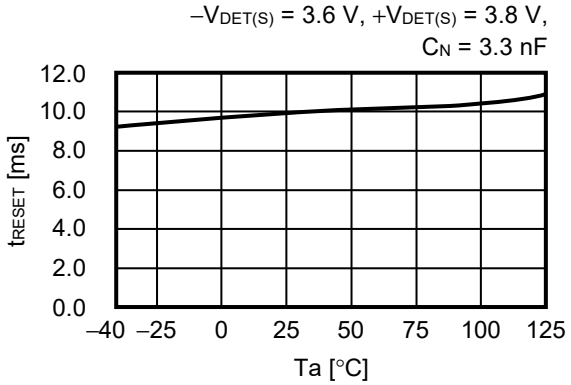
1. Detection delay time (t_{RESET}) vs. CN pin capacitance (C_N) (Without output pin capacitance)

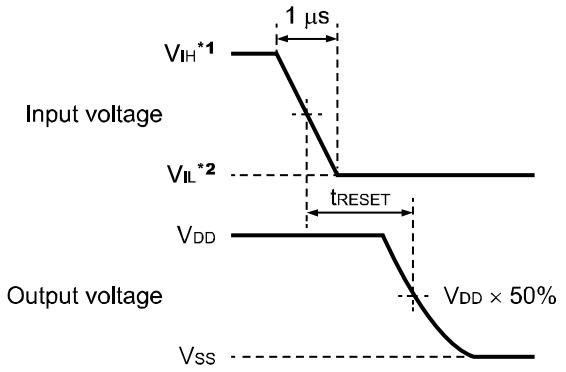
1. 1 VDD detection product



2. Detection delay time (t_{RESET}) vs. Temperature (Ta)

2. 1 VDD detection product





*1. $V_{IH} = -V_{DET(S)} + 0.5$ V
*2. $V_{IL} = -V_{DET(S)} - 0.5$ V

Figure 59 Test Condition of Detection Delay Time

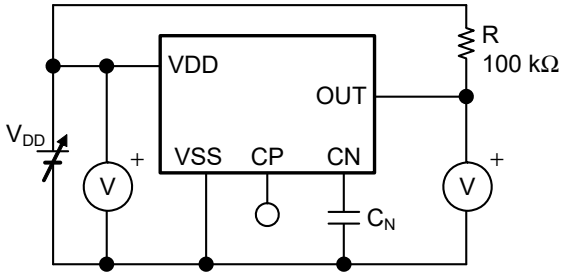


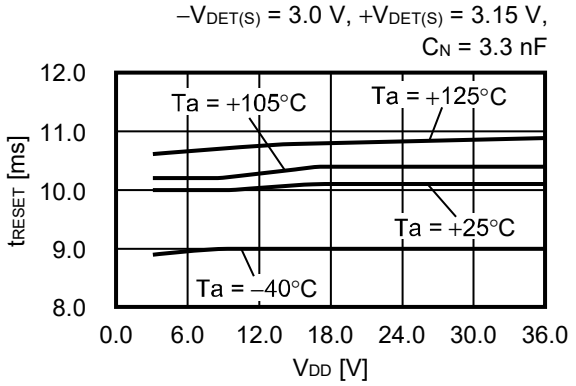
Figure 60 Test Circuit of Detection Delay Time

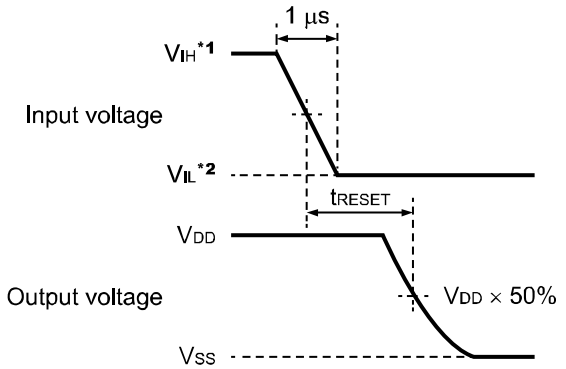
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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3. Detection delay time (t_{RESET}) vs. Power supply voltage (V_{DD})

3. 1 SENSE detection product





***1.** $V_{IH} = -V_{DET(S)} + 0.5$ V

***2.** $V_{IL} = -V_{DET(S)} - 0.5$ V

Figure 61 Test Condition of Detection Delay Time

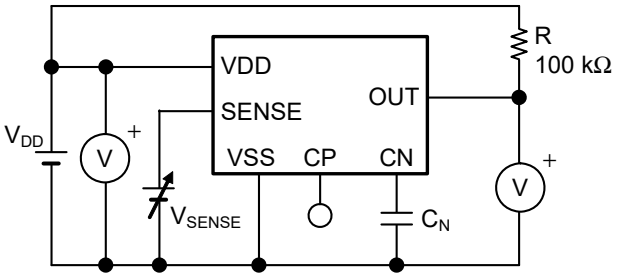


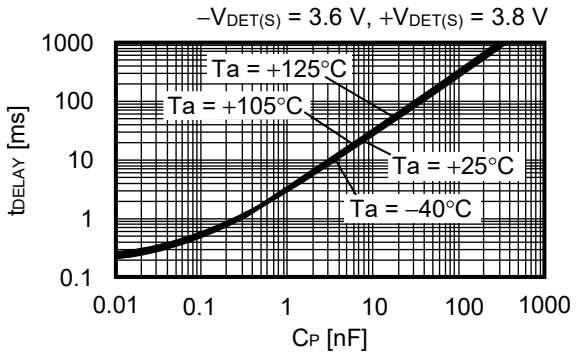
Figure 62 Test Circuit of Detection Delay Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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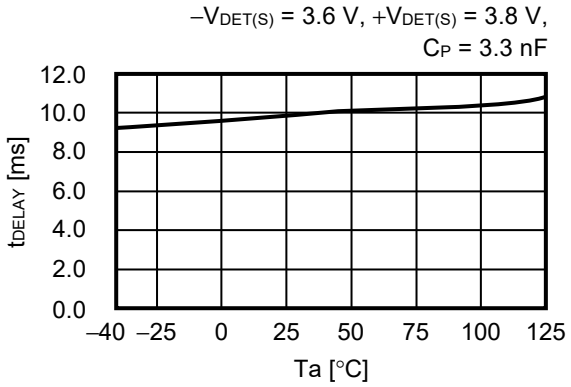
4. Release delay time (t_{DELAY}) vs. CP pin capacitance (C_P) (Without output pin capacitance)

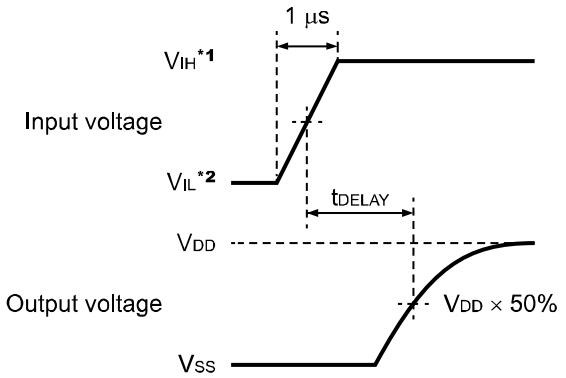
4. 1 VDD detection product



5. Release delay time (t_{DELAY}) vs. Temperature (Ta)

5. 1 VDD detection product





*1. $V_{IH} = +V_{DET(S)} + 0.5$ V
*2. $V_{IL} = +V_{DET(S)} - 0.5$ V

Figure 63 Test Condition of Release Delay Time

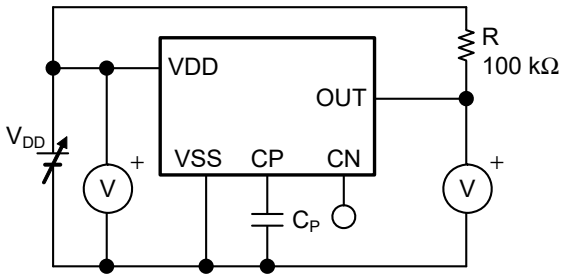


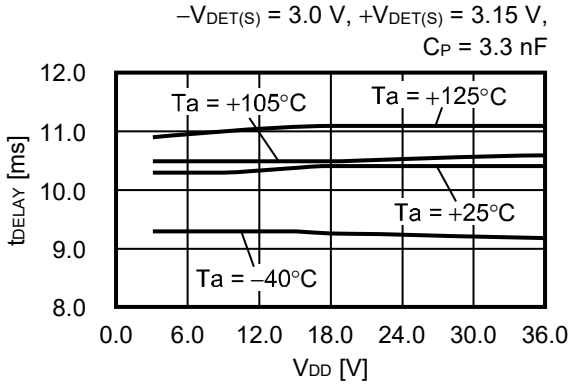
Figure 64 Test Circuit of Release Delay Time

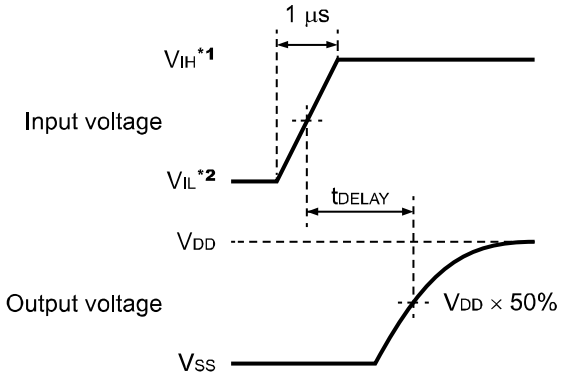
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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6. Release delay time (t_{DELAY}) vs. Power supply voltage (V_{DD})

6. 1 SENSE detection product





*1. $V_{IH} = +V_{DET(S)} + 0.5$ V
*2. $V_{IL} = +V_{DET(S)} - 0.5$ V

Figure 65 Test Condition of Release Delay Time

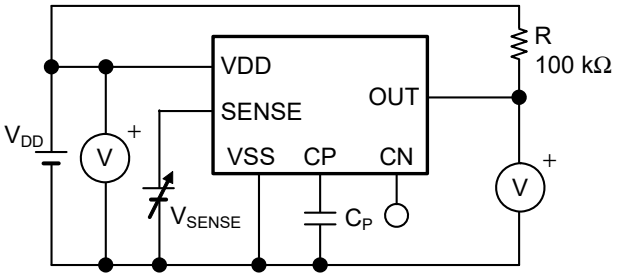
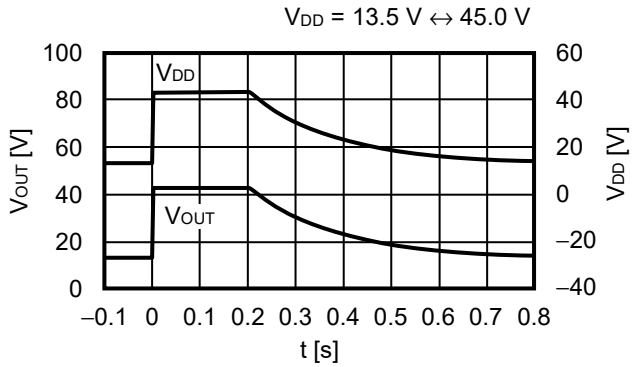


Figure 66 Test Circuit of Release Delay Time

7. Load dump characteristics (Ta = +25°C)

7. 1 VDD detection, active "L" product



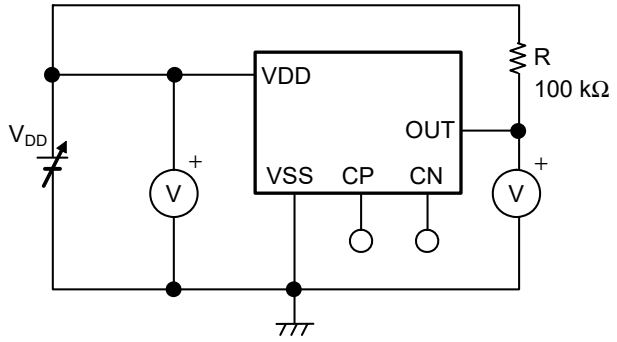


Figure 67 Test Circuit of Load Dump Characteristics

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.
Using the S-19110 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in **Figure 68** and **Figure 69**.

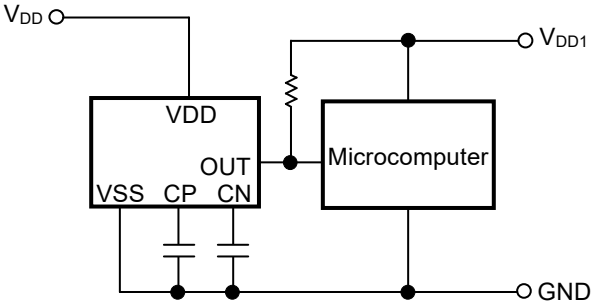


Figure 68 Example of Reset Circuit (VDD Detection Product)

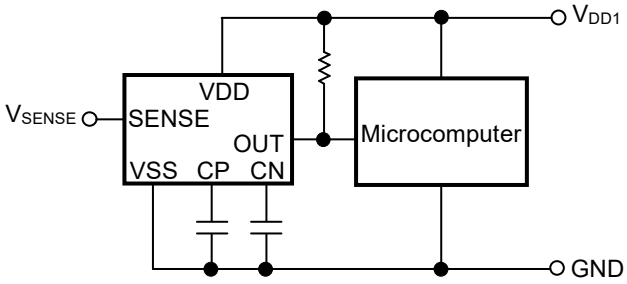


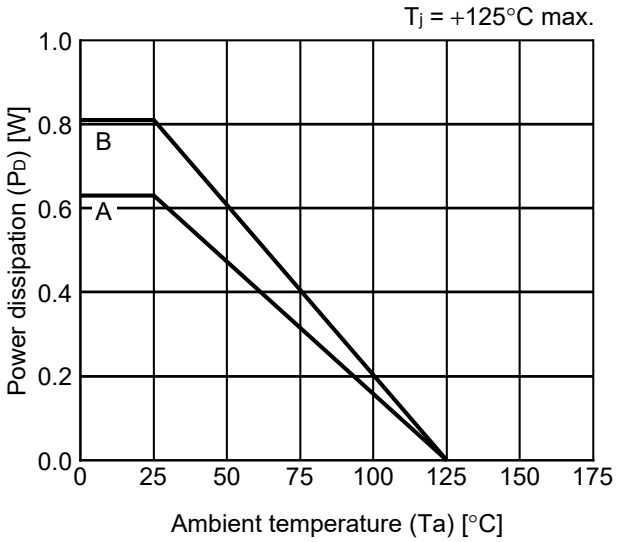
Figure 69 Example of Reset Circuit (SENSE Detection Product)

**Caution The above connection diagrams will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constants.**

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Power Dissipation

SOT-23-6



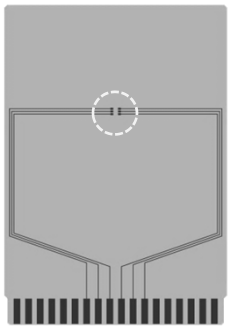
Board	Power Dissipation (P_D)
A	0.63 W
B	0.81 W
C	–
D	–
E	–

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SOT-23-3/3S/5/6 Test Board

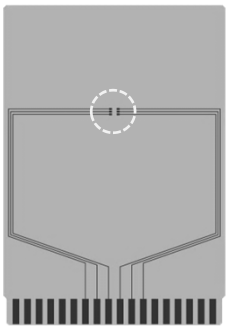
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

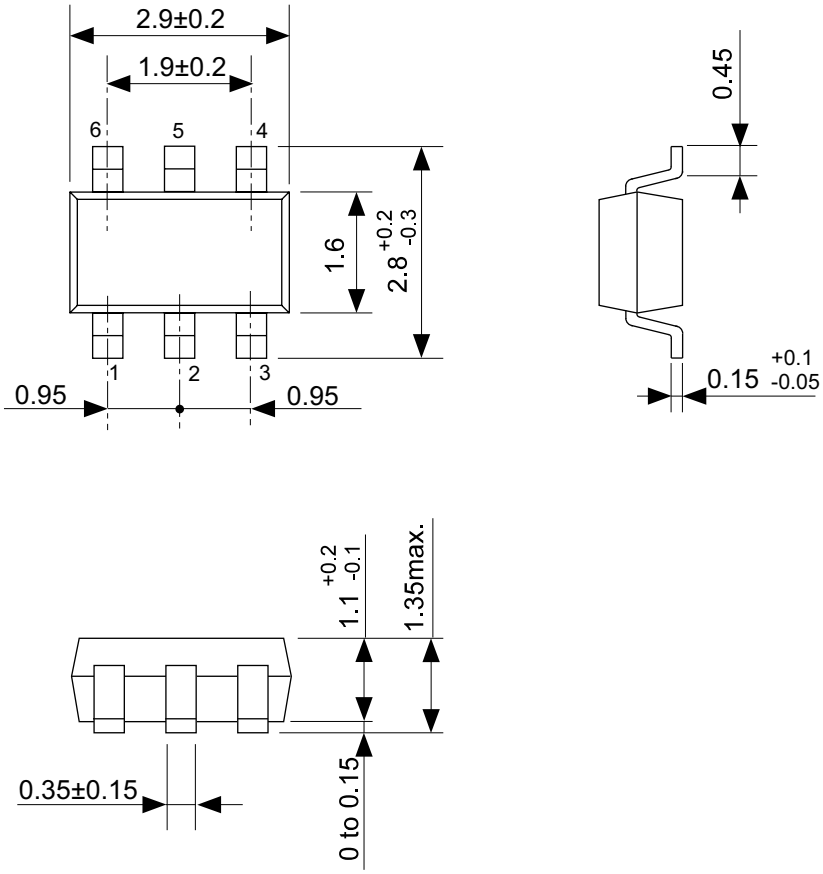
(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

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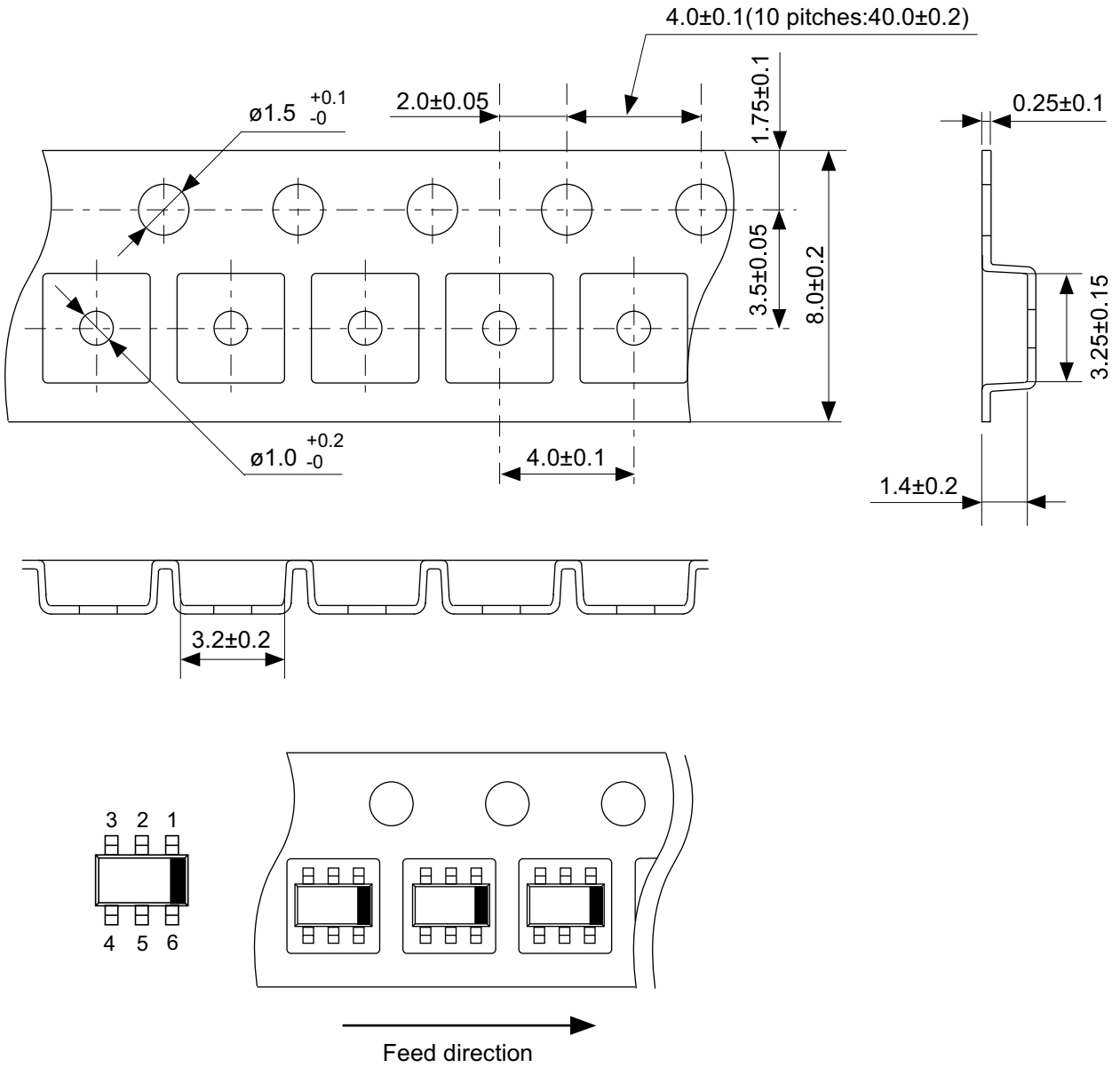


No. MP006-A-P-SD-2.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

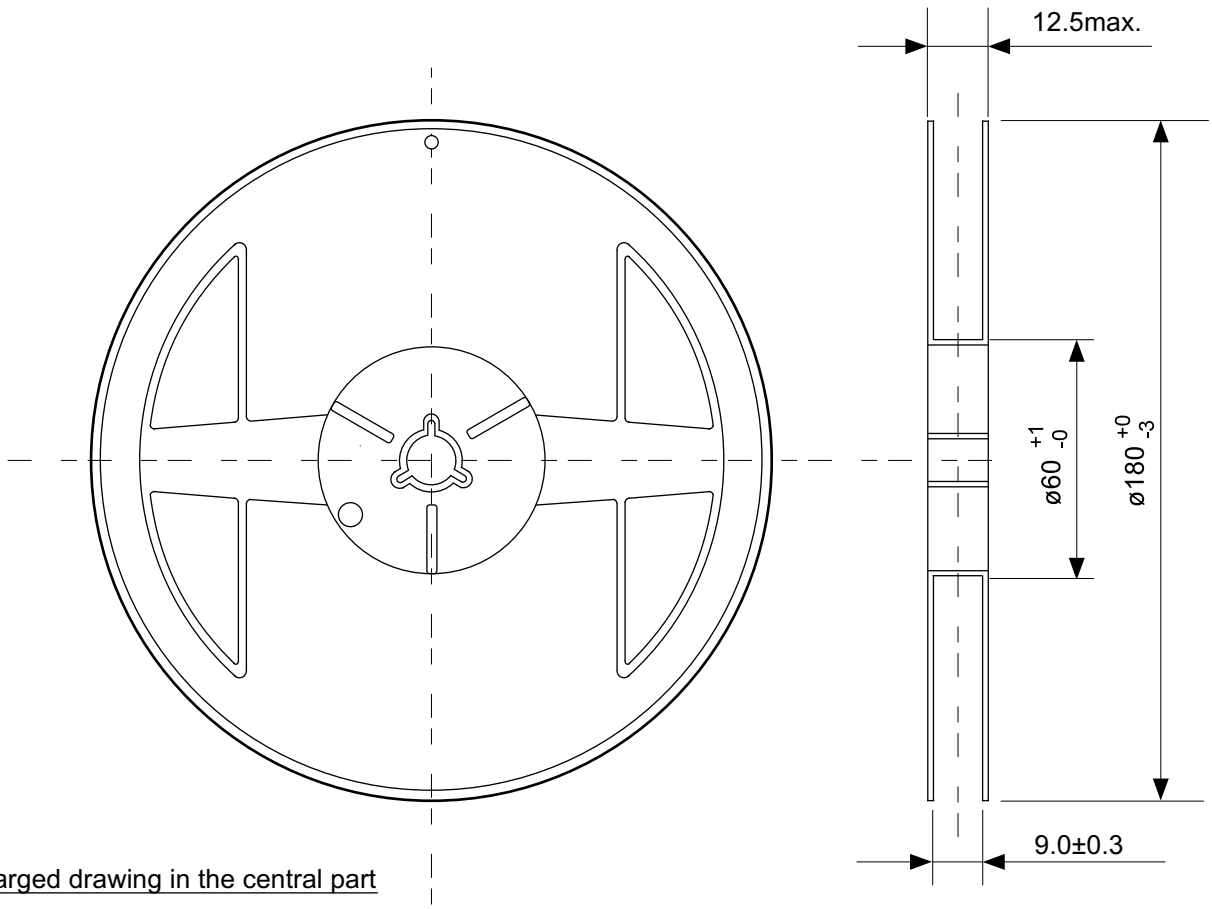
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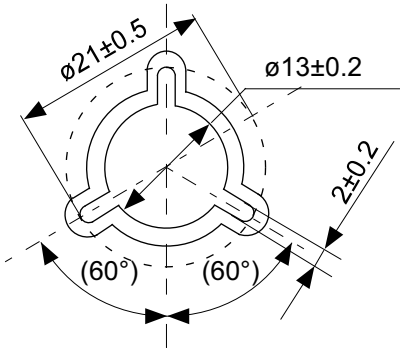
No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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Enlarged drawing in the central part



No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			

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