Ordering number : EN7177B

CPH5905

N-Channel JFET and NPN Bipolar Transistor
15V, 10 to 32mA, 50V, 150mA, Composite type, CPH5

ON Semiconductor®
http://onsemi.com

Features

- Composite type with J-FET and NPN transistors contained in the CPH5 package, improving the mounting efficiency greatly
- The CPH5905 contains a 2SK3357-equivalent chip and a 2SC4639-equivalent chip in one package
- Drain and emitter are shared

Specifications

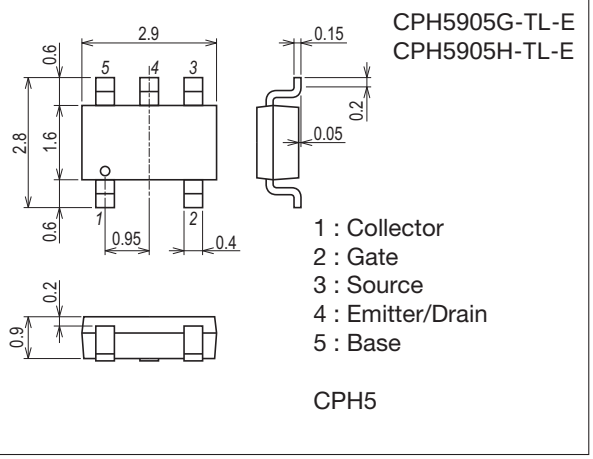
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
[FET]				
Drain-to-Source Voltage	V_{DSX}		15	V
Gate-to-Drain Voltage	V_{GDS}		−15	V
Gate Current	I_G		10	mA
Drain Current	I_D		50	mA
Allowable Power Dissipation	P_D	Mounted on a ceramic board (600mm²×0.8mm)	350	mW
[TR]				
Collector-to-Base Voltage	V_{CBO}		55	V
Collector-to-Emitter Voltage	V_{CEO}		50	V
Emitter-to-Base Voltage	V_{EBO}		6	V
Collector Current	I_C		150	mA
Collector Current (Pulse)	I_{CP}		300	mA
Base Current	I_B		30	mA
Collector Dissipation	P_C	Mounted on a ceramic board (600mm²×0.8mm)	350	mW
[TR]				
Total Power Dissipation	P_T	Mounted on a ceramic board (600mm²×0.8mm)	500	mW
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

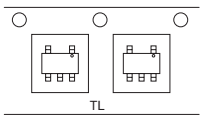
unit : mm (typ)
7017A-007



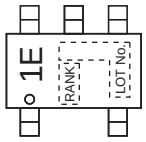
Product & Package Information

- Package : CPH5
- JEITA, JEDEC : SC-74A, SOT-25
- Minimum Packing Quantity : 3,000 pcs./reel

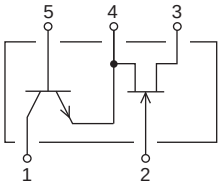
Packing Type : TL



Marking



Electrical Connection



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Electrical Characteristics at Ta=25°C

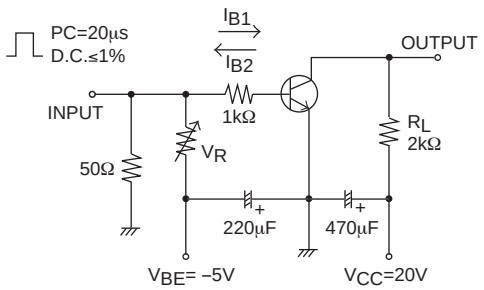
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FET]						
Gate-to-Drain Breakdown Voltage	$V_{(BR)GDS}$	I_G=−10μA, V_{GS}=0V	−15			V
Gate Cutoff Current	I_{GSS}	V_{GS}=−10V, V_{DS}=0V			−1.0	nA
Cutoff Voltage	V_{GS}(off)	V_{DS}=5V, I_D=100μA	−0.4	−0.7	−1.5	V
Drain Current	I_{DSS}	V_{DS}=5V, V_{GS}=0V	10.0*		32.0*	mA
Forward Transfer Admittance	| yfs |	V_{DS}=5V, V_{GS}=0V, f=1kHz	24	35		mS
Input Capacitance	Ciss	V_{DS}=5V, V_{GS}=0V, f=1kHz		10.0		pF
Reverse Transfer Capacitance	Crss	V_{DS}=5V, V_{GS}=0V, f=1kHzz		2.9		pF
Noise Figure	NF	V_{DS}=5V, Rg=1kΩ, I_D=1mA, f=1kHz		1.0		dB
[TR]						
Collector Cutoff Current	I_{CBO}	V_{CB}=35V, I_E=0A			0.1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=4V, I_C=0A			0.1	μA
DC Current Gain	h_{FE}	V_{CE}=6V, I_C=1mA	135		400	
Gain-Bandwidth Product	f_T	V_{CE}=6V, I_C=10mA		200		MHz
Output Capacitance	Cob	V_{CB}=6V, f=1MHz		1.7		pF
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=50mA, I_B=5mA		0.08	0.4	mV
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=50mA, I_B=5mA		0.8	1.0	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0A	55			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, R_{BE}=∞	50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0A	6			V
Turn-On Time	t_{on}	See specified Test Circuit.		0.15		ns
Storage Time	t_{stg}			0.75		ns
Fall Time	t_f			0.20		ns

* : The CPH5905 is classified by I_{DSS} as follows : (unit : mA)

Rank	G	H
I_{DSS}	10.0 to 20.0	16.0 to 32.0

The specifications shown above are for each individual FET or transistor.

Switching Time Test Circuit



$10I_{B1}$= −$10I_{B2}$=I_C=10mA

Ordering Information

Device	Package	Shipping	memo
CPH5905G-TL-E	CPH5	3,000pcs./reel	Pb Free
CPH5905H-TL-E	CPH5	3,000pcs./reel	

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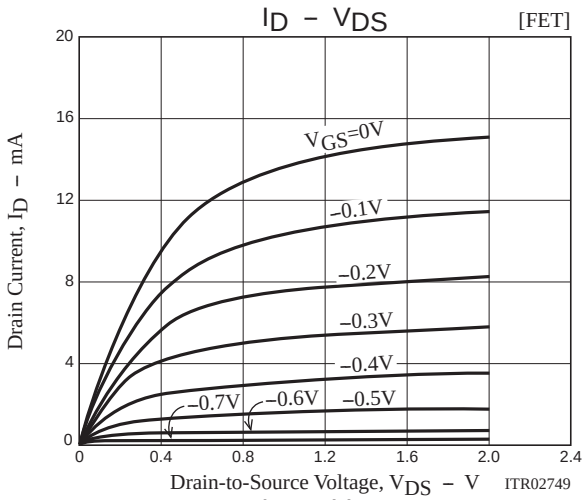

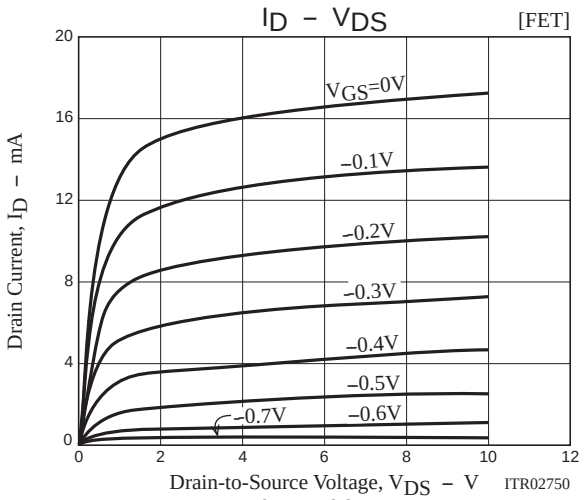

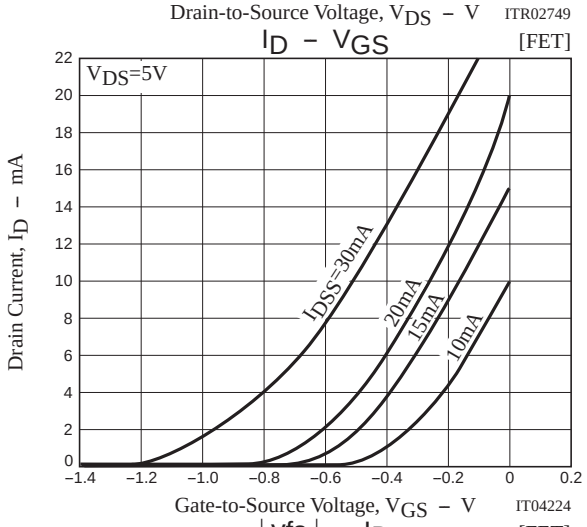

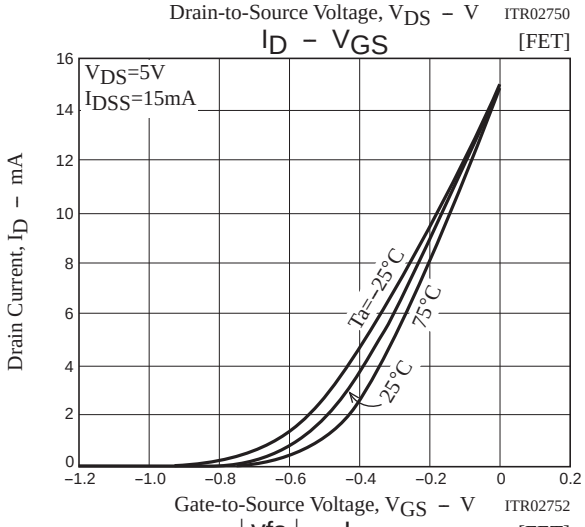

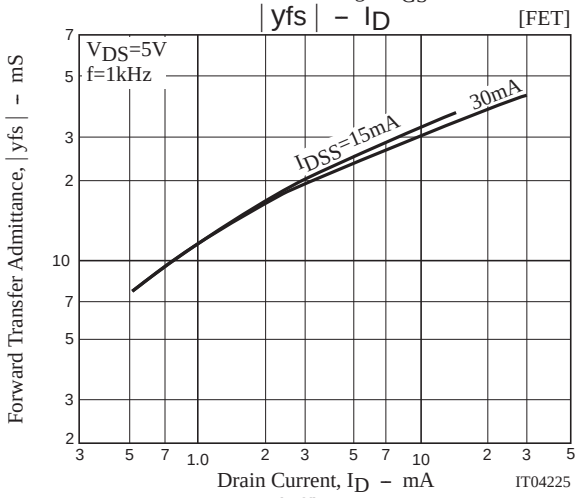

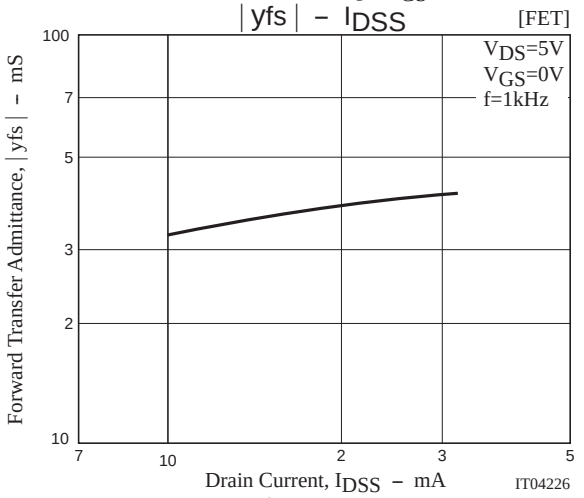

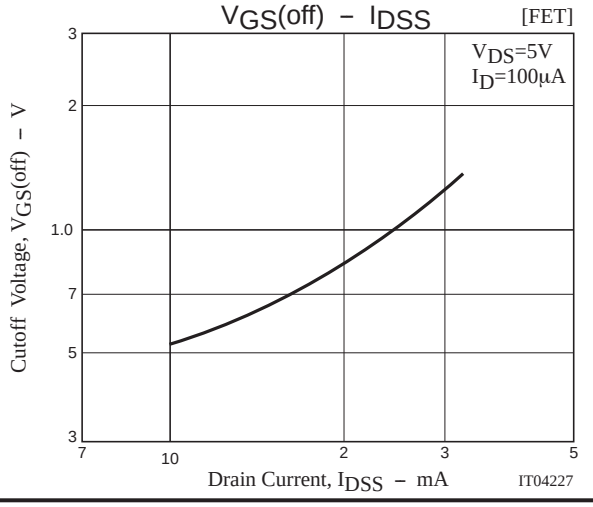

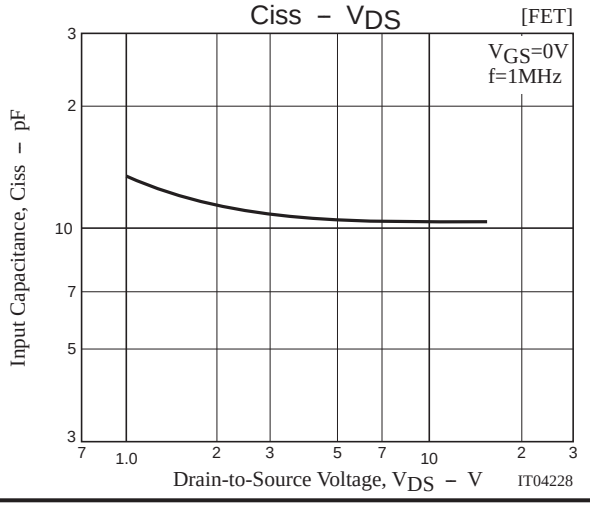

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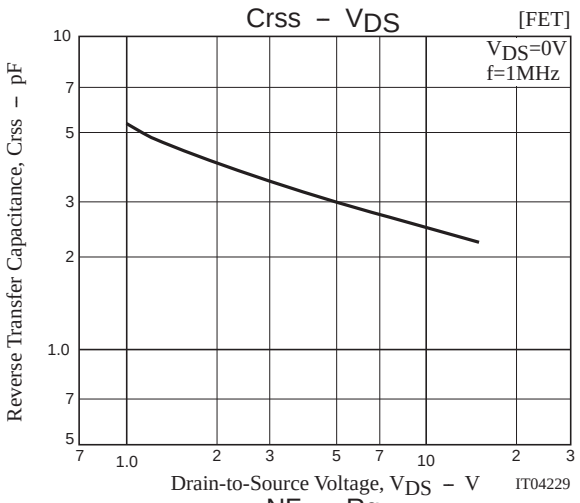

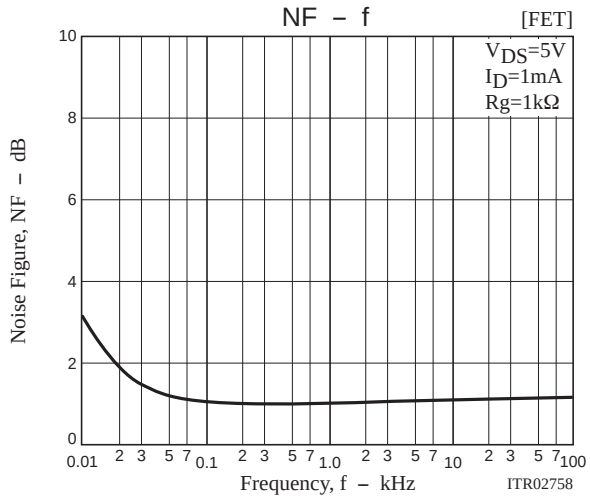

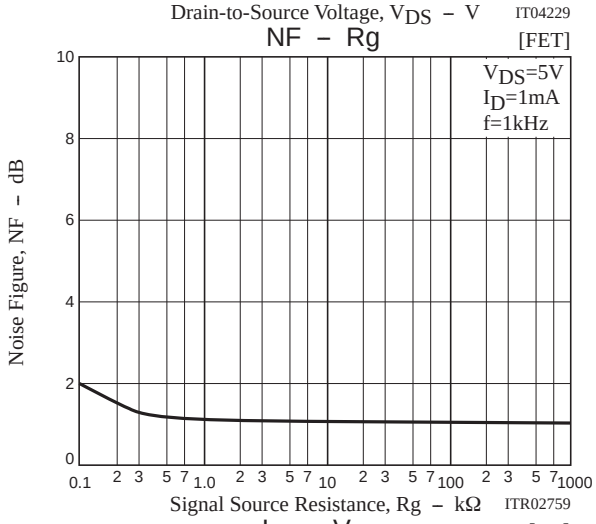

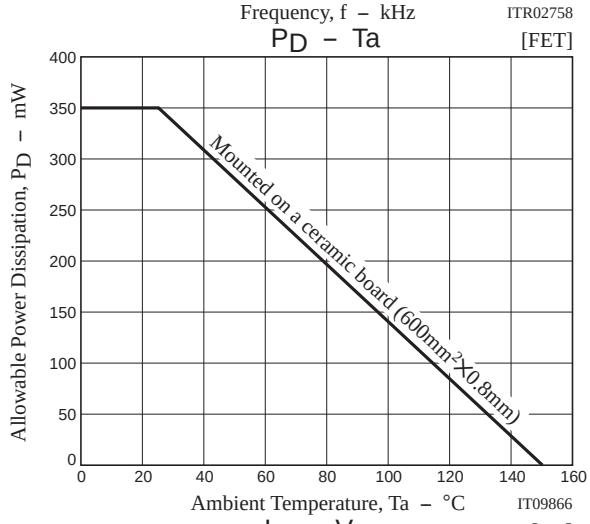

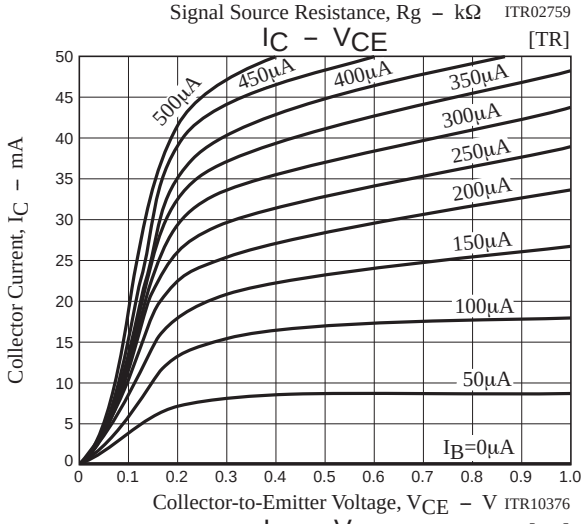

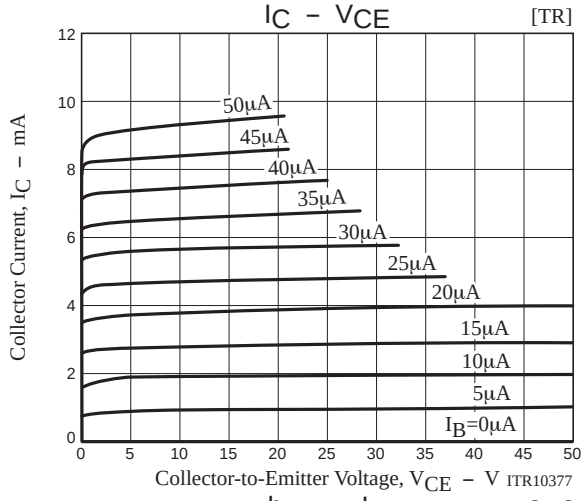

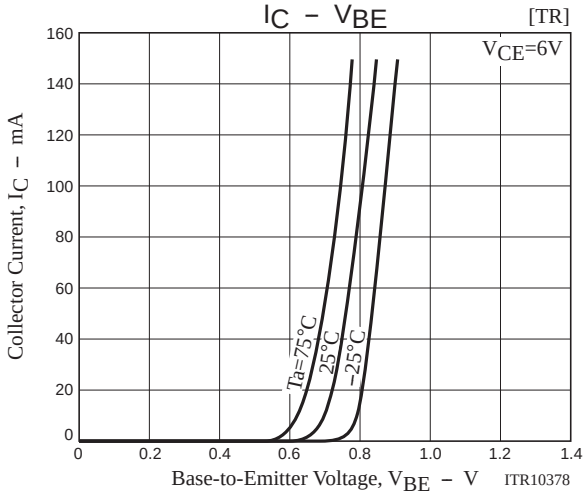

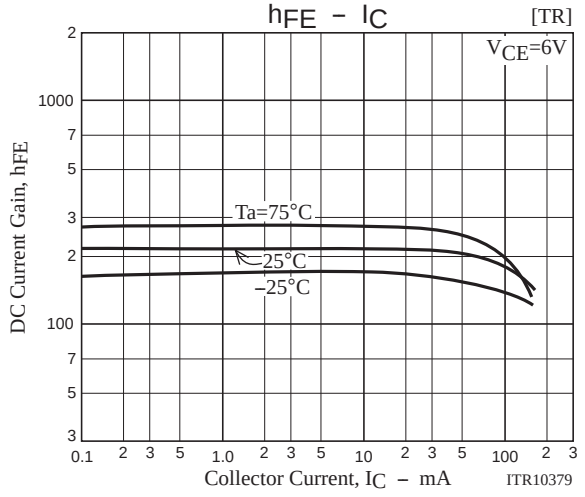

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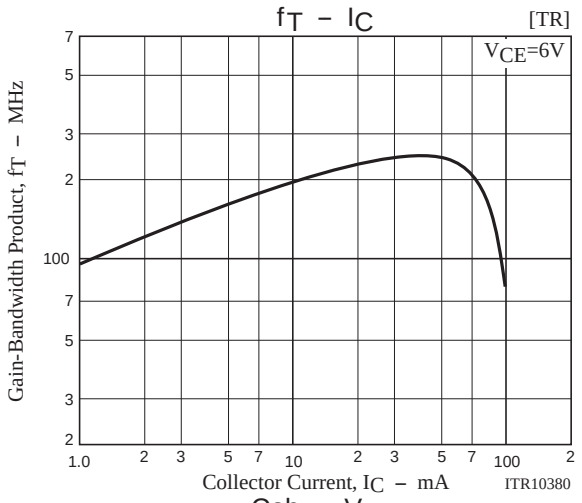

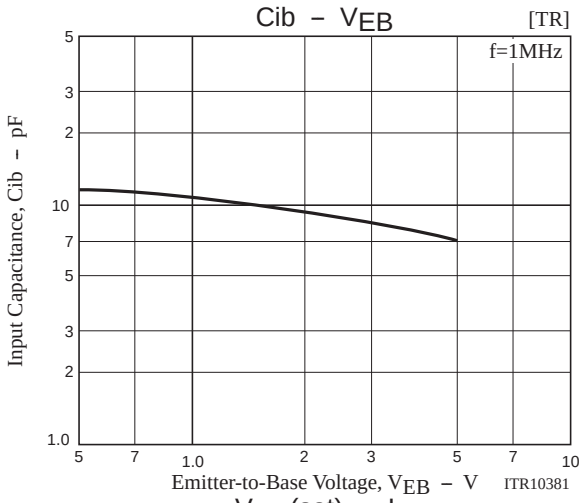

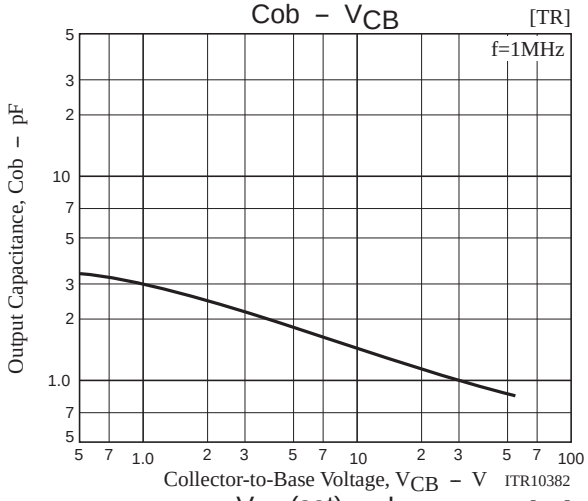

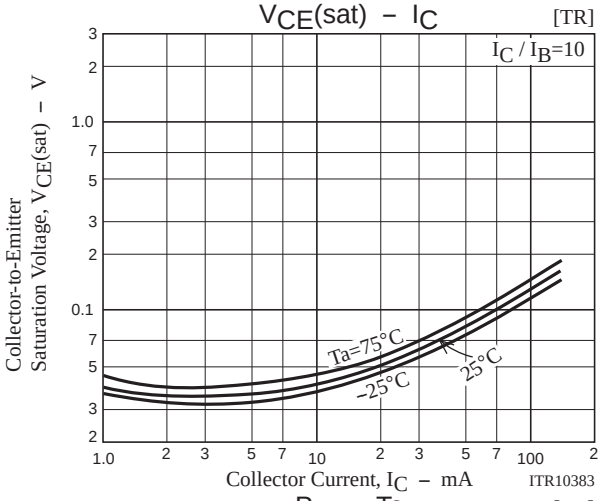

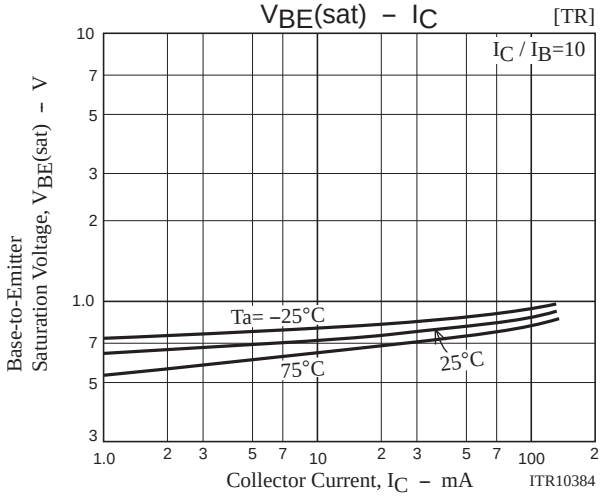

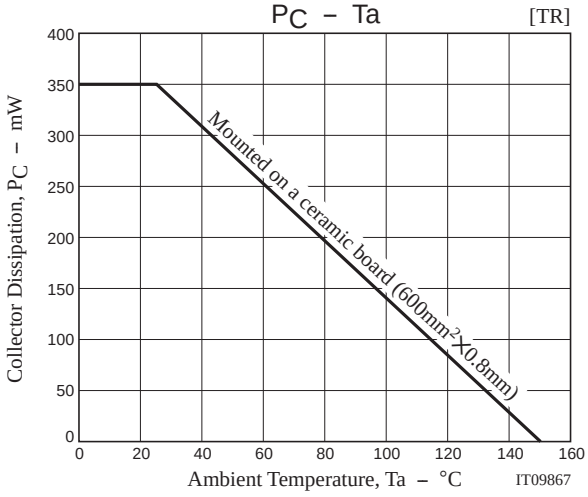

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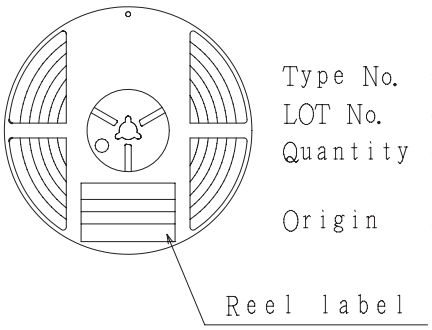
Embossed Taping Specification

CPH5905G-TL-E, CPH5905H-TL-E

1. Packing Format

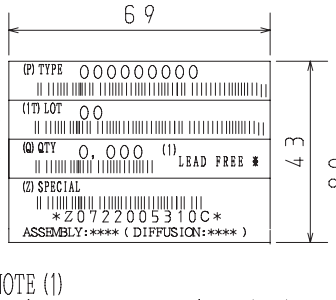
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
CPH5	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Packing method



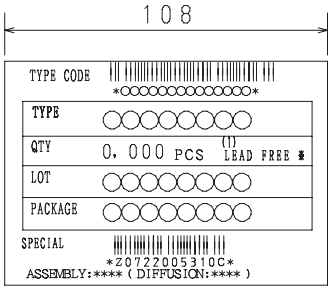
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.

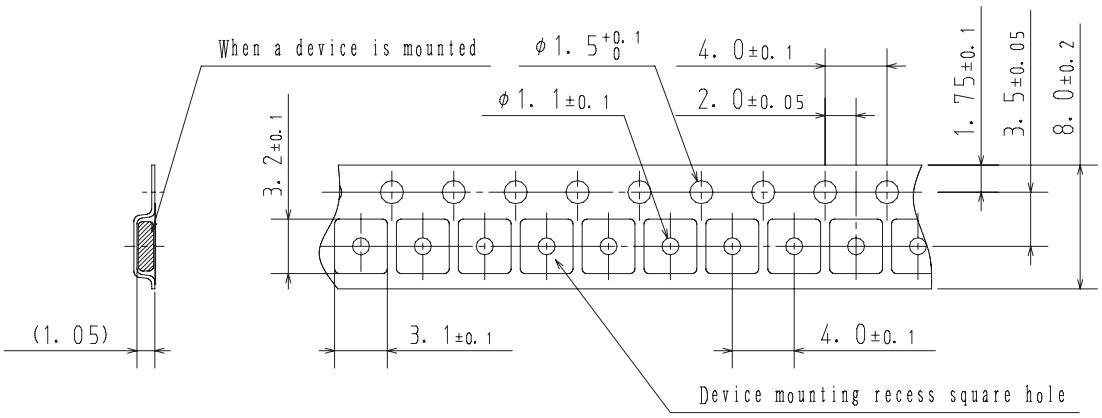


NOTE (1)
The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

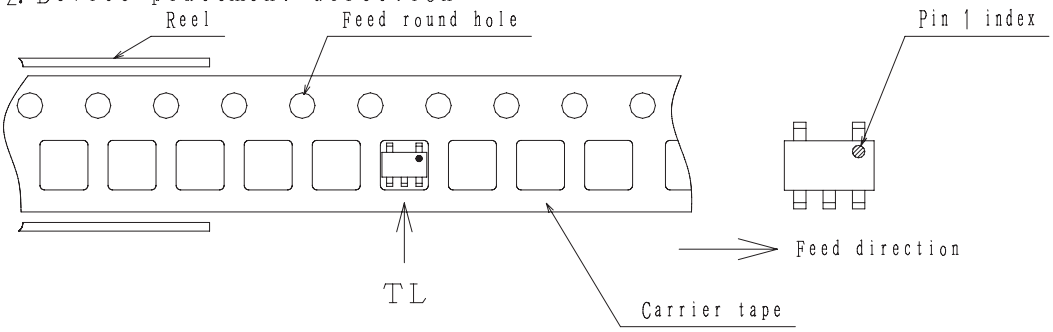
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction



Those with pin 1 index on the feed hole side·····TL

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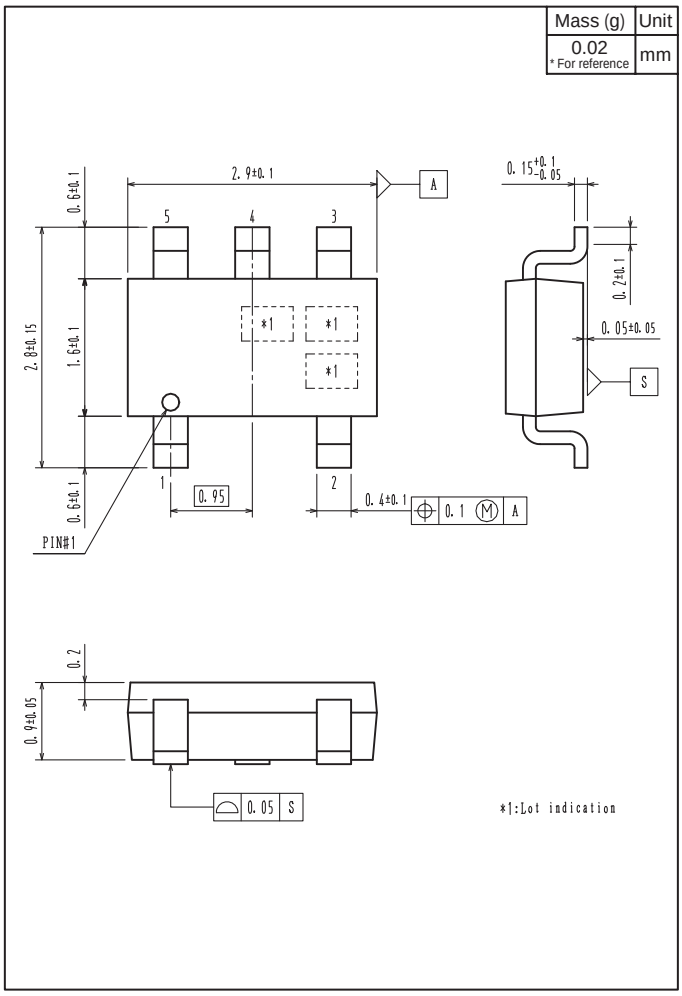
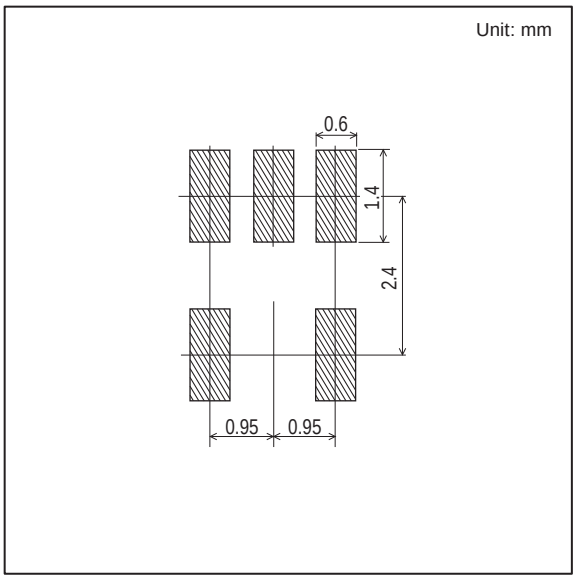
Outline Drawing

CPH5905G-TL-E, CPH5905H-TL-E



Land Pattern Example



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