

PESD5V0U4BW

Ultra low capacitance bidirectional quadruple ESD protection array

6 January 2026 Product data sheet

1. General description

Ultra low capacitance bidirectional quadruple ElectroStatic Discharge (ESD) protection array in an ultra small and flat lead SOT665 Surface-Mounted Device (SMD) plastic package, designed to protect up to four signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of up to four lines
- ESD protection up to 10 kV
- Ultra low diode capacitance: C_d = 2.9 pF
- IEC 61000-4-2; level 4 (ESD)
- Ultra low leakage current: I_{RM} = 5 nA

3. Applications

- Computers and peripherals
- Portable electronics
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems

4. Quick reference data

Table 1. Quick reference data

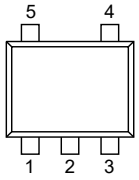
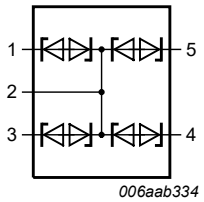
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	2.9	3.5	pF

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 SOT665	
2	CC	common cathode		
3	K2	cathode (diode 2)		
4	K3	cathode (diode 3)		
5	K4	cathode (diode 4)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U4BW	SOT665	plastic, surface-mounted package; 5 leads; 1 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT665

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0U4BW	A6

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[1] [2]	-	10	kV
		MIL-STD-883; human body model (HBM)	[1] [2]	-	8	V

[1] Device stressed with ten non-repetitive ESD pulses.
[2] Measured from pin 1, 3, 4 or 5 to pin 2.

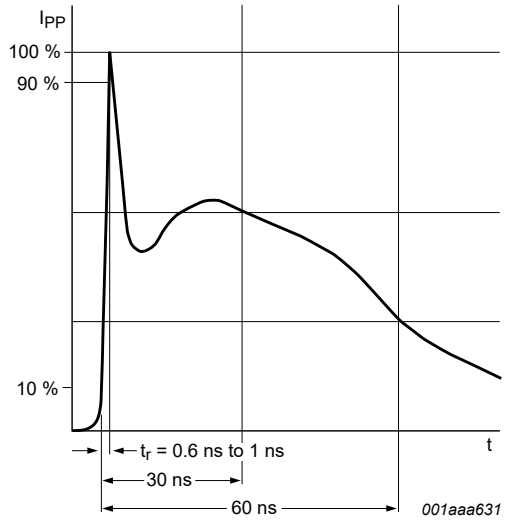


Fig. 1. ESD pulse waveform according to IEC 61000-4-2

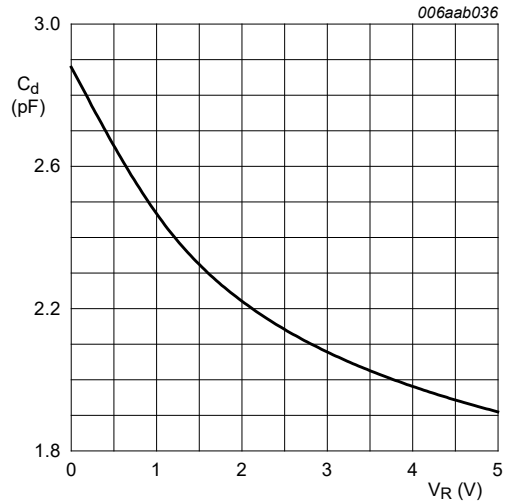
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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
V_{BR}	breakdown voltage	I_R = 5 mA; T_{amb} = 25 °C		5.5	6.5	9.5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V; T_{amb} = 25 °C		-	5	100	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	2.9	3.5	pF
		f = 1 MHz; V_R = 5 V; T_{amb} = 25 °C		-	1.9	-	pF
R_{diff}	differential resistance	I_R = 1 mA; T_{amb} = 25 °C		-	-	100	Ω



f = 1 MHz; T_{amb} = 25 °C

Fig. 2. Diode capacitance as a function of reverse voltage; typical values

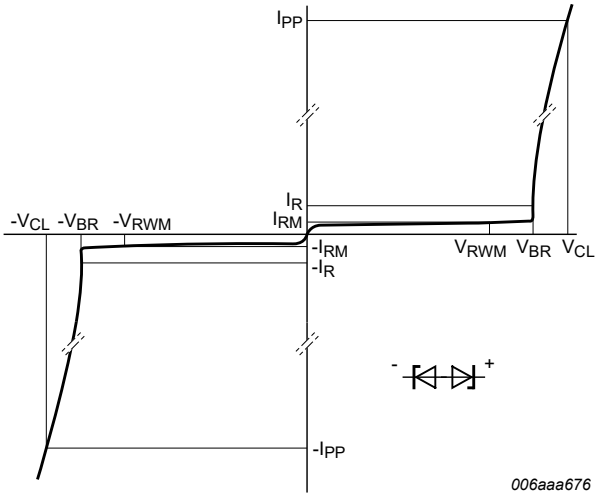


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

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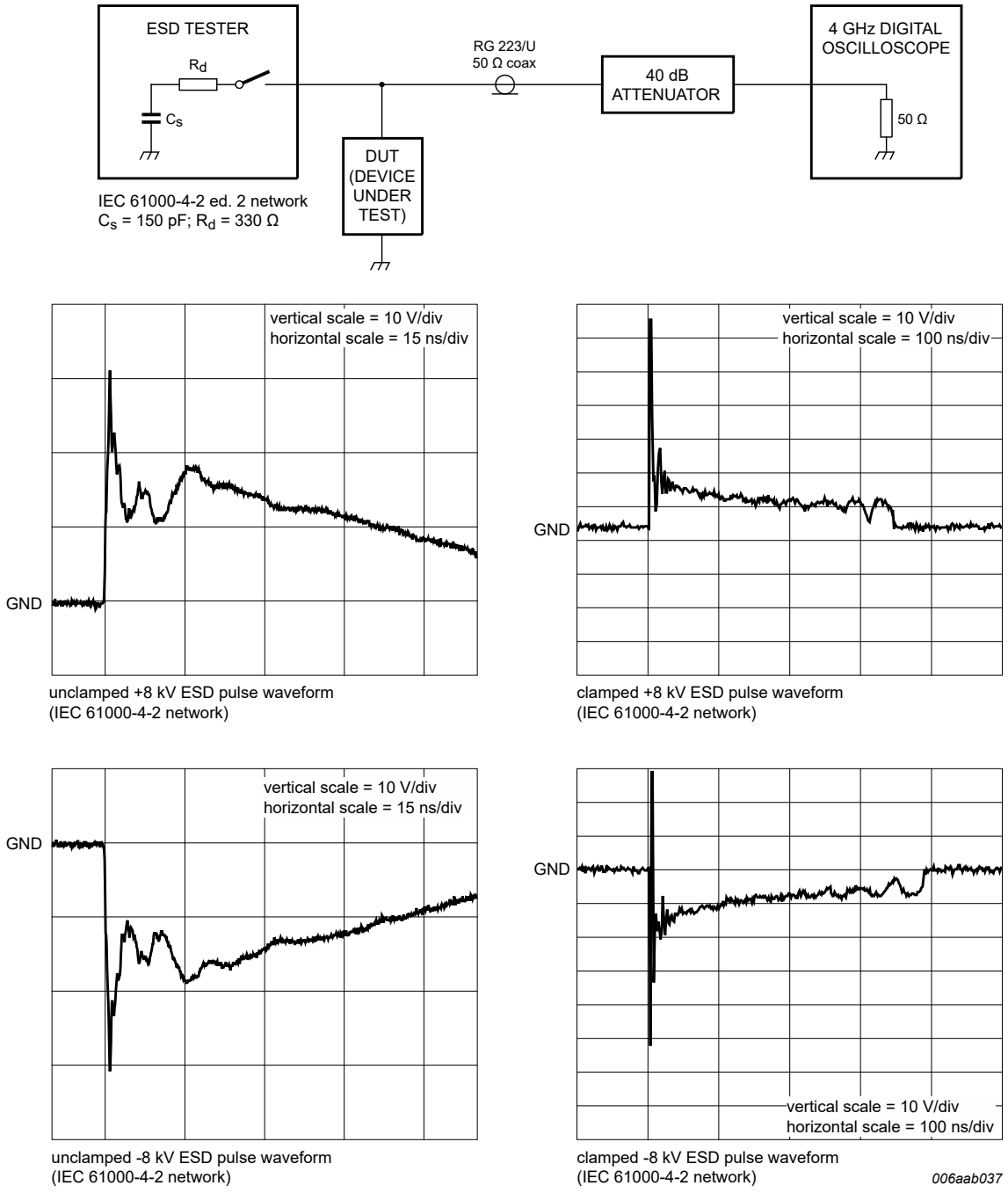


Fig. 4. ESD clamping test setup and waveforms

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10. Application information

The device is designed for the protection of up to four bidirectional data or signal lines from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground.

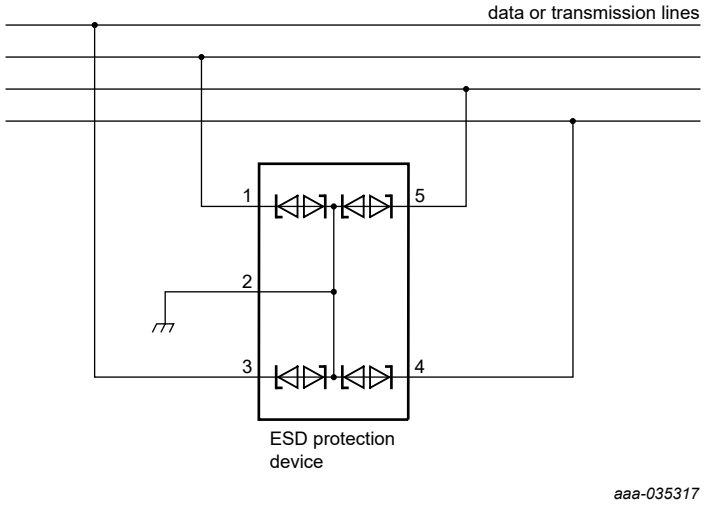


Fig. 5. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

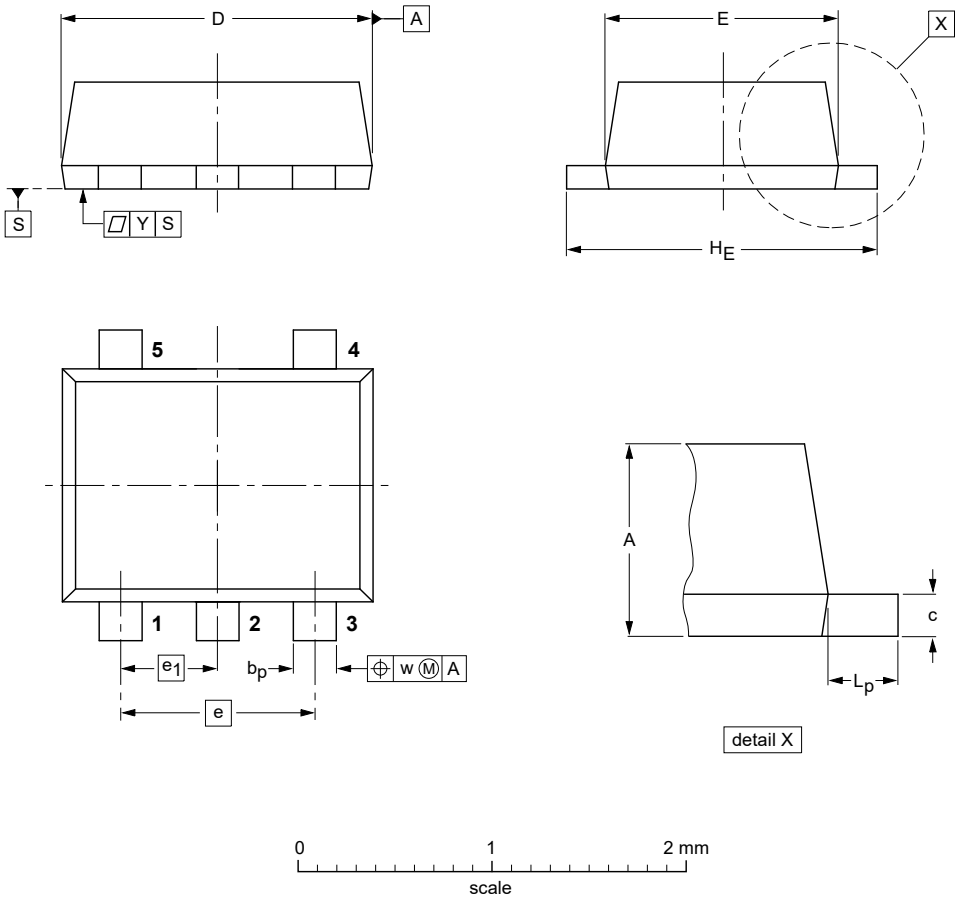
1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

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11. Package outline

Plastic surface-mounted package; 5 leads **SOT665**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT665						~~04-11-08~~ 06-03-16

Fig. 6. Package outline SOT665

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12. Soldering

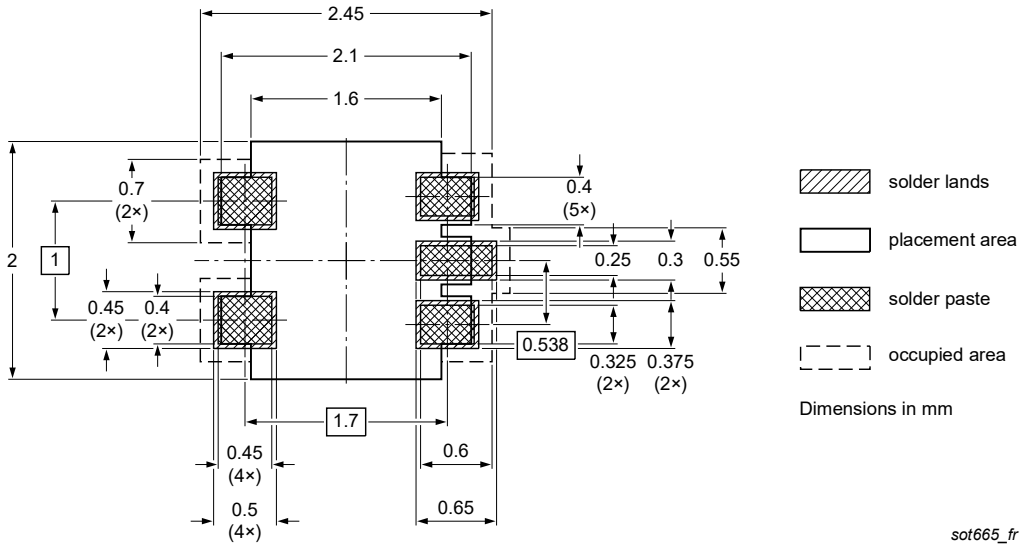


Fig. 7. Reflow soldering footprint for SOT665

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13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U4BW v.3	20260106	Product data sheet	-	PESD5V0U4BW v.2
Modifications:	• Chapter "General description": typo correction			
PESD5V0U4BW v.2	20221228	Product data sheet	-	PESD5V0U4BF_ PESD5V0U4BW_1
PESD5V0U4BF_ PESD5V0U4BW_1	20080815	Product data sheet	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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