MP2457

36V, 0.6A, 2MHz, Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2457 is a high-frequency, step-down, switching regulator with integrated high-side and low-side power MOSFETs. The MP2457 can provide up to 0.6A of output current efficiently with current-mode control for fast loop response.

The wide 5V to 36V input range accommodates a variety step-down applications, and the 0.6μA shutdown mode quiescent current allows the device to be used in battery-powered applications. The MP2457 uses high duty cycle and low dropout mode for low input voltage conditions.

The MP2457 achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

Frequency foldback prevents short circuit and inductor current runaway during start-up. Thermal shutdown provides reliable and fault-tolerant operation.

The MP2457 is available in a cost-effective TSOT23-6 package.

FEATURES

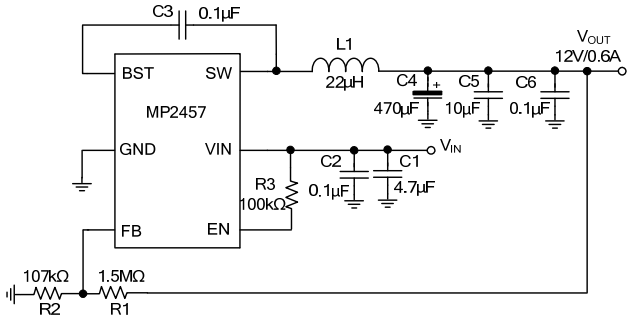
- Meets 0.1% Output Voltage Ripple
- Low Dropout Mode
- 65μA Operating Quiescent Current
- Light-Load Mode
- >90% Efficiency
- Dedicated Internal Compensation
- Stable with Ceramic/Electrolytic Output Capacitors
- Wide 5V to 36V Operating Input Range
- 400mΩ/200mΩ Internal Power MOSFETs
- 2MHz Fixed Switching Frequency
- Internal Soft Start (SS)
- Precision Current Limit without Current Sensing Resistor
- Output Adjustable from 0.8V to 0.95·V_{IN}
- Guaranteed Industrial Temperature Range Limits
- Available in a TSOT23-6 Package

APPLICATIONS

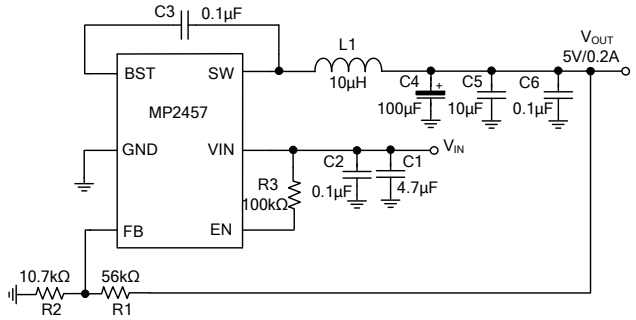
- Power Meters
- Aftermarket Automotive
- Multi-Function Printers (MFP)
- General Consumer

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TYPICAL APPLICATION



12V Output, 0.6A Load



5V Output, 0.2A Load

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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2457GJ	TSOT23-6	*See Below*

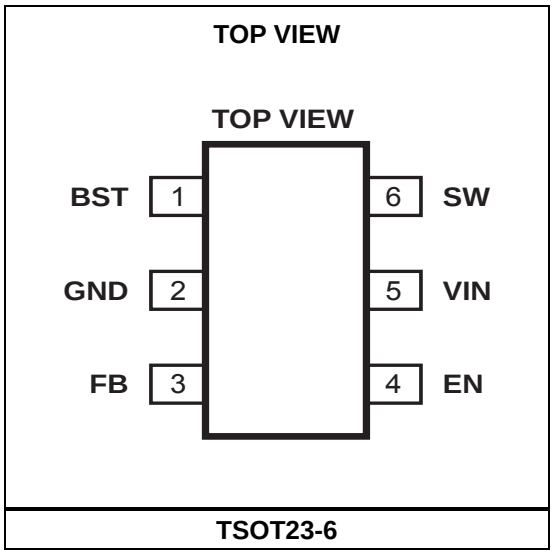
* For Tape & Reel, add suffix –Z (e.g.: MP2457GJ–Z).

TOP MARKING

|AQZY

AQZ: Product code of MP2457GJ
Y: Year code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +40V
Switch voltage (V_{SW}) ..... -0.3V to (V_{IN} + 0.3V)
BST to SW ..... -0.3 to +6.0V
All other pins ..... -0.3V to +6.0V
Continuous power dissipation (T_A = 25°C) (2) 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 5V to 36V
Output voltage (V_{OUT}) ..... Adjustable from 0.8V
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance (3) θ_{JA} θ_{JC}

TSOT23-6	100	55 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device. The value of V_{IN} is guaranteed at T_J = +25°C.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (4), unless otherwise noted. Typical values at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	T_J = -40°C to +125°C	0.78	0.8	0.82	V
		T_J = +25°C	0.788	0.8	0.812	
Feedback bias current					0.1	µA
High-side switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		400	800	mΩ
Low-side switch on resistance	R_{ON_LS}			200	400	mΩ
High-side switch leakage		V_{EN} = 0V, V_{SW} = 0V			1	µA
Low-side switch leakage					1	µA
Current limit	I_{LIM}		0.7	0.9	1.1	A
V_{IN} UVLO rising threshold			4.35	4.6	4.85	V
V_{IN} UVLO falling threshold			3.65	3.9	4.15	V
V_{IN} UVLO hysteresis				0.7		V
Soft-start time		V_{FB} from 10% to 90%		0.5	1	ms
Oscillator frequency	f_{SW}		1.6	2	2.4	MHz
Minimum switch on time (5)	t_{ON}			100		ns
Shutdown supply current	I_S	V_{EN} < 0.3V		0.6	1.5	µA
Quiescent supply current	I_Q	No load, V_{FB} = 0.83V, no switching		65	80	µA
Thermal shutdown (5)				175		°C
Thermal shutdown hysteresis (5)				30		°C
Enable rising threshold	V_{IH}	Low to high	1.62	1.8	1.98	V
Enable falling threshold			1.395	1.55	1.705	V
Enable threshold hysteresis				250		mV

NOTES:

4) Not tested in production and guaranteed by over-temperature correlation.

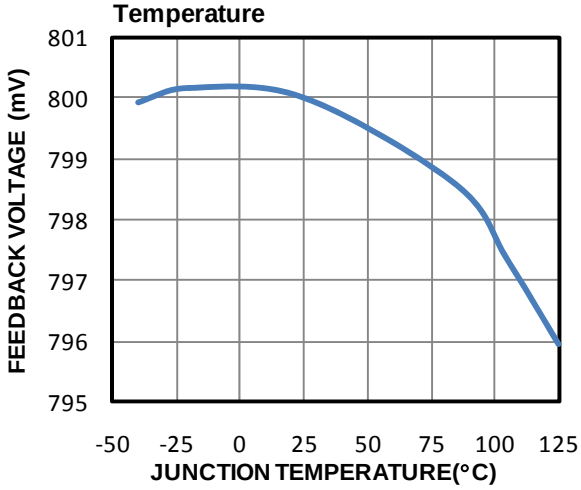
5) Not tested in production and derived from bench characterization.

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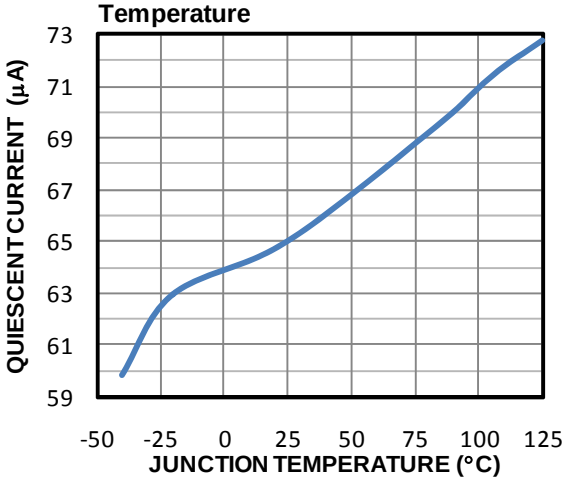
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TYPICAL CHARACTERISTICS

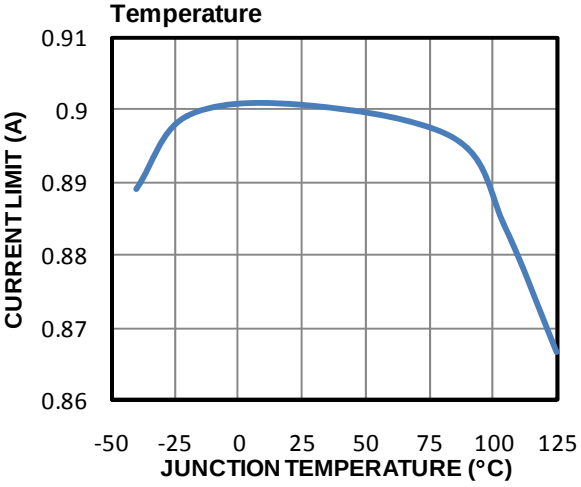
Feedback Voltage vs. Junction Temperature



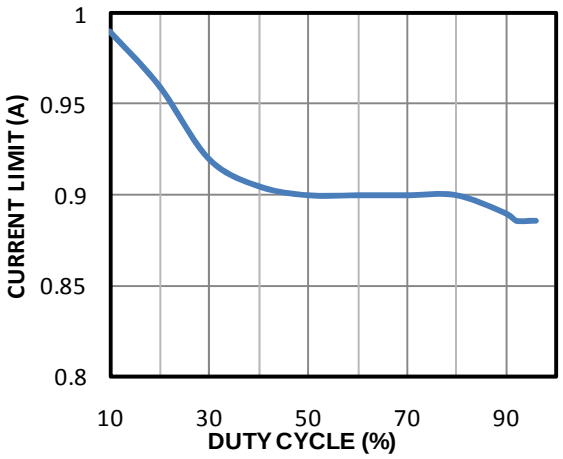
Quiescent Current vs. Junction Temperature



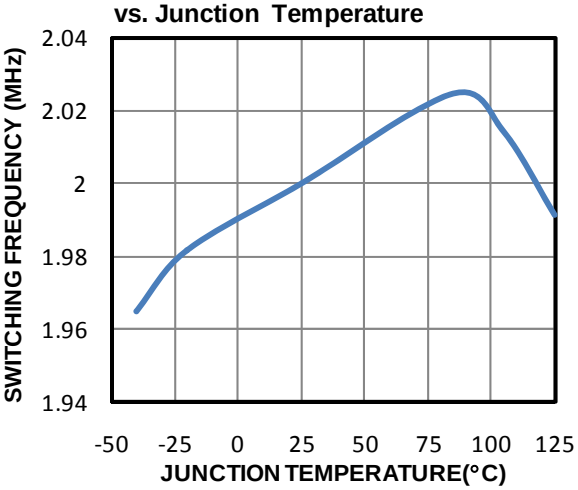
Current Limit vs. Junction Temperature



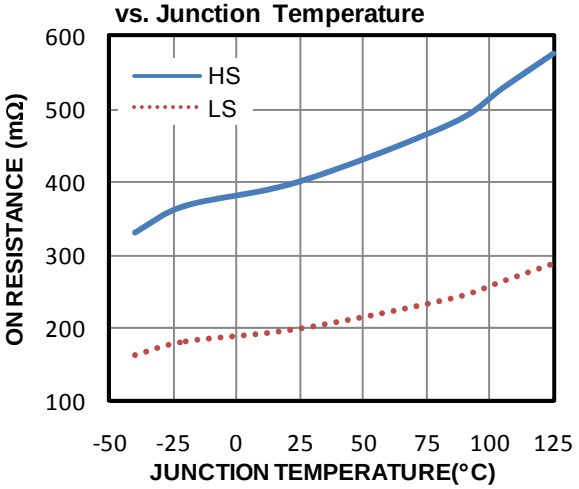
Current Limit vs. Duty Cycle



Switching Frequency vs. Junction Temperature



Switch On Resistance vs. Junction Temperature

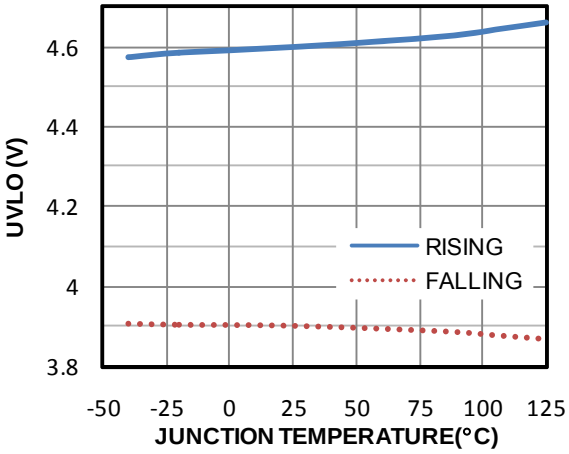


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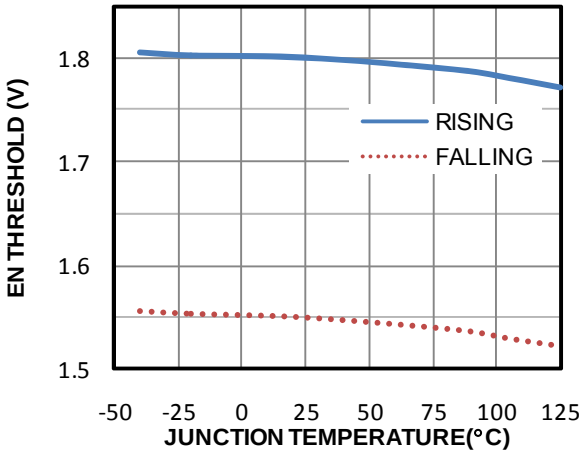
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} UVLO vs. Junction Temperature



EN Threshold vs. Junction Temperature



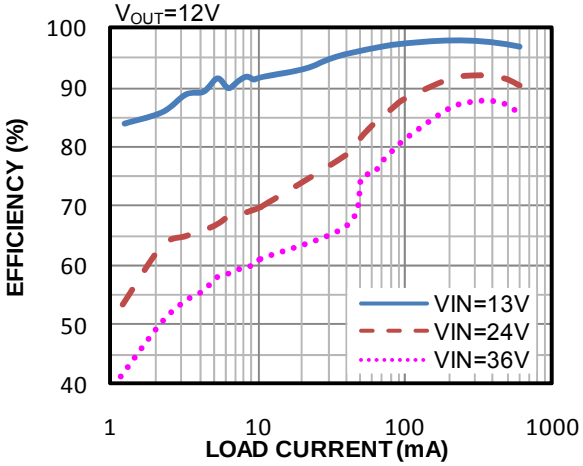
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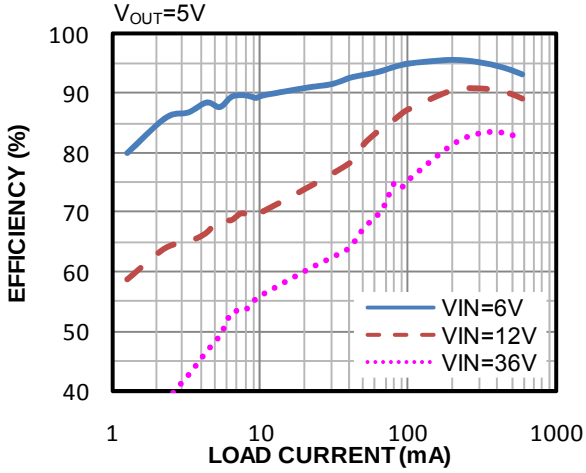
TYPICAL PERFORMANCE CHARACTERISTIC

V_{IN} = 24V, V_{OUT} = 12V, C1 = 4.7µF, C5 = 10µF, C4 = 470µF, L1 = 22µH, and T_A = +25°C, unless otherwise noted.

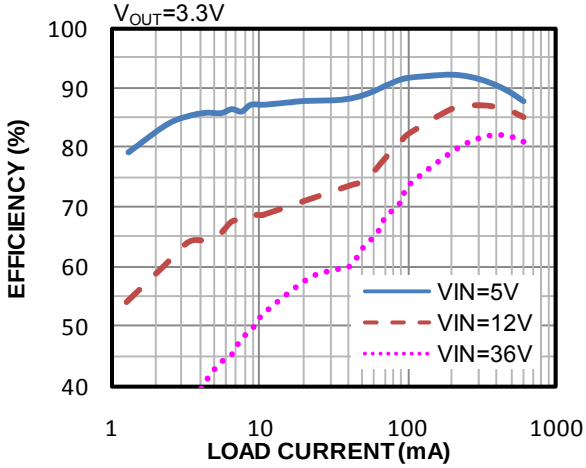
Efficiency vs. Load Current
V_{OUT}=12V



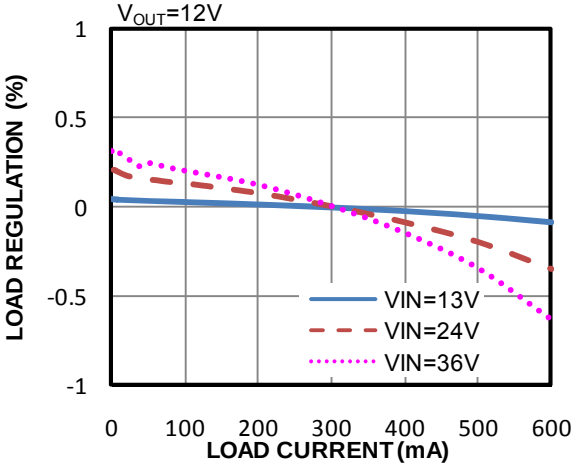
Efficiency vs. Load Current
V_{OUT}=5V



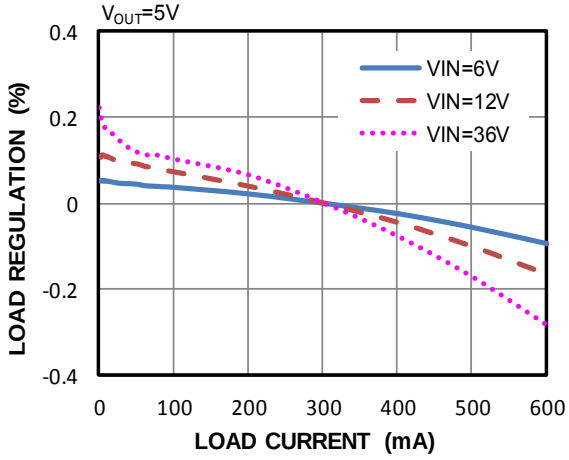
Efficiency vs. Load Current
V_{OUT}=3.3V



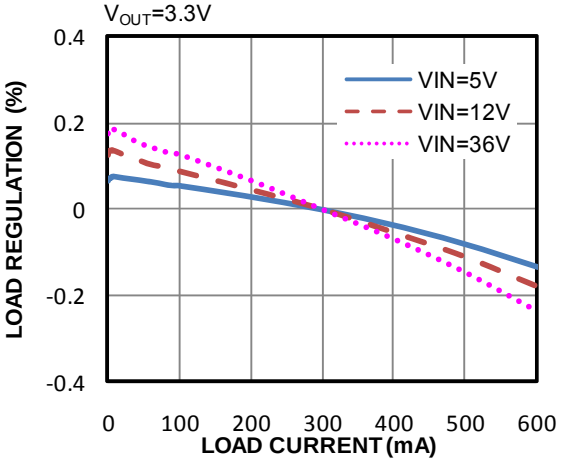
Load Regulation
V_{OUT}=12V



Load Regulation
V_{OUT}=5V



Load Regulation
V_{OUT}=3.3V



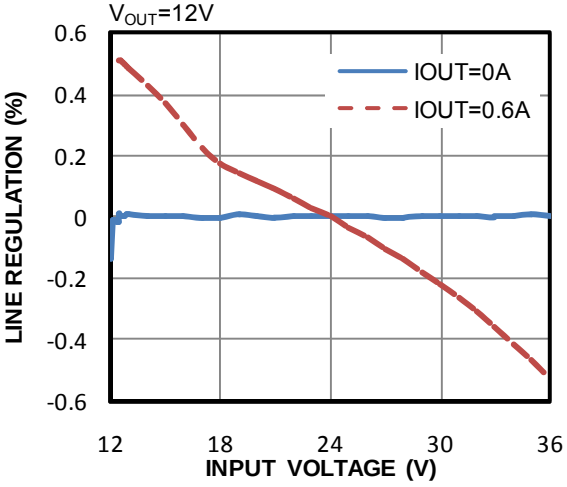
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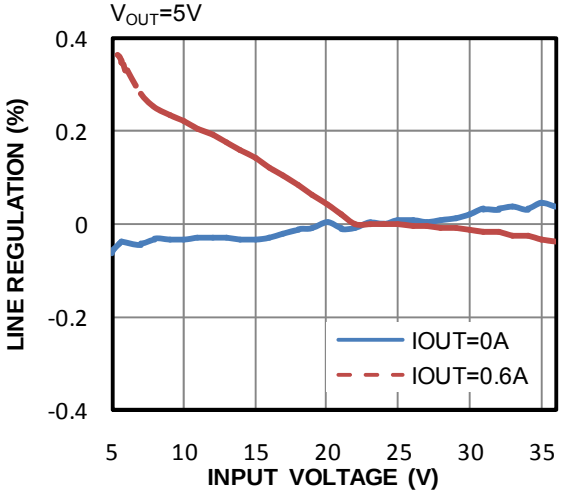
TYPICAL PERFORMANCE CHARACTERISTIC *(continued)*

V_{IN} = 24V, V_{OUT} = 12V, C1 = 4.7µF, C5 = 10µF, C4 = 470µF, L1 = 22µH, and T_A = +25°C, unless otherwise noted.

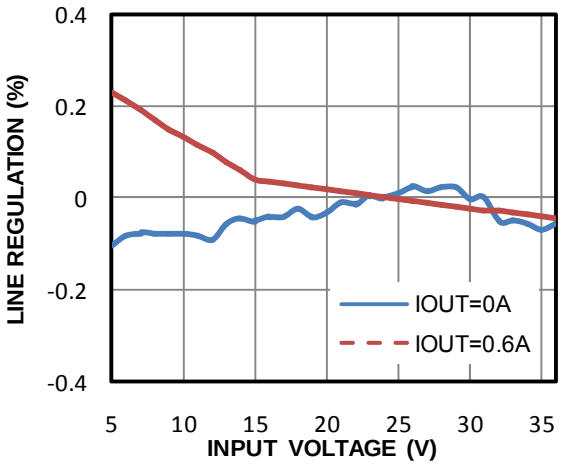
Line Regulation
V_{OUT}=12V



Line Regulation
V_{OUT}=5V



Line Regulation
V_{OUT}=3.3V



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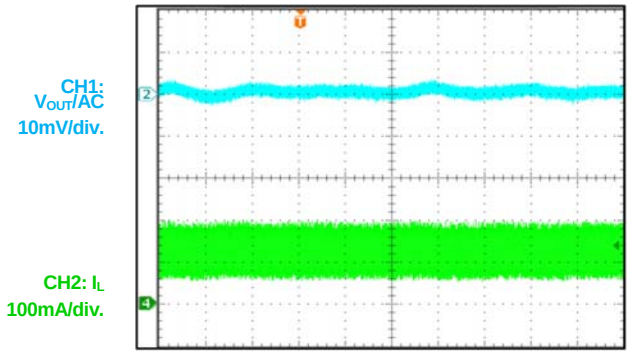
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TYPICAL PERFORMANCE CHARACTERISTIC *(continued)*

V_{IN} = 24V, V_{OUT} = 12V, C1 = 4.7µF, C5 = 10µF, C4 = 470µF, L1 = 22µH, and T_A = +25°C, unless otherwise noted.

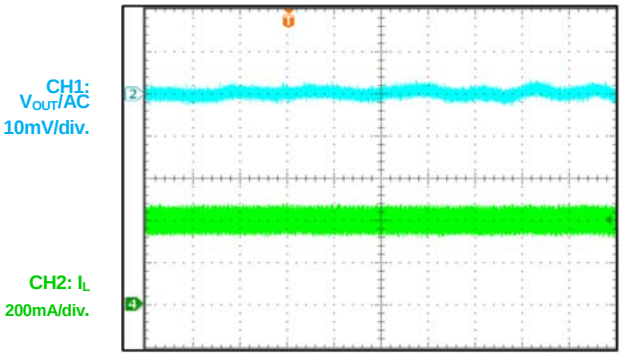
Output Voltage Ripple

I_{OUT} = 0.125A



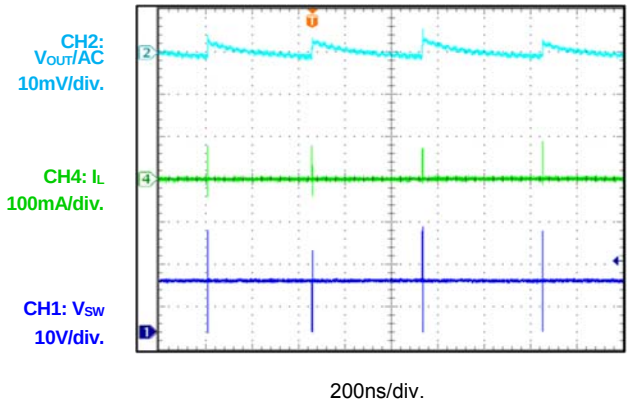
Output Voltage Ripple

I_{OUT} = 0.4A



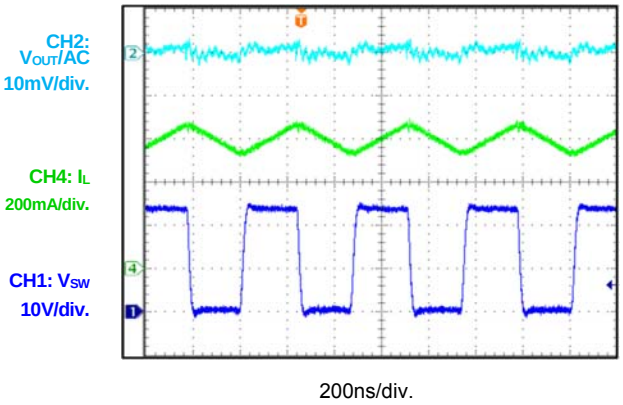
Steady State

I_{OUT} = 0A



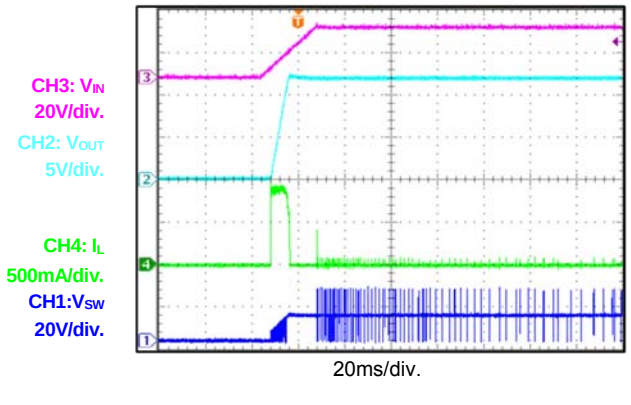
Steady State

I_{OUT} = 0.6A



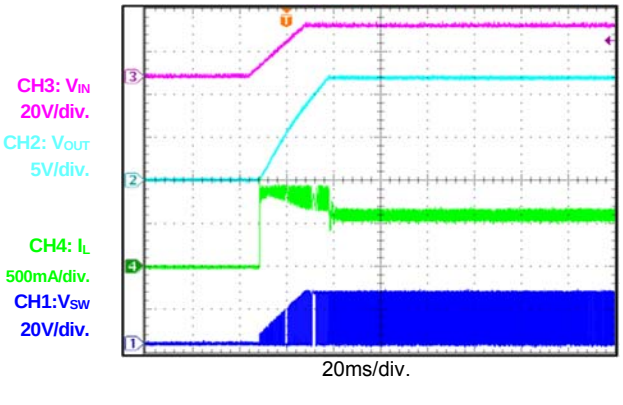
Start-Up through V_{IN}

I_{OUT} = 0A



Start-Up through V_{IN}

I_{OUT} = 0.6A



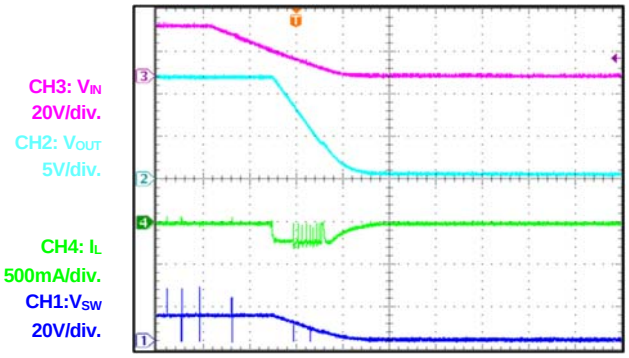
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TYPICAL PERFORMANCE CHARACTERISTIC *(continued)*

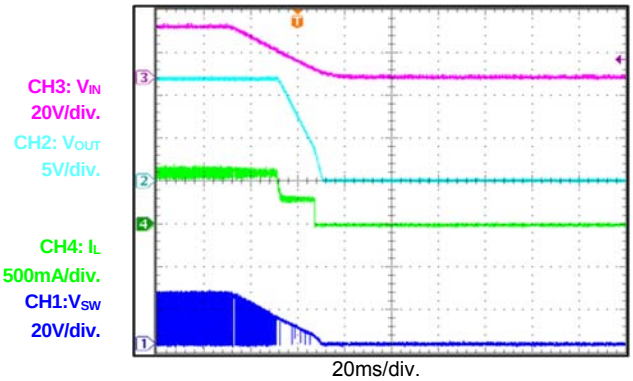
V_{IN} = 24V, V_{OUT} = 12V, C1 = 4.7µF, C5 = 10µF, C4 = 470µF, L1 = 22µH, and T_A = +25°C, unless otherwise noted.

Shutdown through V_{IN}
I_{OUT} = 0A



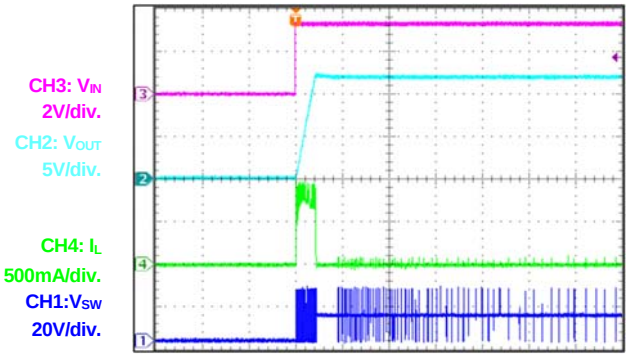
20ms/div.

Shutdown through V_{IN}
I_{OUT} = 0.6A



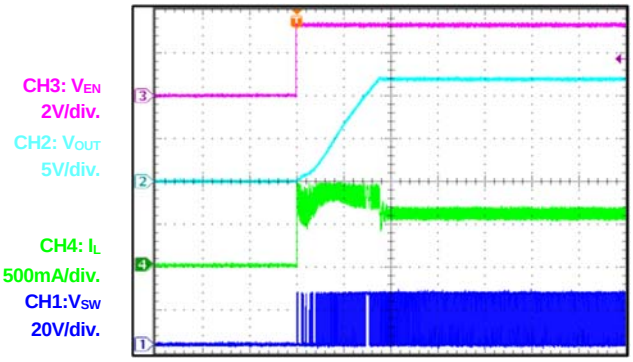
20ms/div.

Start-Up through EN
I_{OUT} = 0A



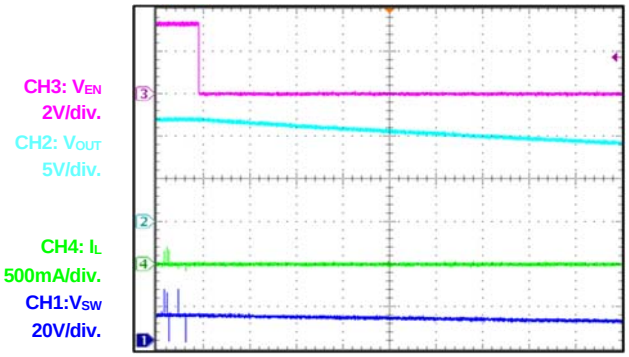
20ms/div.

Start-Up through EN
I_{OUT} = 0.6A



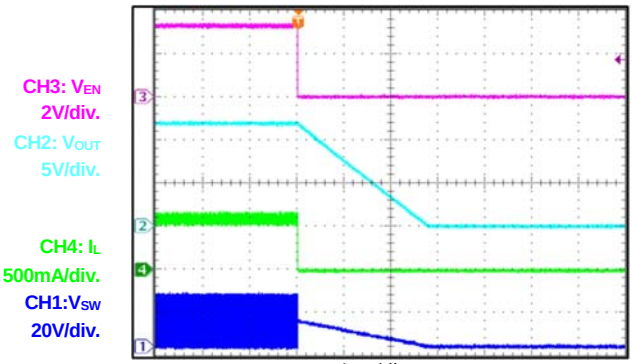
4ms/div.

Shutdown through EN
I_{OUT} = 0A



4s/div.

Shutdown through EN
I_{OUT} = 0.6A



4ms/div.

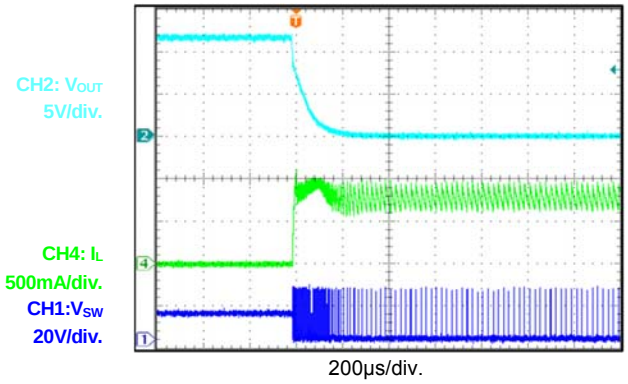
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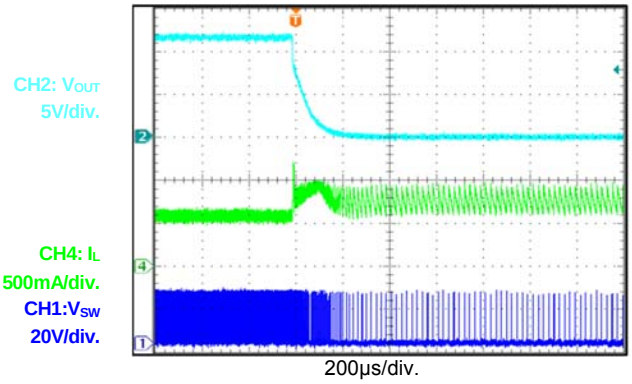
TYPICAL PERFORMANCE CHARACTERISTIC *(continued)*

V_{IN} = 24V, V_{OUT} = 12V, C1 = 4.7µF, C5 = 10µF, C4 = 470µF, L1 = 22µH, and T_A = +25°C, unless otherwise noted.

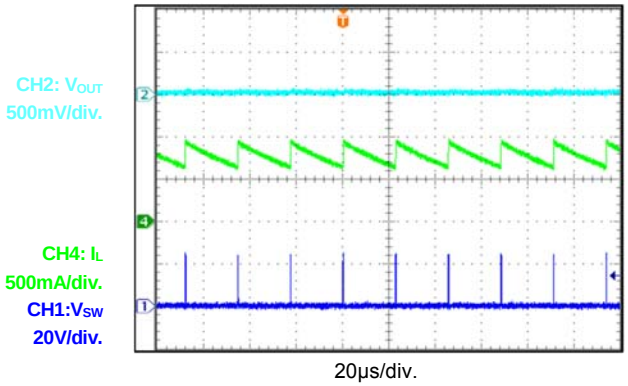
SCP Entry
I_{OUT} = 0A to Short Circuit



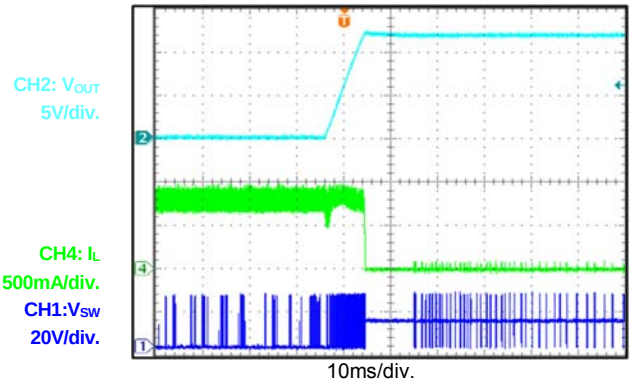
SCP Entry
I_{OUT} = 0.6A to Short Circuit



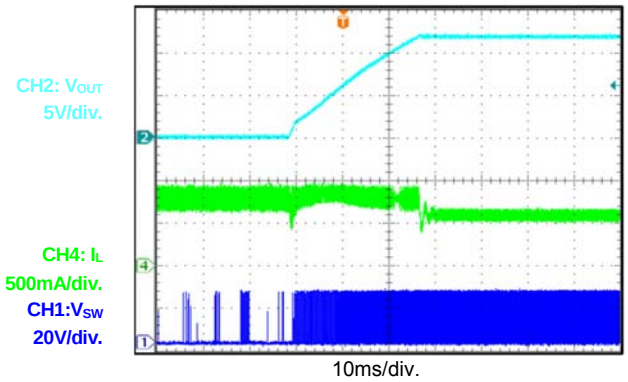
SCP Steady State



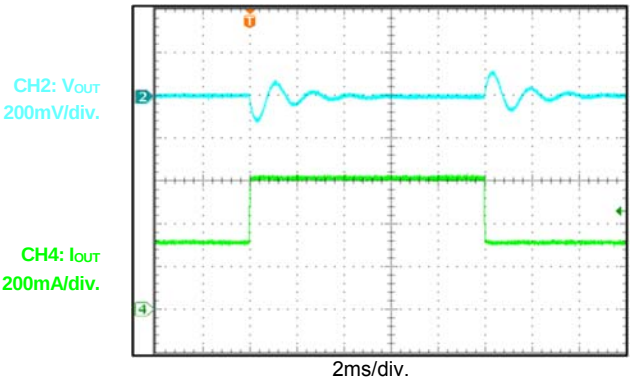
SCP Recovery
Short Circuit to I_{OUT} = 0A



SCP Recovery
Short Circuit to I_{OUT} = 0.6A



Load Transient
I_{OUT} = 0.3A <-> 0.6A, 1.6A/µs



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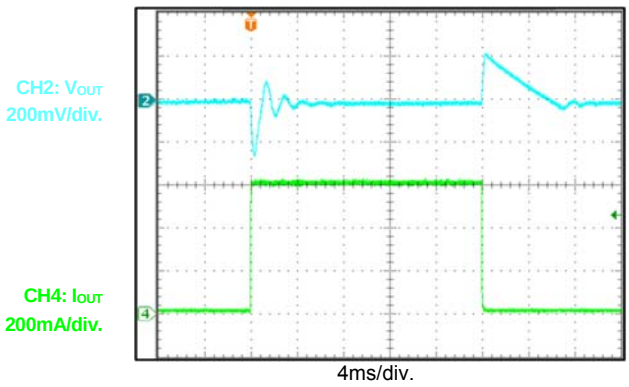
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TYPICAL PERFORMANCE CHARACTERISTIC *(continued)*

V_{IN} = 24V, V_{OUT} = 12V, C1 = 4.7µF, C5 = 10µF, C4 = 470µF, L1 = 22µH, and T_A = +25°C, unless otherwise noted.

Load Transient

I_{OUT} = 10mA <-> 0.6A, 1.6A/µs



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PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
2	GND	**Ground.** Connect an output capacitor as close to GND as possible. Avoid routing GND near high-current switch paths.
3	FB	**Feedback.** FB is the input to the error amplifier. Connect FB to an external resistor divider between the output and GND. Compare FB against the internal 0.8V reference to set the regulation voltage.
4	EN	**Enable input.** Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip. Float EN to disable the chip.
5	VIN	**Input supply.** VIN supplies power to the internal control circuitry, both BST regulators, and the high-side switch. Place a decoupling capacitor to ground close to VIN to reduce switching spikes.
6	SW	**Switch node.** SW is the output of the high-side switch.

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BLOCK DIAGRAM

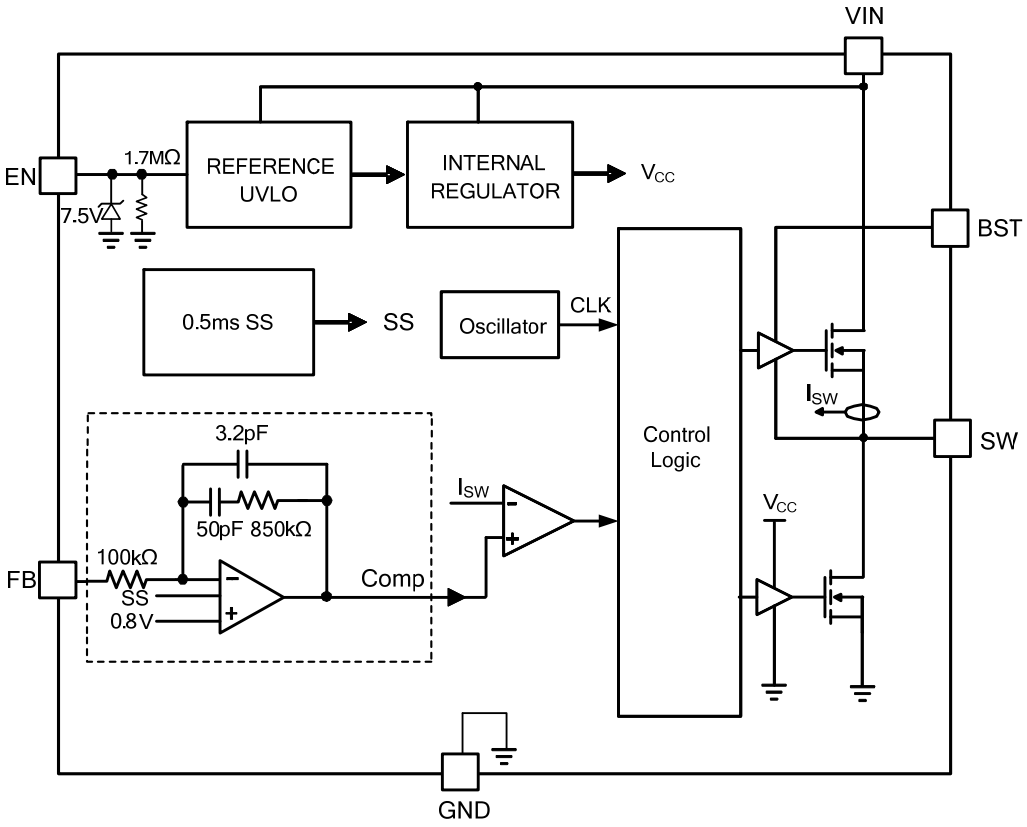


Figure 1: Functional Block Diagram

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OPERATION

The MP2457 is a 2MHz, synchronous, step-down, switching regulator with integrated high-side and low-side power MOSFETs. The MP2457 provides an internally compensated, highly efficient output of up to 0.6A with current-mode control and also features a wide input voltage range, internal soft-start control, and a precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the MP2457 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle initiated by the internal clock turns on the power high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). After the HS-FET is off, the low-side MOSFET (LS-FET) turns on, and the inductor current flows through the LS-FET. To avoid a shoot-though, a dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time. For each turn-on and turn-off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

To prevent inductor current and output voltage runaway, the switching frequency folds back when the HS-FET minimum turn-on is detected internally.

When the PWM signal goes low, the HS-FET turns off and remains off for at least 160ns before the next cycle begins. If the current in the HS-FET does not reach the COMP-set current value within one PWM cycle, the HS-FET remains on to avoid a turn-off operation.

Pulse-Skipping Mode (PSM)

Under light-load conditions, the MP2457 enters pulse-skipping mode (PSM) to improve efficiency. PSM is triggered when V_{COMP} drops below the internal sleep threshold, which generates a pause command to block the turn-on clock pulse, so the power MOSFET does not turn on. This reduces gate driving and switching losses. The pause command causes the entire chip to enter sleep mode, reducing the quiescent current to improve light-load efficiency.

When V_{COMP} exceeds the sleep threshold, the pause signal resets, and the chip resumes normal PWM operation. Whenever the pause command changes from low to high, the PWM signal goes high immediately and turns on the power MOSFET.

Error Amplifier (EA)

The error amplifier is composed of an internal op-amp with an R-C feedback network connected between its output node (internal COMP node) and its negative input node (FB). When the FB voltage (V_{FB}) drops below the internal reference voltage (V_{REF}), the op-amp drives the COMP output high, producing a higher switch peak current output and delivering more energy to the output. Conversely, when V_{FB} rises above V_{REF}, the switch peak current output drops.

Connect FB to the tap of a voltage divider connected between V_{OUT} and GND composed of R_1 and R_2. R_1 also serves to control the gain of the error amplifier in addition to the internal compensation R-C network.

Internal Regulator

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 3.0V, the output of the regulator is in full regulation. When V_{IN} drops below 3.0V, the output degrades.

Enable Control (EN)

The MP2457 has a dedicated enable control pin (EN). When V_{IN} rises above the threshold, EN can enable or disable the chip for high effective logic. Its falling threshold is 1.55V, and its rising threshold is about 1.8V. An internal 1.7MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

When the EN voltage is pulled to 0V, the chip enters the lowest shutdown current mode. When the EN voltage rises above 0V but remains below the rising threshold, the chip remains in shutdown mode with a slightly higher shutdown current.

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EN is clamped internally using a 7.5V series Zener diode. Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current below 100μA. For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 7.5V) \div 100\mu A = 45k\Omega$.

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

Under-Voltage Lockout (UVLO)

V_{IN} under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is approximately 4.6V, while its falling threshold is 3.9V.

Internal Soft Start (SS)

A reference-type soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V during the SS time. When V_{SS} is lower than V_{REF}, V_{SS} overrides V_{REF} as the error amplifier reference.

The maximum V_{SS} value is approximately the same as V_{FB}, so if V_{FB} falls, the maximum of V_{SS} falls. This accommodates short-circuit recovery. When the short circuit is removed, V_{SS} ramps up to prevent an output voltage overshoot.

Thermal Shutdown

Thermal shutdown prevents thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of about 2.4V and a falling threshold of about 300mV. During UVLO, V_{SS} resets to zero. When the UVLO ends, the controller enters soft start.

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes falls below its regulation, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path goes from V_{IN} to BST to SW. The external circuit must provide enough voltage headroom to facilitate the charging.

Current Comparator and Current Limit

A current-sense MOSFET senses the power MOSFET current. This current is input to the high-speed current comparator for current-mode control. When the power MOSFET turns on, the comparator is first blanked to limit noise, and then compares the power switch current against V_{COMP}. When the sensed value exceeds V_{COMP}, the comparator output goes low to turn off the power MOSFET. The maximum current of the internal power MOSFET is limited cycle-by-cycle internally. The switching frequency folds back to prevent an inductor current runaway during start-up or a short circuit.

Low Dropout Operation

The MP2457 is designed to operate at almost 100% duty cycle to improve dropout. When the current in the HS-FET does not reach the COMP-set current value within one PWM cycle, the HS-FET remains on to prevent a turn-off operation. The HS-FET can remain on for a maximum of 15μs and then turns off for a minimum of 160ns.

To prevent the voltage across BST to SW from dropping too low during the low dropout operation, the current comparator enters power-save mode, in which the speed is degraded. This reduces the bootstrap capacitor current consumption when HS-FET turns on for longer than 2μs. Therefore, the voltage across the bootstrap capacitor can remain at a high level (close to 5V).

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block first starts to generate a stable reference voltage and current, and then the internal regulator starts to provide a stable supply for the rest of the circuit.

While the internal supply rail is up, an internal timer turns the power MOSFET off for about 50μs to blank any start-up noise. When the internal soft-start block is enabled, it first holds its SS output low to ensure that the rest of the circuit is ready before ramping up.

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Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled low. The floating driver is not subject to this shutdown command, but its charging path is disabled.

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APPLICATION INFORMATION

Setting the Output Voltage

Set the output voltage of MP2457 by using a resistor divider (see Figure 2):

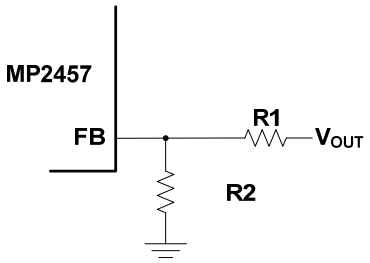


Figure 2: FB Resistor Divider to Set V_{OUT}

Calculate the output voltage with Equation (1):

$$V_{OUT} = V_{FB} \frac{(R1+R2)}{R2} \quad (1)$$

The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation network.

To achieve optimal stability performance and transient response, choose R1 to be around 1.5MΩ in applications with a 12V output rail. Set R1 to be 56kΩ for 5V output rail applications. Then, calculate R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (2)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
5V	56kΩ (1%)	10.7kΩ (1%)
12V	1.5MΩ (1%)	107kΩ (1%)

Selecting the Inductor

The inductor supplies constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage but also has a larger physical size, higher series resistance, and lower saturation current.

To determine the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current and choose a peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L1 = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where I_{LOAD} is the load current.

Additionally, the inductor value influences the MP2457 load ability during start-up. When the output voltage starts up, f_S folds back the minimum to several tens of kHz. Based on Equation (4), a smaller L1 or a lower f_S leads to a higher I_{LP}. Therefore, if a small inductor value is used (e.g.: 10μH inductor in a 5V output application), the current limit is reached when the MP2457 starts up with a >250mA constant current load. Then, the output voltage fails to be set up. In this case, for a >250mA constant current load with a 10μH inductor, the MP2457 must first start up with a load <250mA before increasing the current load. However, if the load is resistive, the MP2457 can output a >250mA load sufficiently.

Selecting the Input Capacitor

The input capacitor (C1) can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (C2) (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

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The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

An output capacitor (C4) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C4}\right) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C4} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

In power meter applications, the output capacitors are large-value electrolytic capacitors, typically, with an R_{ESR} and capacitance with a large temperature variation. This large temperature variation changes the part's feedback loop, making it difficult to keep the loop stable over the full operation temperature, especially when the MP2457 works in a deep dropout mode (V_{IN} - V_{OUT} < 1V).

It is recommended that the capacitance of the electrolytic capacitor be less than 560μF, and R_{ESR} should be greater than 70mΩ at room temperature.

Compensation Components

The goal of compensation design is to shape the converter transfer function to achieve a desirable loop gain. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies can cause system instability. Generally, set the crossover frequency to equal approximately one-tenth of the switching frequency. If using an electrolytic capacitor, select a loop bandwidth no higher than 1/4 of the ESR zero frequency (f_{ESR}), where f_{ESR} can be calculated with Equation (9):

$$f_{ESR} = \frac{1}{2\pi \times C4 \times R_{ESR}} \quad (9)$$

High Duty Cycle Application Limit

To improve low dropout performance, the MP2457 duty cycle is designed very close to 100% by scaling down the switching frequency approximatively when V_{IN} is close to V_{OUT}.

However, when the MP2457 operates in deep dropout mode (V_{IN} - V_{OUT} < 1V), an additional pole appears within the bandwidth of the feedback loop. This additional pole reduces the loop phase margin and may cause some instability, which makes the output voltage ripple increase. In applications with a 12V output rail, the minimum V_{IN} should be higher than 12.8V. It is recommended that the capacitance of the output electrolytic capacitor be less than 560μF, and R_{ESR} should be greater than 70mΩ.

If V_{IN} drops below V_{OUT}, V_{COMP} increases to its high clamped voltage. Because VCOMP needs time to recover from a high-to-low clamp, the output voltage experiences an overshoot when V_{IN} steps up higher than V_{OUT} quickly.

The MP2457's slope compensation is not enough to prevent the current limit from dropping too low in dropout mode when the inductor value is small. For example, if a 10μH inductor is used in 5V output rail

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applications, the MP2457 may suffer instability around V_{IN} = 7V. To avoid this instability, use a high-value inductor.

Table 2 shows a component selection guide for 12V and 5V output rail applications.

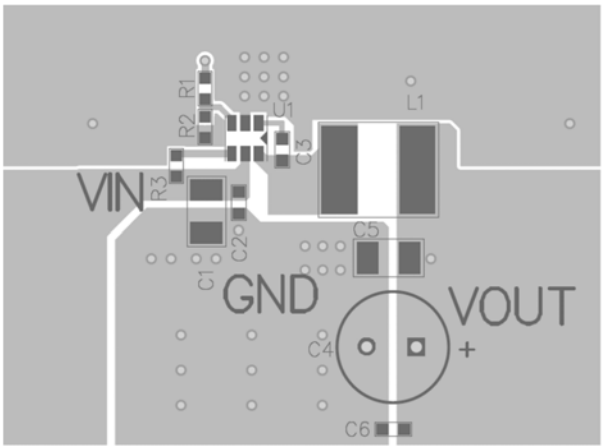
Short-Circuit Application Limit

The MP2457 implements short-circuit protection (SCP) by scaling down the frequency when a fault occurs. However, SCP is guaranteed at $V_{IN} \leqslant$ 25V. At V_{IN} > 25V, due to a low response speed of the current limit loop, there is a risk that the inductor current will rush high when SCP enters with a special slew rate.

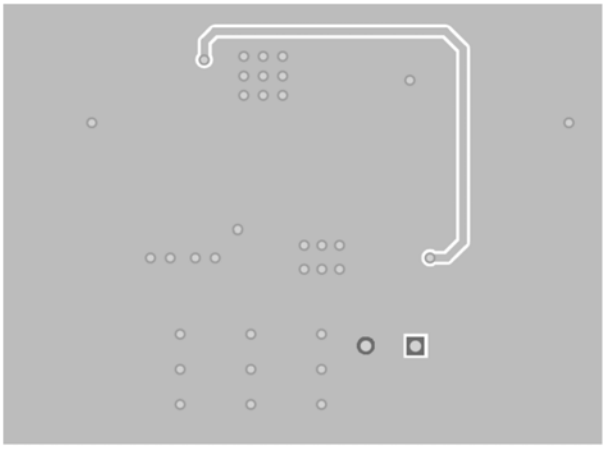
PCB Layout Guidelines

Efficient PCB layout requires high-frequency noise considerations to limit voltage spikes on the SW node and to limit EMI noise. For best results, refer to Figure 3 and follow the guidelines below.

1. Keep the path of the input decoupling capacitor, VIN, SW, and PGND as short as possible using short and wide traces.
2. Keep the passive components as close to the device as possible.
3. Run the feedback trace far from the inductor and noisy power traces. If possible, run the feedback trace on the opposite side of the PCB from the inductor, separated by a ground plane.
   Expect greater switching losses at high switching frequencies.
4. Add a grid of thermal vias under the exposed pad to improve thermal conductivity.
5. Use small vias (15mil barrel diameter) so that the hole fills during the plating process and prevent solder wicking during the reflow process associated with larger vias.
6. Use a pitch (distance between the centers) of approximately 40mil between the thermal vias.



Top Silk and Top Layer



Bottom Layer

Figure 3: Recommended Layout

Table 2: Components Selection Guide

V_{OUT}	Load	R1	R2	L1	C3	C4	
						Capacitance	R_{ESR}
5V	200mA	56kΩ (1%)	10.7kΩ (1%)	10µH	10µF	100µF	>70mΩ
	600mA	56kΩ (1%)	10.7kΩ (1%)	22µH	10µF	100µF	>70mΩ
12V	600mA	1.5MΩ (1%)	107kΩ (1%)	22µH	10µF	470µF	>70mΩ

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TYPICAL APPLICATION CIRCUITS

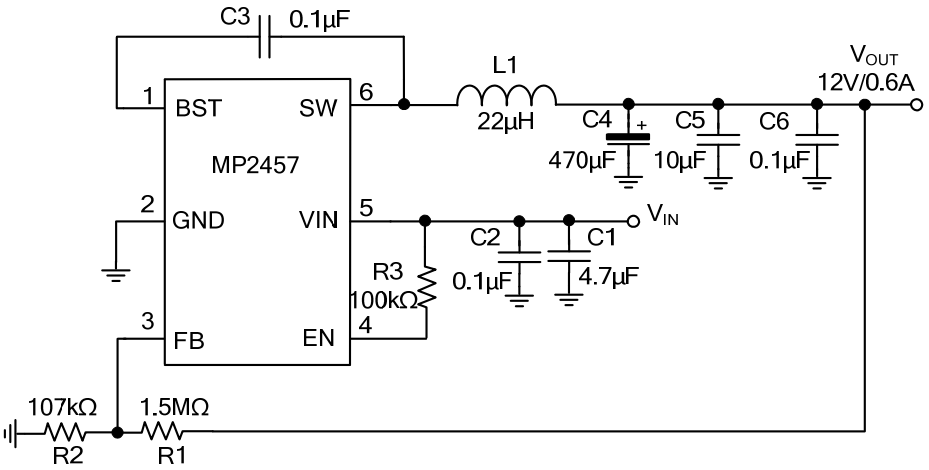


Figure 4: 12V Output

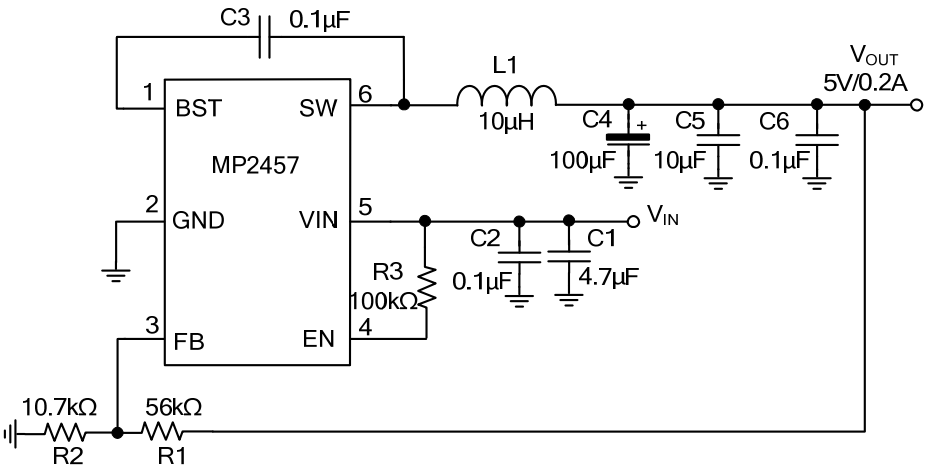


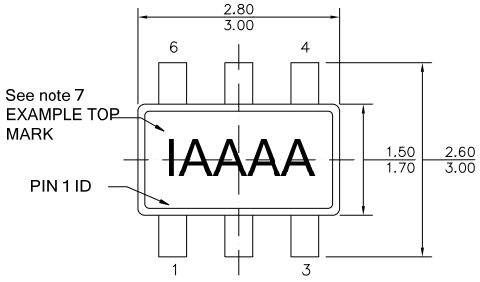
Figure 5: 5V Output

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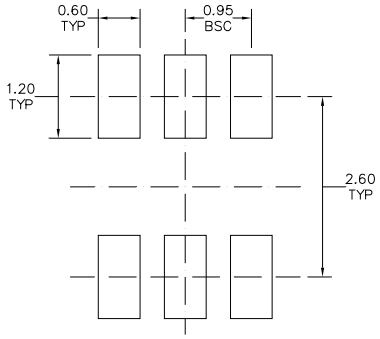
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PACKAGE INFORMATION

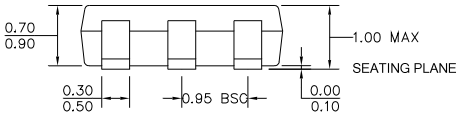
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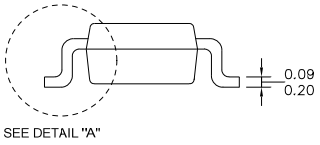
TOP VIEW



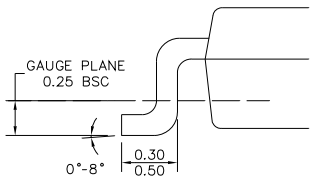
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

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1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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