

Ultra-Low Jitter 156.25 MHz LVDS XO

Features

- 156.25 MHz LVDS
- Typical Phase Noise:
 - 93 fs (Integration Range: 1.875 MHz to 20 MHz)
- ± 25 ppm Total Frequency Stability
- -40°C to +85°C Temperature Range
- Industry Standard 6-Lead 7 mm x 5 mm LGA Package

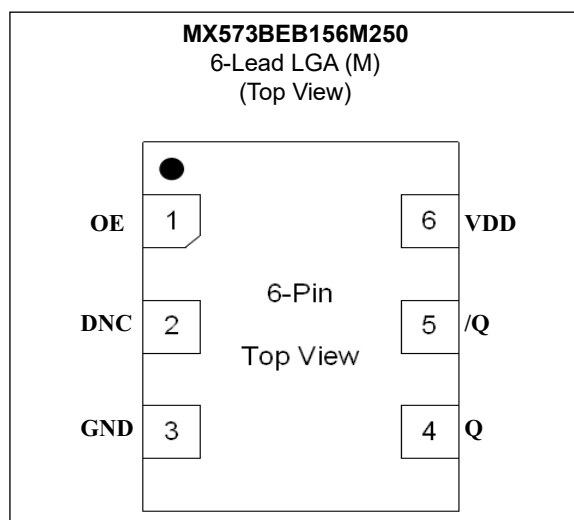
Applications

- 10/40/100 Gigabit Ethernet
- Fibre Channel 10G/12G SERDES

General Description

The MX573BEB156M250 is an ultra-low phase jitter XO with LVDS output that is optimized for high line rate applications.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN})	+4.6V
ESD (Machine Model)	200V
ESD (HBM)	2 kV

Operating Ratings ‡

Supply Voltage (V_{IN})	+2.375V to +3.63V
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† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 2.375$ to $3.63V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, outputs terminated with 100Ω between Q and /Q. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current	I_{DD}	—	90	100	mA	—
Center Frequency	f_0	—	156.25	—	MHz	—
Frequency Stability	f_{STAB}	—	—	± 25	ppm	Note 2
Phase Noise	δ_j	—	162	—	fsRMS	Integration Range (12 kHz to 20 MHz)
		—	93	—		Integration Range (1.875 MHz to 20 MHz)
Start-Up Time	t_{START}	—	—	20	ms	—
Rise/Fall Time	t_r/t_f	100	—	400	ps	—
Duty Cycle	—	45	—	55	%	—
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	LVDS output levels, $V_{OH(MAX)} = V_{CM(MAX)} + 1/2V_{OD(MAX)}$
Output Low Voltage	V_{OL}	0.898	1.025	1.252	V	LVDS output levels, $V_{OL(MIN)} = V_{CM(MIN)} - 1/2V_{OD(MAX)}$
Output Differential Voltage	V_{OD}	247	350	454	mV	—
Common Mode Output Voltage	V_{CM}	1.125	1.2	1.375	V	—

Note 1: Ensured after thermal equilibrium.

2: Inclusive of initial accuracy, supply voltage, temperature drift, aging (5yrs), shock, and vibration.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	-65	—	+125	$^{\circ}C$	—
Lead Temperature	T_{LEAD}	—	—	+260	$^{\circ}C$	Soldering, 10 sec.
Case Temperature	T_{CASE}	—	—	+115	$^{\circ}C$	—
Ambient Temperature Range	T_A	-40	—	+85	$^{\circ}C$	—
Package Thermal Resistances						
Thermal Resistance, LGA 6-Ld	θ_{JC}	—	53	—	$^{\circ}C/W$	Still-Air

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Pin Level	Description
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50 k Ω Pull-Up (Internal)
2	DNC	—	—	Make no connection, leave floating.
3	GND	PWR	—	Power Supply Ground
4, 5	Q, /Q	O, Diff	LVDS	Clock Output Frequency = 156.25 MHz
6	VDD	PWR	—	Power Supply

ENVIRONMENTAL SPECIFICATIONS

Specification	Standard
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free/RoHS/Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, $R1=2 \times 10^{-8}$ atm cc/s
MSL Level	Crystal - MSL-1, Package MSL-3
Solvent Resistance	MIL-STD-202, Method 215

3.0 PHASE NOISE PLOTS

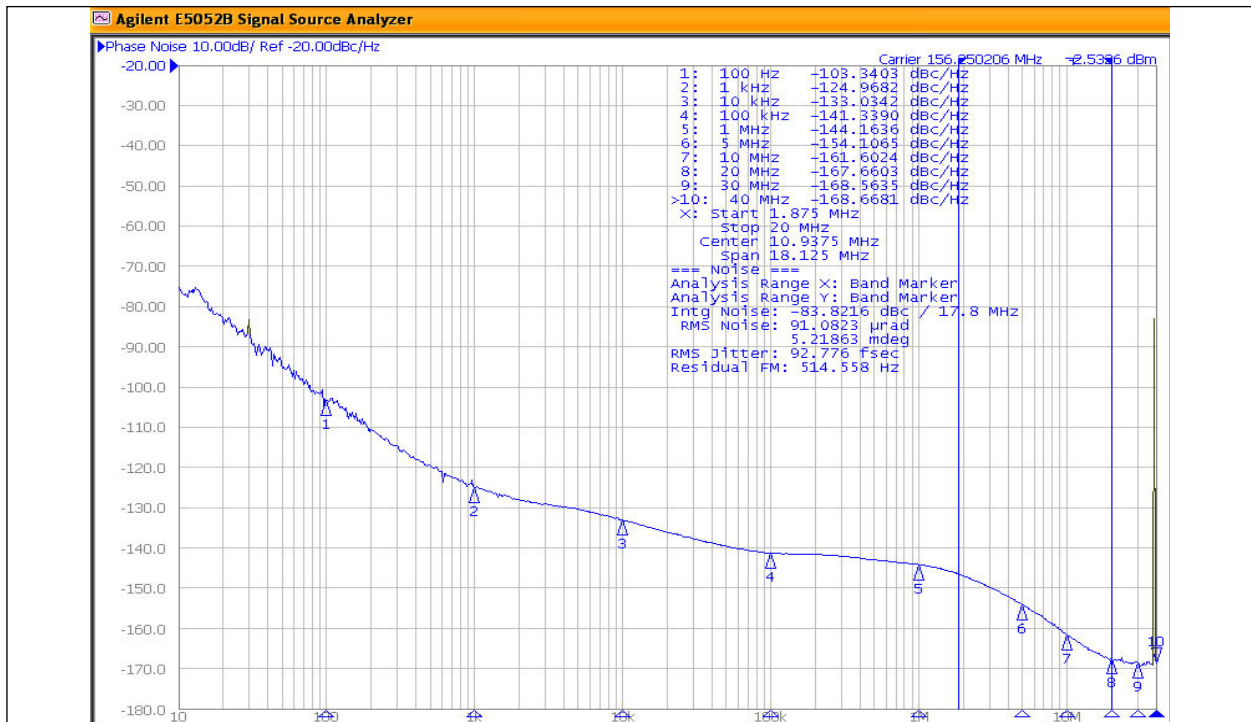


FIGURE 3-1: LVDS Output 156.25 MHz (1.875 MHz to 20 MHz) 93 fs.

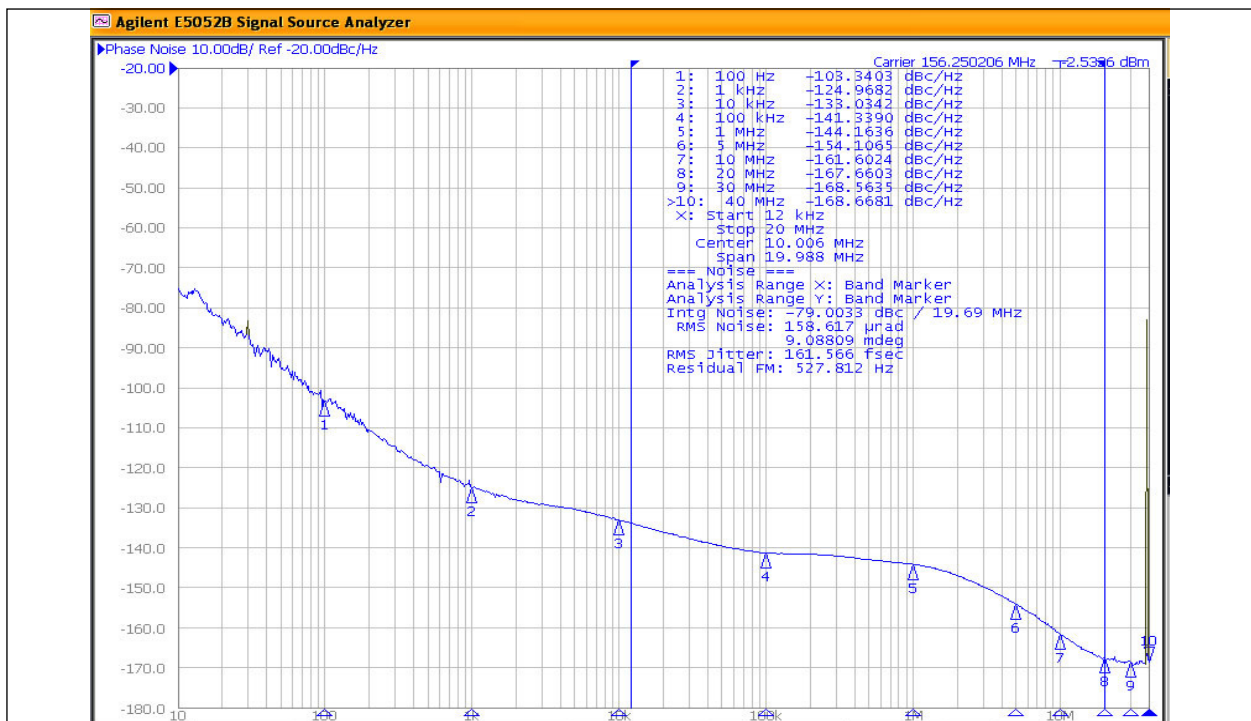
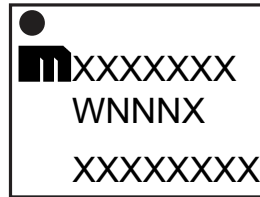


FIGURE 3-2: LVDS Output 156.25 MHz (12 kHz to 20 MHz) 162 fs.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

6-Lead LGA*



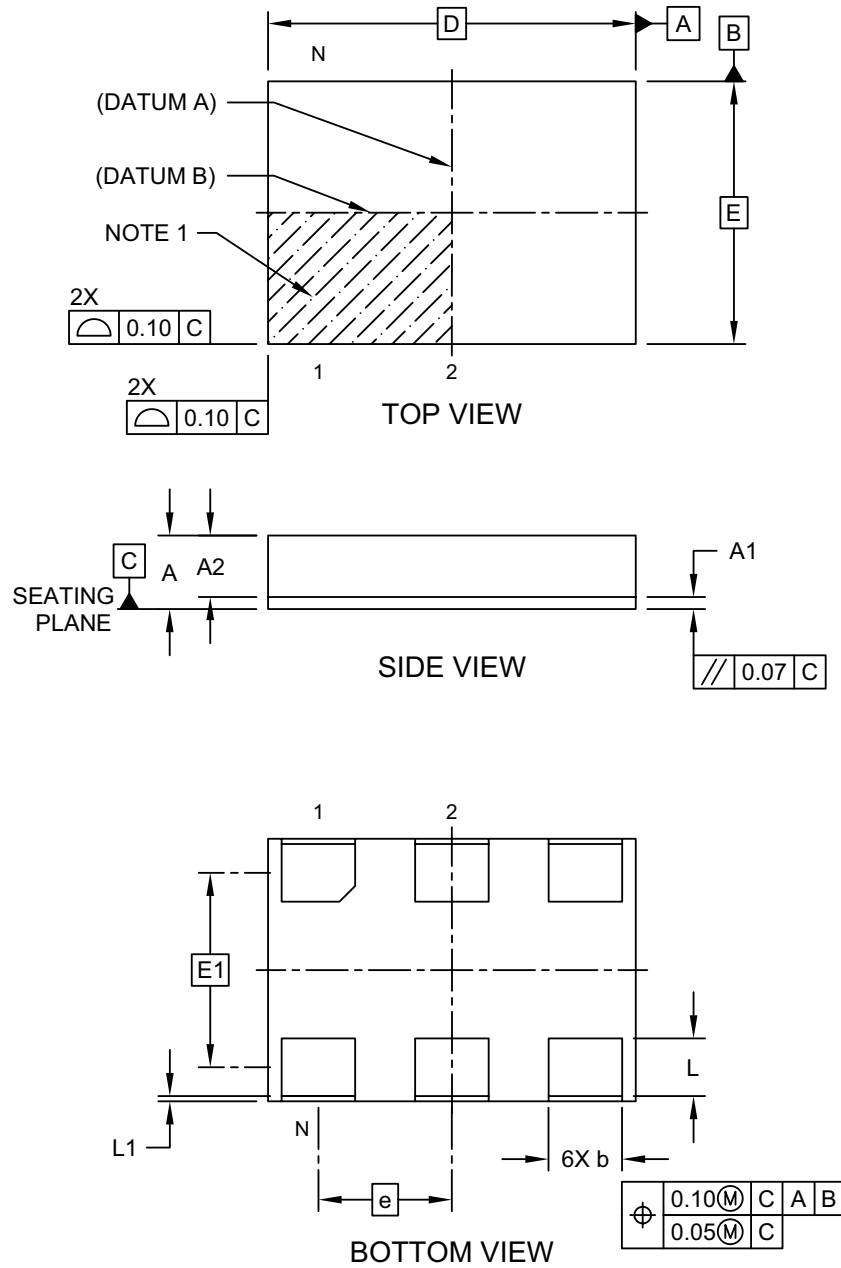
Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

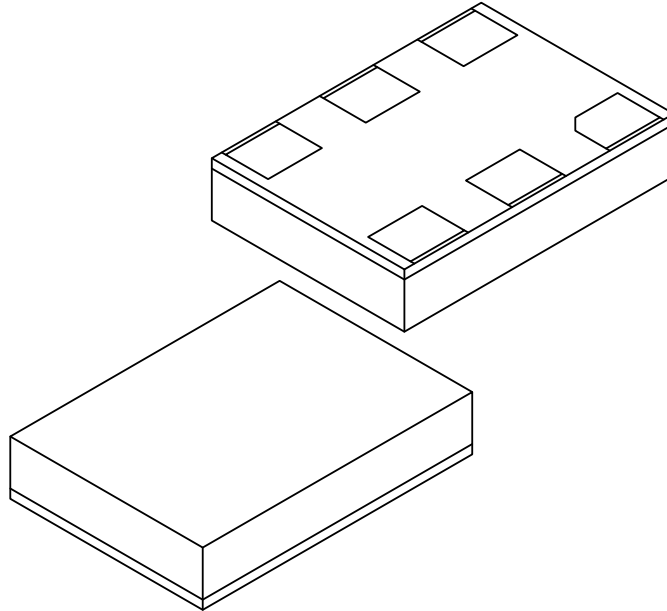


Microchip Technology Drawing C04-1071A Sheet 1 of 2

MX573BEB156M250

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	2.54 BSC		
Overall Height	A	1.26	1.33	1.40
Substrate Thickness	A1	0.19	0.23	0.27
Mold Cap Thickness	A2	1.07	1.10	1.13
Overall Length	D	7.00 BSC		
Pitch	E1	3.70 BSC		
Overall Width	E	5.00 BSC		
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.05	1.10	1.15
Pullback	L1	0.05	0.10	0.15

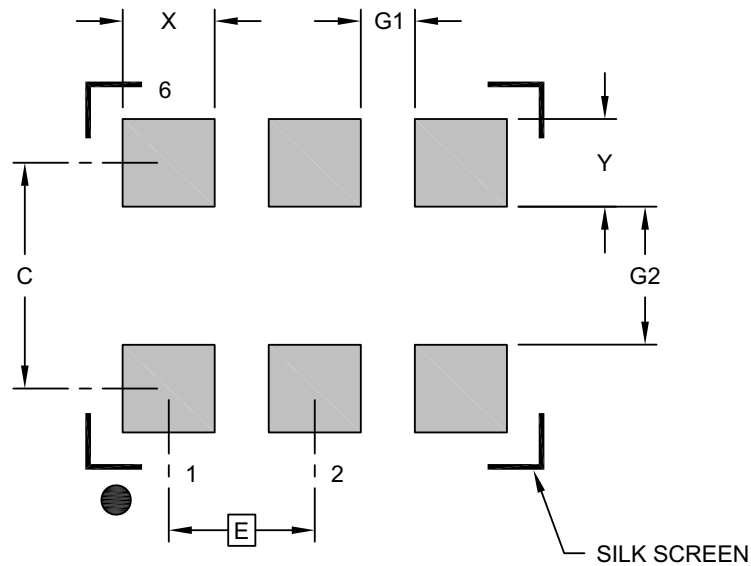
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1071A Sheet 2 of 2

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.54 BSC		
Contact Pad Spacing	C		3.93	
Contact Pad Width (X6)	X			1.60
Contact Pad Length (X6)	Y			1.53
Contact to Contact (X4)	G1	0.94		
Contact to Contact (X3)	G2	2.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3071A

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Converted Micrel document MX573BEB156M250 to Microchip data sheet template DS20006882A.
- Minor text changes throughout.

MX573BEB156M250

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part No.</u>	<u>XX</u>	<u>X</u>	<u>X</u>	<u>XXXMXXX</u>	<u>[-XX]</u>	Examples:
Device	Crystal Frequency	Stability	Output Logic	Output Frequency	Media Type	
Device:	MX57:	3.3V/5V 800 MHz LVTTTL/LVCMOS-to-Differential LVPECL Translator				a) MX573BEB156M250: MX57, 39.06250 MHz Crystal Frequency, ±25 ppm Stability, LVDS Output Logic, 156.25 MHz Output Frequency, Tube
Crystal Frequency:	3B	=	39.06250 MHz			b) MX573BEB156M250-TR: MX57, 39.06250 MHz Crystal Frequency, ±25 ppm Stability, LVDS Output Logic, 156.25 MHz Output Frequency, Tape & Reel
Stability:	E	=	±25 ppm			Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Output Logic:	B	=	LVDS			
Output Frequency:	156M250	=	156.25 MHz			
Media Type:	<blank> TR	= =	Tube Tape & Reel			

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