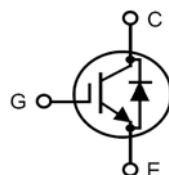


XPT™ 650V GenX4™ IXXR110N65B4H1 w/ Sonic Diode

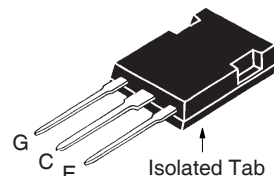
(Electrically Isolated Tab)

Extreme Light Punch Through
IGBT for 10-30kHz Switching



$$\begin{aligned} V_{CES} &= 650V \\ I_{C110} &= 70A \\ V_{CE(sat)} &\leq 2.10V \\ t_{fi(typ)} &= 43ns \end{aligned}$$

ISOPLUS247™



G = Gate C = Collector
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C}$ to 175°C	650	V
V_{CGR}	$T_J = 25^\circ\text{C}$ to 175°C , $R_{GE} = 1M\Omega$	650	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$ (Chip Capability)	165	A
I_{C110}	$T_C = 110^\circ\text{C}$	70	A
I_{F110}	$T_C = 110^\circ\text{C}$	48	A
I_{CM}	$T_C = 25^\circ\text{C}$, 1ms	490	A
SSOA (RBSOA)	$V_{GE} = 15V$, $T_{VJ} = 150^\circ\text{C}$, $R_G = 2\Omega$ Clamped Inductive Load	$I_{CM} = 220$ @ $V_{CE} \leq V_{CES}$	A
t_{sc} (SCSOA)	$V_{GE} = 15V$, $V_{CE} = 360V$, $T_J = 150^\circ\text{C}$ $R_G = 82\Omega$, Non Repetitive	10	μs
P_C	$T_C = 25^\circ\text{C}$	455	W
T_J		-55 ... +175	$^\circ\text{C}$
T_{JM}		175	$^\circ\text{C}$
T_{stg}		-55 ... +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_C	Mounting Force	20..120/4.5..27	N/lb
Weight		5	g

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Optimized for 10-30kHz Switching
- Square RBSOA
- Short Circuit Capability
- Anti-Parallel Sonic Diode
- High Current Handling Capability

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts
- High Frequency Power Inverters

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu\text{A}$, $V_{GE} = 0V$	650		V
$V_{GE(th)}$	$I_C = 250\mu\text{A}$, $V_{CE} = V_{GE}$	4.0		6.5 V
I_{CES}	$V_{CE} = V_{CES}$, $V_{GE} = 0V$ $T_J = 150^\circ\text{C}$			25 μA 3 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 110A$, $V_{GE} = 15V$, Note 1 $T_J = 150^\circ\text{C}$	1.72 2.05		2.10 V V

Symbol Test Conditions

(T_J = 25°C Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

g_{fs}	I _C = 60A, V _{CE} = 10V, Note 1	30	52	S
C_{ies}	V _{CE} = 25V, V _{GE} = 0V, f = 1MHz		5500	pF
C_{oes}			470	pF
C_{res}			80	pF
Q_{g(on)}	I _C = 110A, V _{GE} = 15V, V _{CE} = 0.5 • V _{CES}		183	nC
Q_{ge}			32	nC
Q_{gc}			83	nC
t_{d(on)}	Inductive load, T_J = 25°C I _C = 55A, V _{GE} = 15V V _{CE} = 400V, R _G = 2Ω Note 2		26	ns
t_{ri}			40	ns
E_{on}			2.20	mJ
t_{d(off)}			146	ns
t_{fi}			43	ns
E_{off}			1.05	1.70 mJ
t_{d(on)}	Inductive load, T_J = 150°C I _C = 55A, V _{GE} = 15V V _{CE} = 400V, R _G = 2Ω Note 2		25	ns
t_{ri}			40	ns
E_{on}			3.00	mJ
t_{d(off)}			140	ns
t_{fi}			110	ns
E_{off}			2.16	mJ
R_{thJC}				0.33 °C/W
R_{thCS}			0.15	°C/W

Reverse Sonic Diode (FRD)

Symbol Test Conditions

(T_J = 25°C Unless Otherwise Specified)

Characteristic Values

Min. Typ. Max.

V_F	I _F = 100A, V _{GE} = 0V, Note 1	T _J = 150°C	1.7	2.3	V
			1.8		V
I_{RM}	I _F = 100A, V _{GE} = 0V, -di _F /dt = 1500A/μs, V _R = 300V	T _J = 150°C	95		A
t_{rr}			100		ns
R_{thJC}				0.70	°C/W

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Switching times & energy losses may increase for higher V_{CE}(Clamp), T_J or R_G.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

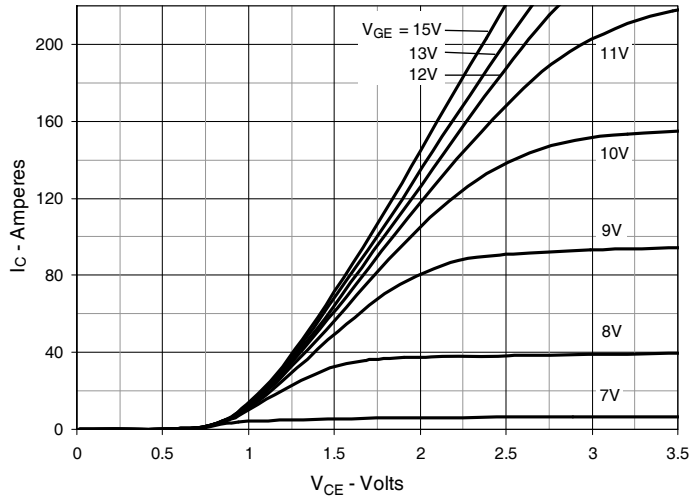


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

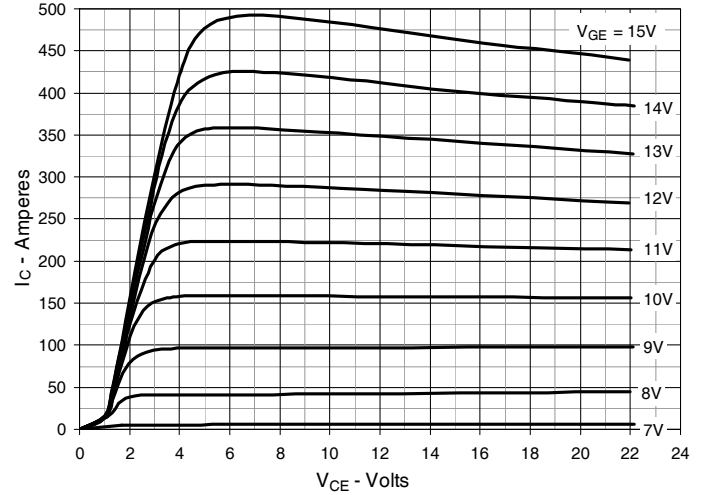


Fig. 3. Output Characteristics @ $T_J = 150^\circ\text{C}$

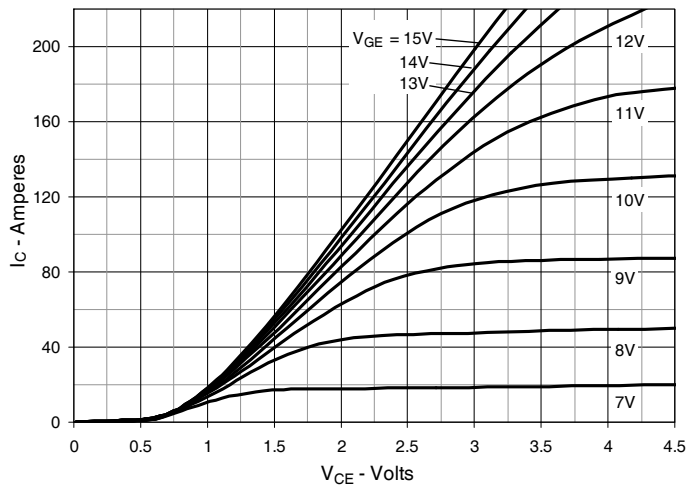


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

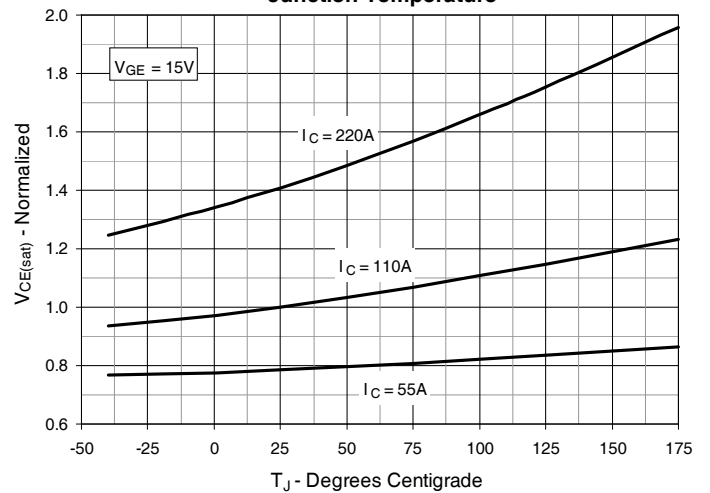


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

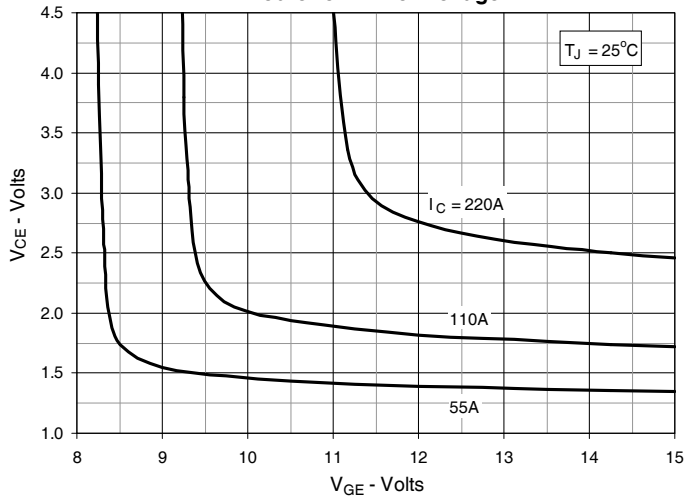


Fig. 6. Input Admittance

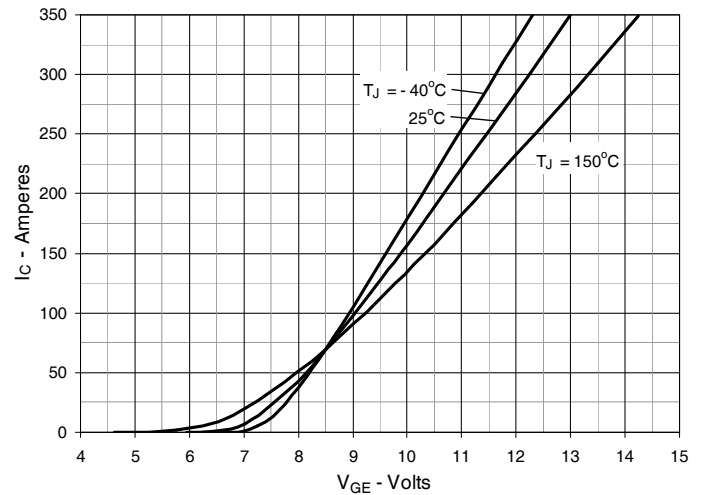


Fig. 7. Transconductance

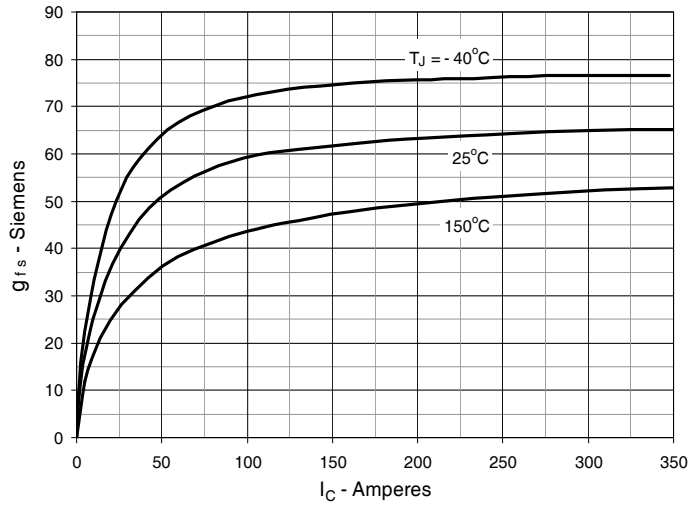


Fig. 8. Gate Charge

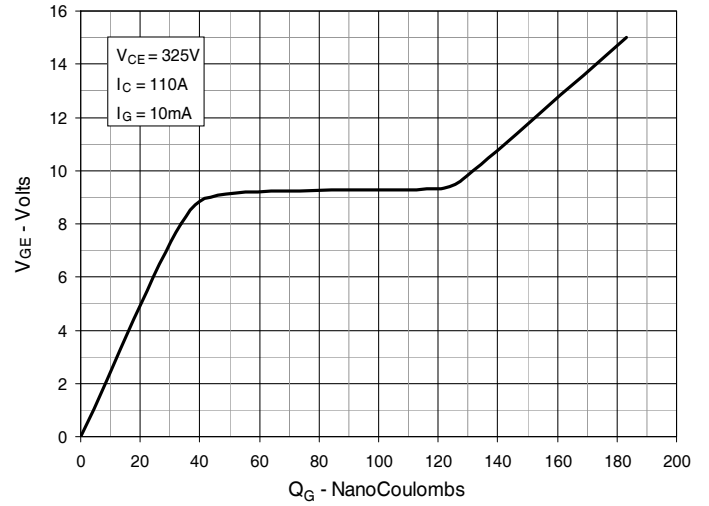


Fig. 9. Capacitance

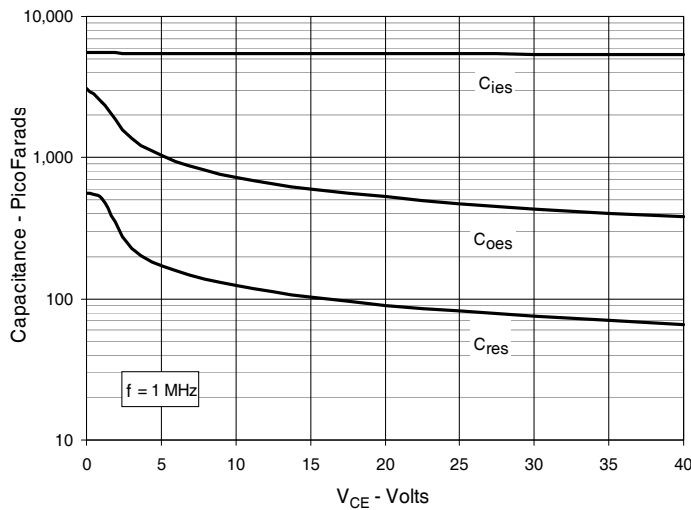


Fig. 10. Reverse-Bias Safe Operating Area

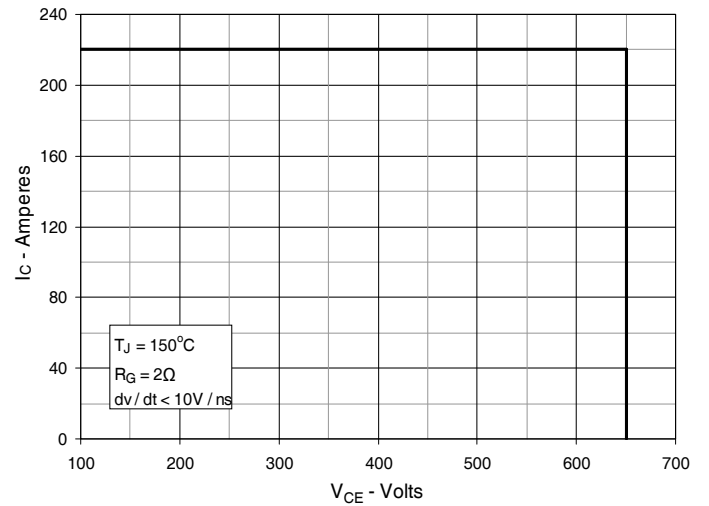


Fig. 11. Maximum Transient Thermal Impedance (IGBT)

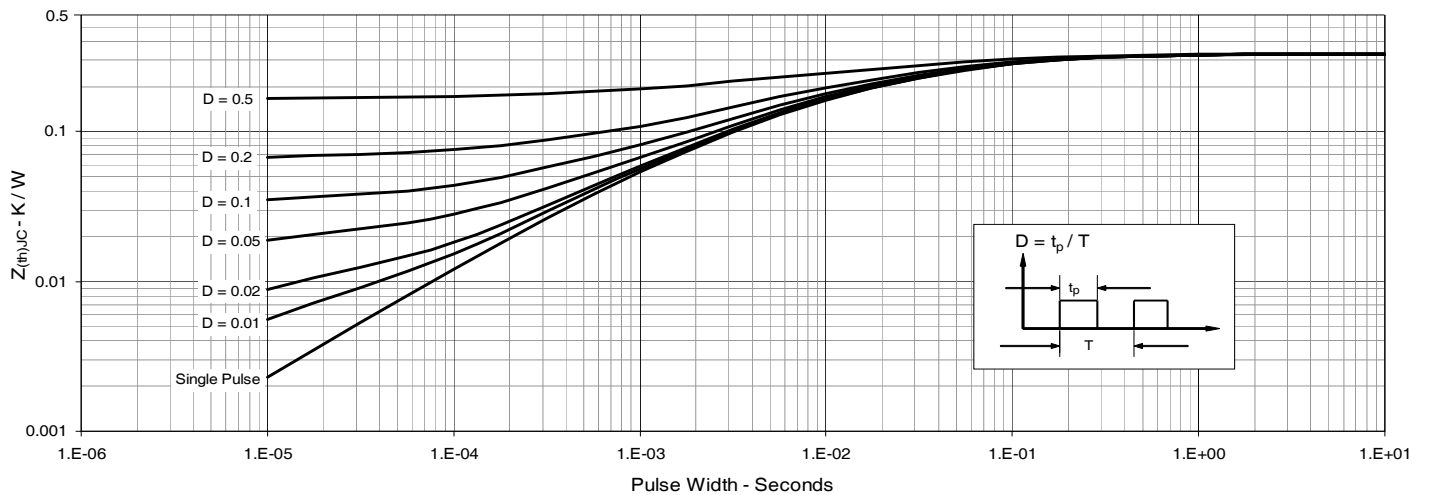


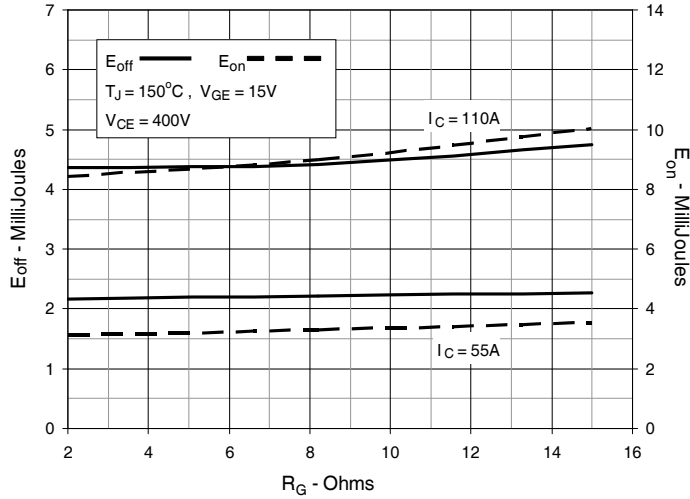
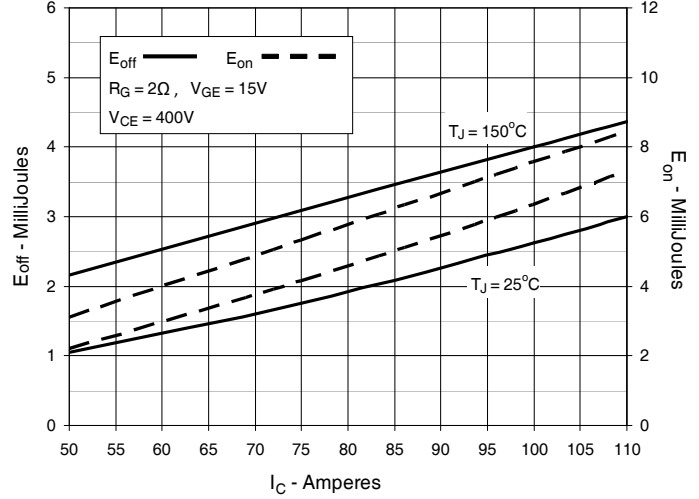
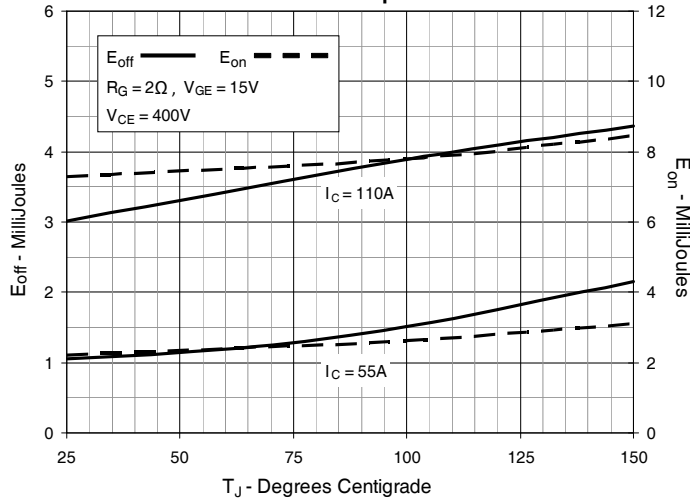
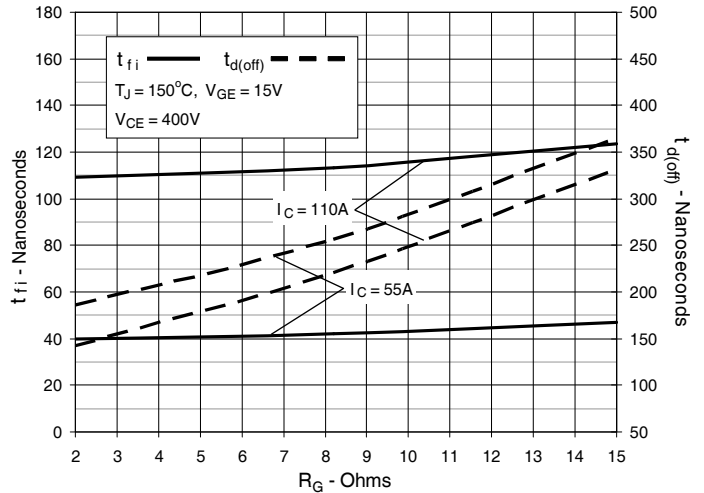
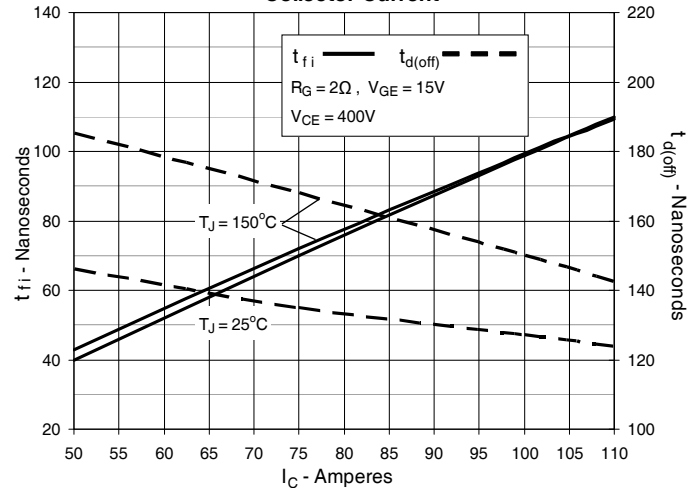
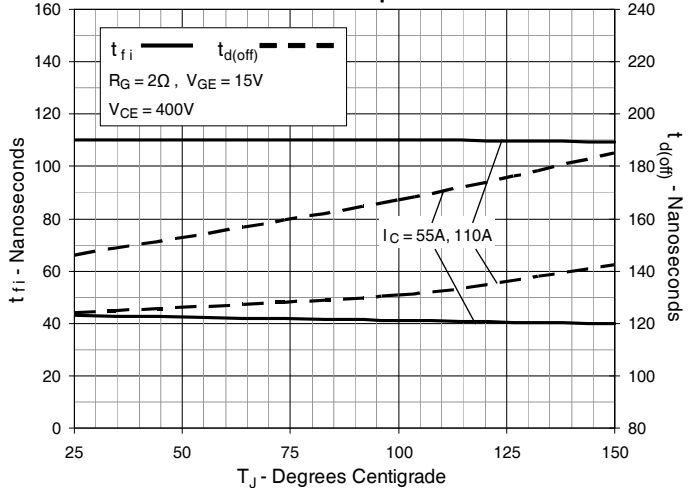
Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

Fig. 13. Inductive Switching Energy Loss vs. Collector Current

Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature

Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature


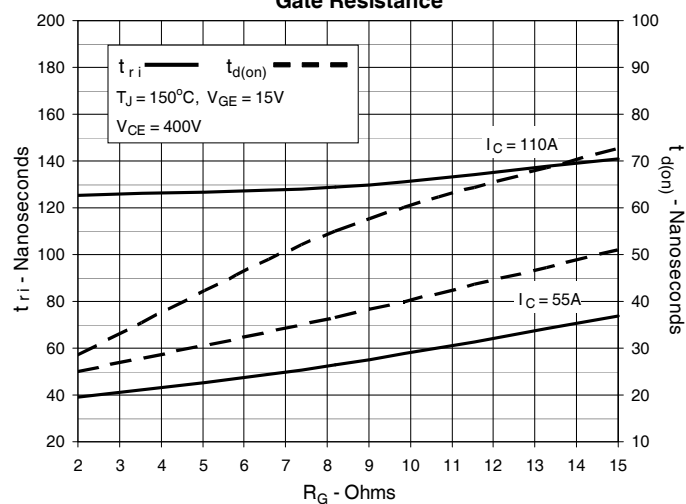
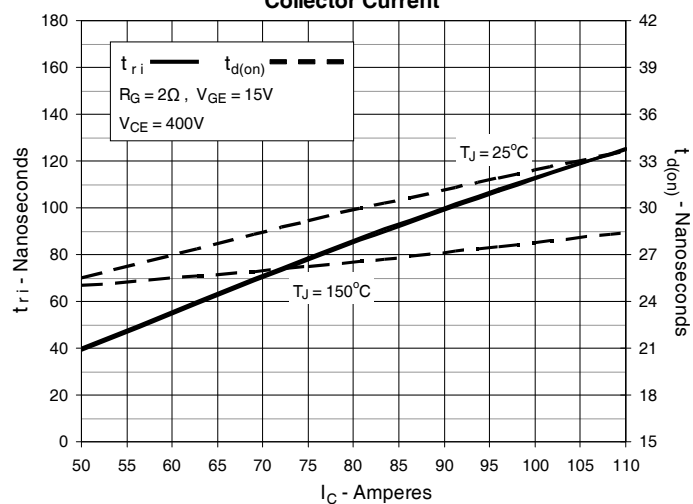
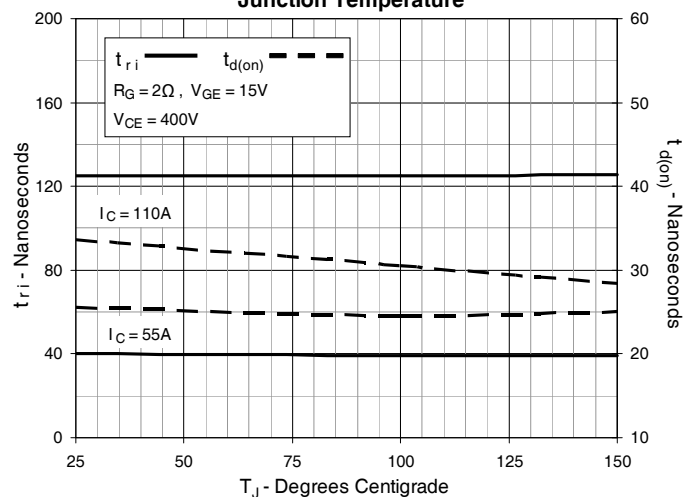
Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature


Fig. 21. Typ. Forward characteristics

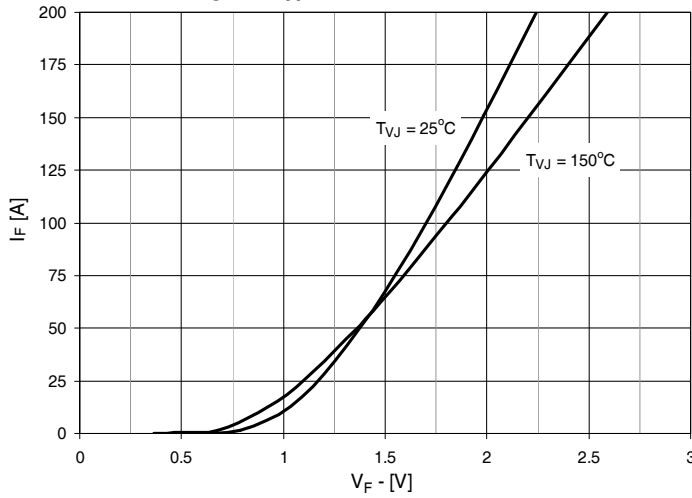


Fig. 22. Typ. Reverse Recovery Charge Q_{rr} vs. $-di_F/dt$

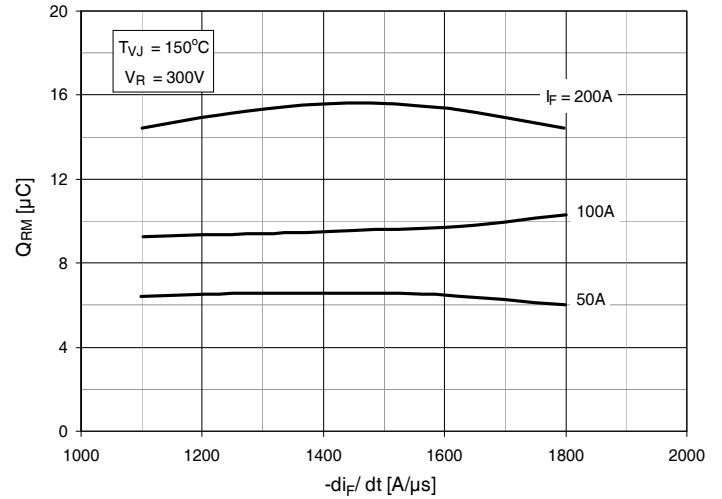


Fig. 23. Typ. Peak Reverse Current I_{RM} vs. $-di_F/dt$

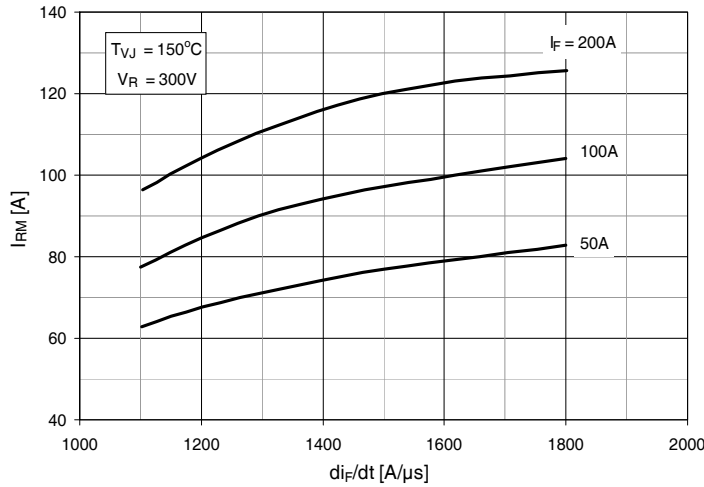


Fig. 24. Typ. Recovery Time t_{rr} vs. $-di_F/dt$

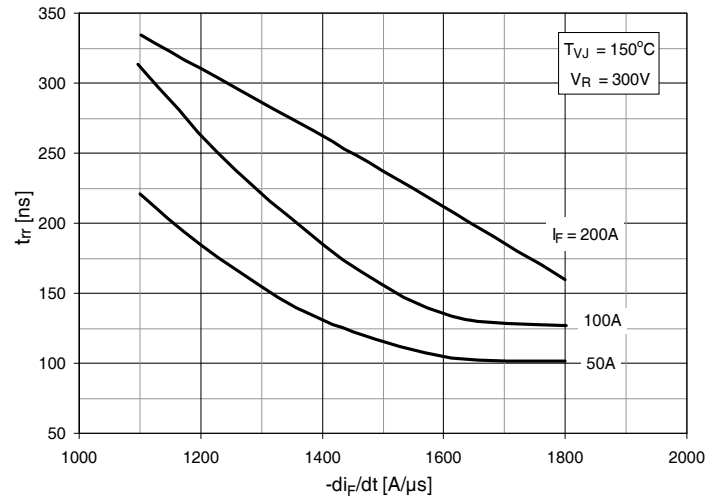


Fig. 25. Typ. Recovery Energy E_{rec} vs. $-di_F/dt$

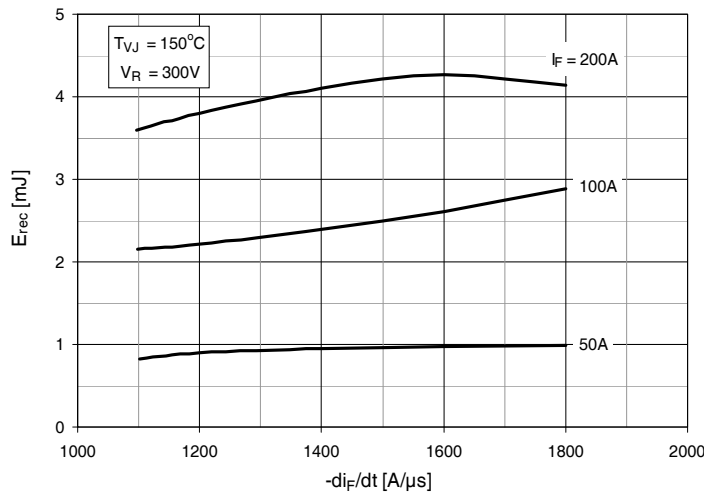
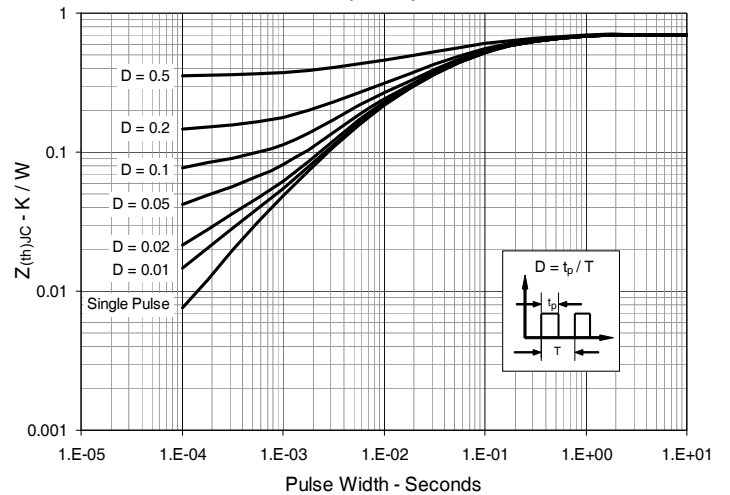
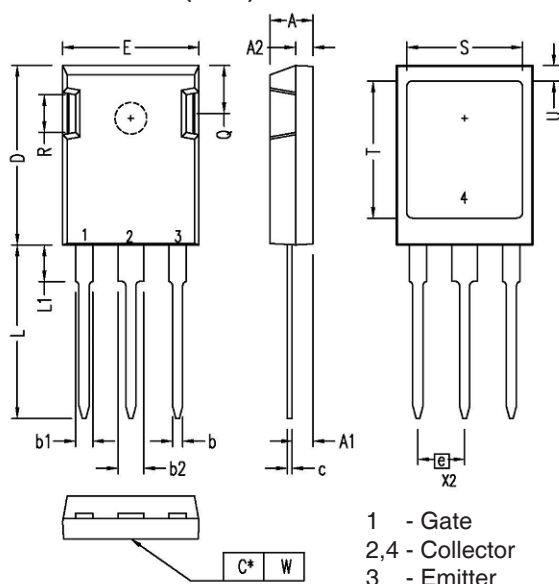


Fig. 26. Maximum Transient Thermal Impedance (Diode)



ISOPLUS247 (IXXR) Outline


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.085	1.91	2.15
b2	.115	.126	2.92	3.20
C	.024	.033	0.61	0.83
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.811	19.81	20.60
L1	.150	.172	3.81	4.38
Q	.220	.244	5.59	6.20
R	.170	.191	4.32	4.85
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03
W	0	.004	0	0.10

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.
 C* - Convex bow of substrate is typ<0.04mm over plastic surface level of device bottom side.
 LEAD FINISH - External leads are Pb free solder dip.

