

**MOSFET – N-Channel,  
Shielded Gate,  
POWERTRENCH®****60 V, 2.6 A, 116 mΩ****FDN86501LZ****General Description**

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

**Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)} = 116 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 2.6 \text{ A}$
- Max  $r_{DS(on)} = 173 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 2.1 \text{ A}$
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

**Applications**

- Primary DC-DC Switch
- Load Switch

**MOSFET MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

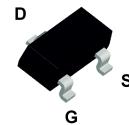
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Continuous (Note 1a)	2.6	A
	Pulsed (Note 4)	24	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	6	mJ
$P_D$	Power Dissipation (Note 1a)	1.5	W
	(Note 1b)	0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta,JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ\text{C/W}$
$R_{\theta,JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	80	$^\circ\text{C/W}$

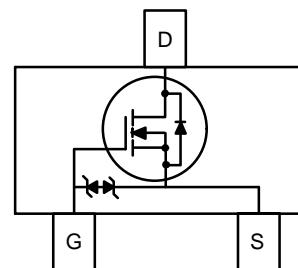
$V_{DS}$	$r_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	116 mΩ @ 10 V	2.6 A
	173 mΩ @ 4.5 V	



**SOT-23/SUPERSOT™-23, 3 LEAD, 1.4x2.9  
CASE 527AG**

**MARKING DIAGRAM**

8650 = Specific Device Code  
M = Date Code

**PIN ASSIGNMENT****ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

# FDN86501LZ

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60	—	—	V
$\frac{\Delta \text{BV}_{\text{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	—	68	—	$\text{mV}/^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 2)

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.0	1.9	2.4	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	—	-5	—	$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.6 \text{ A}$	—	89	116	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 2.1 \text{ A}$	—	121	173	
		$V_{GS} = 10 \text{ V}, I_D = 2.6 \text{ A}, T_J = 125^\circ\text{C}$	—	152	198	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 2.6 \text{ A}$	—	8	—	S

### DYNAMIC CHARACTERISTICS

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	236	335	pF
$C_{\text{oss}}$	Output Capacitance		—	77	110	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		—	4.9	10	pF
$R_g$	Gate Resistance		0.1	0.8	2.0	$\Omega$

### SWITCHING CHARACTERISTICS (Note 2)

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 2.6 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$	—	4.4	10	ns
$t_r$	Rise Time		—	1.2	10	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		—	9.6	20	ns
$t_f$	Fall Time		—	1.2	10	ns
$Q_g$		$V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}$ $V_{DD} = 30 \text{ V}, I_D = 2.6 \text{ A}$	—	3.8	5.4	nC
$Q_g$			—	1.9	2.7	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 30 \text{ V}, I_D = 2.6 \text{ A}$	—	0.7	—	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		—	0.6	—	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

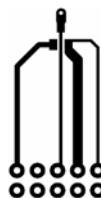
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.6 \text{ A}$ (Note 2)	—	0.9	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2.6 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	—	31	50	ns
$Q_{rr}$	Reverse Recovery Charge		—	19	31	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $80^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b.  $180^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%.

3.  $E_{AS}$  of 6 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3 \text{ mH}$ ,  $I_{AS} = 2 \text{ A}$ ,  $V_{DD} = 60 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ , 100% test at  $L = 0.1 \text{ mH}$ ,  $I_{AS} = 9 \text{ A}$ .

4. Pulsed  $I_d$  please refer to Figure 11 SOA graph for more details.

## TYPICAL CHARACTERISTICS

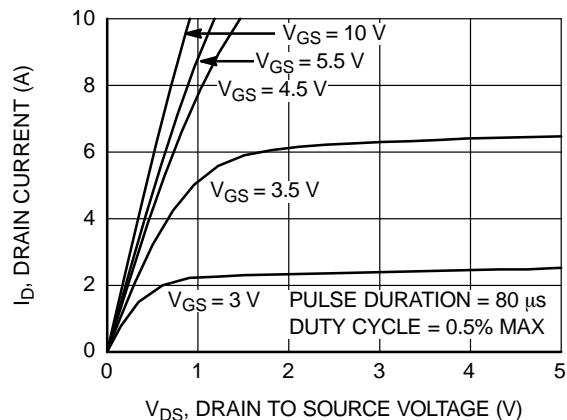
 $(T_J = 25^\circ\text{C}$  unless otherwise noted)

Figure 1. On-Region Characteristics

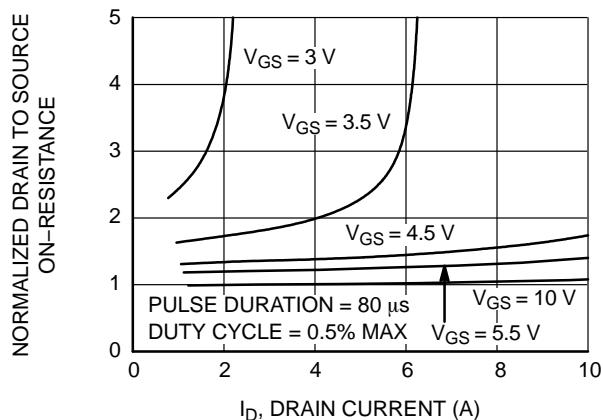


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

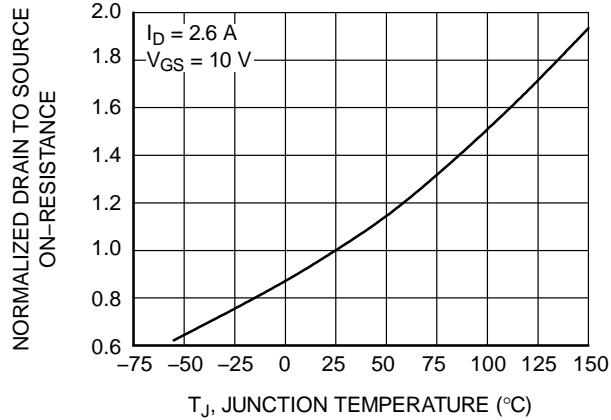


Figure 3. Normalized On-Resistance vs. Junction Temperature

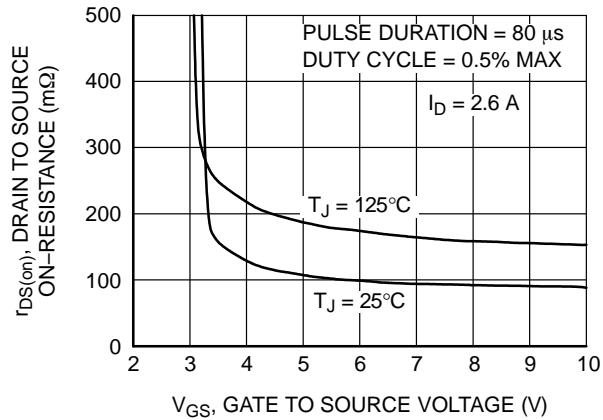


Figure 4. On-Resistance vs. Gate to Source Voltage

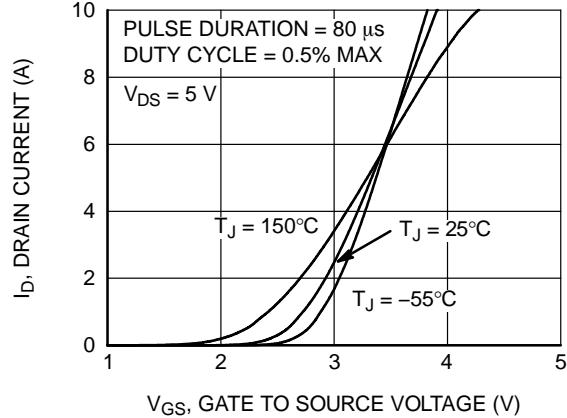


Figure 5. Transfer Characteristics

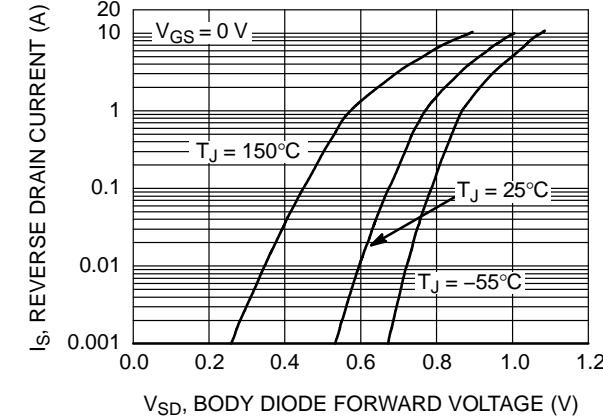
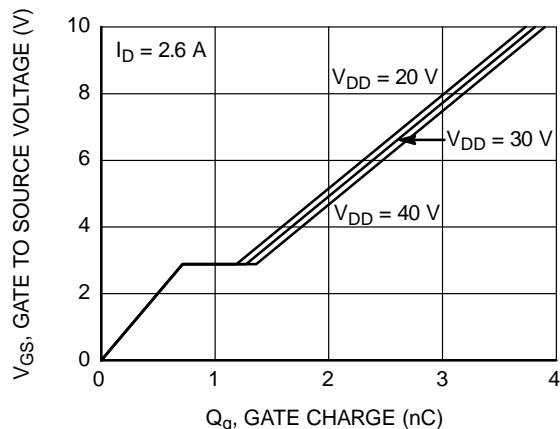


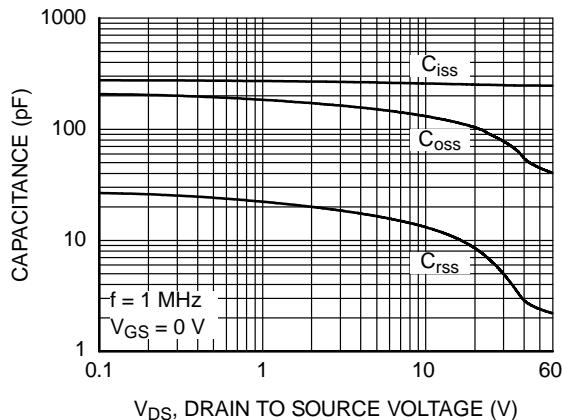
Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

**TYPICAL CHARACTERISTICS**

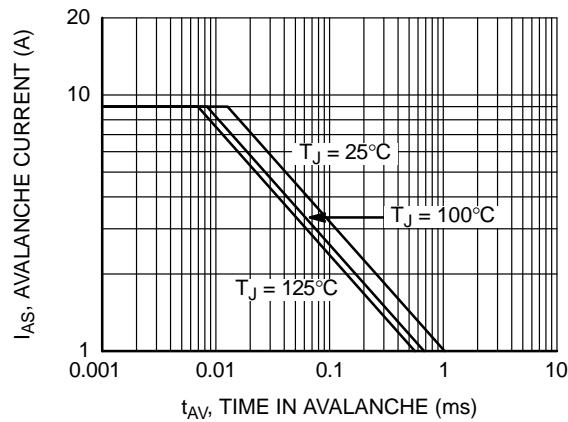
( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)



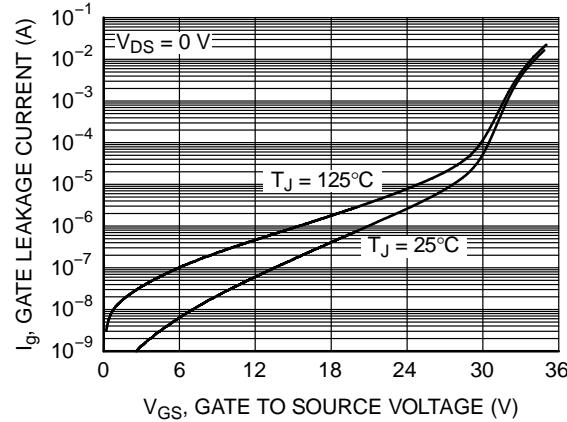
**Figure 7. Gate Charge Characteristics**



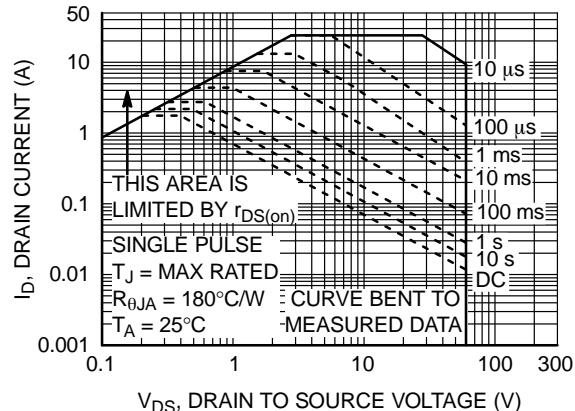
**Figure 8. Capacitance vs. Drain to Source Voltage**



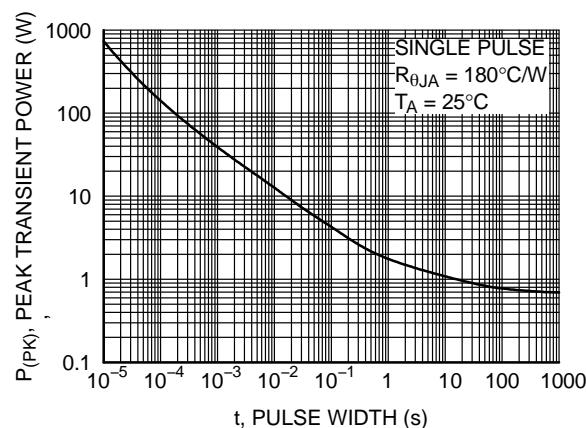
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Gate Leakage Current vs. Gate to Source Voltage**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS

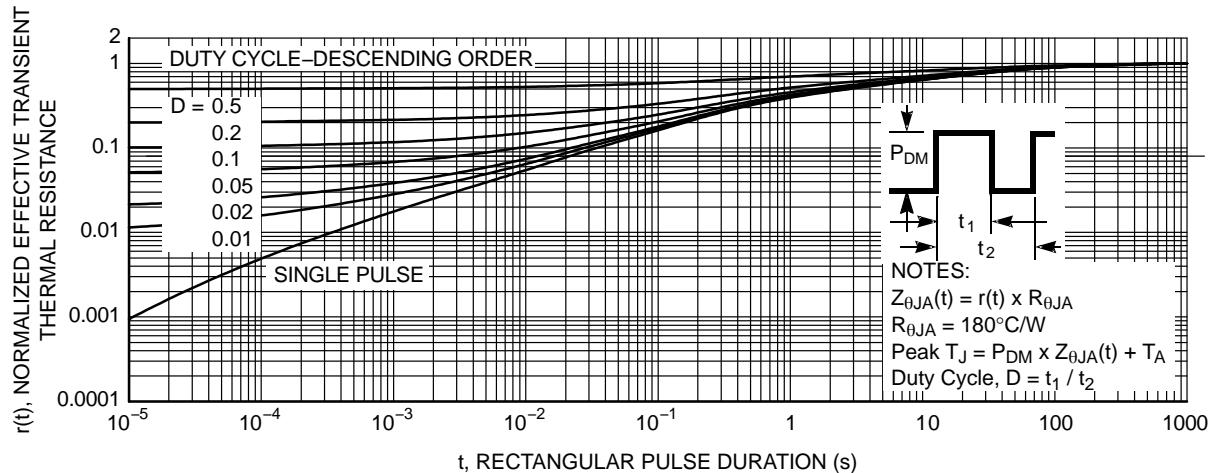
(T<sub>J</sub> = 25°C unless otherwise noted) (continued)

Figure 13. Junction-to-Ambient Transient Thermal Response Curve

## PACKAGE MARKING AND ORDERING INFORMATION

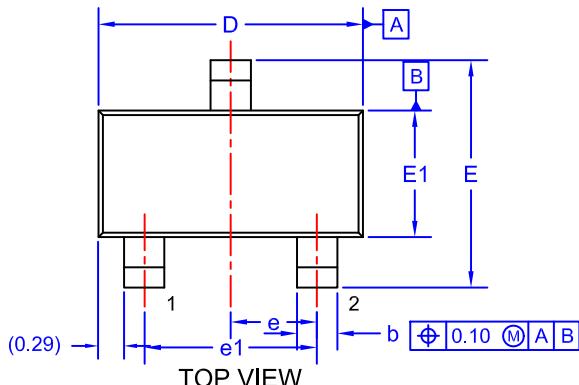
Device	Device Marking	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
FDN86501LZ	8650	SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9 (Pb-Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**SOT-23/SUPERSOT™-23, 3 LEAD, 1.4x2.9**  
CASE 527AG  
ISSUE A

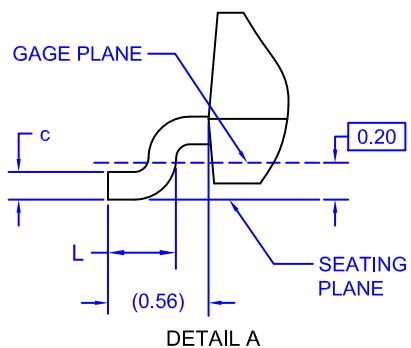
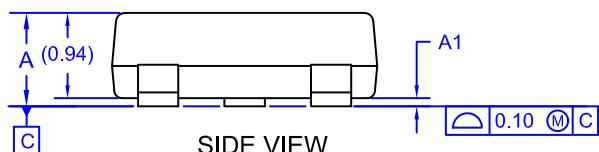
DATE 09 DEC 2019



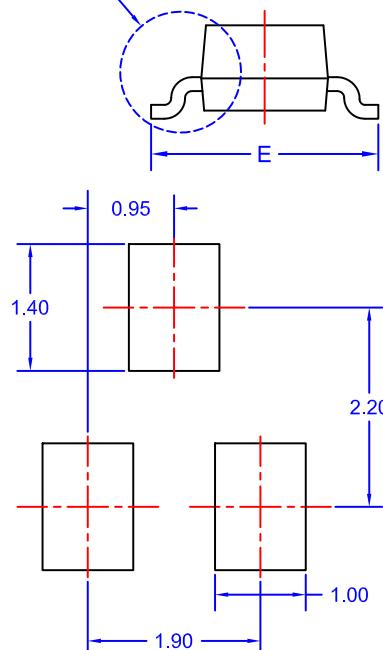
NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

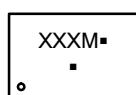


SEE DETAIL A



## LAND PATTERN RECOMMENDATION\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXX = Specific Device Code  
M = Month Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-23/SUPERSOT-23, 3 LEAD, 1.4X2.9	PAGE 1 OF 1

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