REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - LTG	05-02-07	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
Greg A. Pitz

DEFENSE SUPPLY CENTER COLUMBUS
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
N. A. Hauck

DRAWING APPROVAL DATE
87-08-10

REVISION LEVEL
A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, DUAL 4-INPUT MULTIPLEXER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

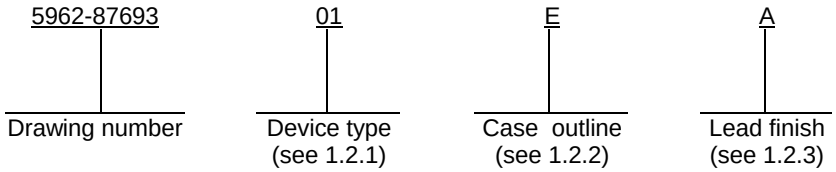
SIZE	CAGE CODE	
A	**67268**	**5962-87693**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC253	Dual 4-input multiplexer with three-state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering 10 seconds) ..... +245°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 4/

See footnotes on next sheet.

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC}) ..... +3.0 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall times:
V_{CC} = 3.6 V ..... 0 to 116 ns (10% to 90%, 40 ns/V)
V_{CC} = 5.5 V ..... 0 to 88 ns (10% to 90%, 20 ns/V)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.
5/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transition and no stored data loss with the following conditions: $V_{IH} \geq 70\%\ V_{CC}$, $V_{IL} \leq 30\%\ V_{CC}$, $V_{OH} \geq 70\%\ V_{CC}$ @ -20 µA, $V_{OL} \leq 30\%\ V_{CC}$ @ 20 µA.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage 1/	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ \mu A$	$V_{CC} = 3.0\ V$	1, 2, 3	All	2.9		V
			$V_{CC} = 4.5\ V$			4.4		
			$V_{CC} = 5.5\ V$			5.4		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4\ mA$	$V_{CC} = 3.0\ V$			2.4		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -24\ mA$	$V_{CC} = 4.5\ V$			3.7		
			$V_{CC} = 5.5\ V$			4.7		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ mA$	$V_{CC} = 5.5\ V$			3.85		
Low level output voltage 1/	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu A$	$V_{CC} = 3.0\ V$	1, 2, 3	All		0.1	V
			$V_{CC} = 4.5\ V$				0.1	
			$V_{CC} = 5.5\ V$				0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 12\ mA$	$V_{CC} = 3.0\ V$				0.5	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 24\ mA$	$V_{CC} = 4.5\ V$				0.5	
			$V_{CC} = 5.5\ V$				0.5	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ mA$	$V_{CC} = 5.5\ V$				1.65	
High level input voltage 2/	V_{IH}		$V_{CC} = 3.0\ V$	1, 2, 3	All	2.1		V
			$V_{CC} = 4.5\ V$			3.15		
			$V_{CC} = 5.5\ V$			3.85		
Low level input voltage 2/	V_{IL}		$V_{CC} = 3.0\ V$	1, 2, 3	All		0.9	V
			$V_{CC} = 4.5\ V$				1.35	
			$V_{CC} = 5.5\ V$				1.65	
Input leakage current low	I_{IL}	$V_{IN} = 0.0\ V$	$V_{CC} = 5.5\ V$	1, 2, 3	All		-1.0	µA
Input leakage current high	I_{IH}	$V_{IN} = 5.5\ V$					1.0	
Quiescent supply current, output high	I_{CCH}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5\ V$		1, 2, 3	All		160	µA
Quiescent supply current, output low	I_{CCL}						160	
Quiescent supply current, output three-state	I_{CCZ}						160	
Off-state output leakage current high	I_{OZH}	$V_{CC} = 5.5\ V$ $V_{IN} = V_{CC}$ or GND $V_{OUT} = 5.5\ V$ or $0.0\ V$		1, 2, 3	All		10.0	µA
Off-state output leakage current low	I_{OZL}						-10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input capacitance	C_{IN}	See 4.3.1c		4	All		8.0	pF
Power dissipation capacitance 3/	C_{PD}	See 4.3.1c		4	All		85.0	pF
Functional tests		Tested at V_{CC} = 3.0 V and repeated at V_{CC} = 5.5 V See 4.3.1d		7, 8	All	L	H	
Propagation delay time, In to Z 4/	t_{PHL1}	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	All	1.0	12.0	ns
				10, 11		1.0	15.0	
			V_{CC} = 4.5 V	9		1.0	9.0	
				10, 11		1.0	11.5	
	t_{PLH1}		V_{CC} = 3.0 V	9		1.0	13.0	
				10, 11		1.0	17.0	
			V_{CC} = 4.5 V	9		1.0	9.0	
				10, 11		1.0	11.5	
Propagation delay time, Sm to Z 4/	t_{PHL2}	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	All	1.0	15.0	ns
				10, 11		1.0	18.5	
			V_{CC} = 4.5 V	9		1.0	11.0	
				10, 11		1.0	13.5	
	t_{PLH2}		V_{CC} = 3.0 V	9		1.0	14.5	
				10, 11		1.0	18.0	
			V_{CC} = 4.5 V	9		1.0	10.5	
				10, 11		1.0	12.5	
Propagation delay time, output enable, $\overline{OE}$ to Z 4/	t_{PZH}	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	All	1.0	7.5	ns
				10, 11		1.0	9.0	
			V_{CC} = 4.5 V	9		1.0	6.0	
				10, 11		1.0	7.0	
	t_{PZL}		V_{CC} = 3.0 V	9		1.0	8.0	
				10, 11		1.0	9.5	
			V_{CC} = 4.5 V	9		1.0	6.0	
				10, 11		1.0	8.0	
Propagation delay time, output disable, $\overline{OE}$ to Z 4/	t_{PHZ}	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	All	1.0	9.0	ns
				10, 11		1.0	10.5	
			V_{CC} = 4.5 V	9		1.0	8.0	
				10, 11		1.0	9.0	
	t_{PLZ}		V_{CC} = 3.0 V	9		1.0	8.0	
				10, 11		1.0	9.5	
			V_{CC} = 4.5 V	9		1.0	7.0	
				10, 11		1.0	8.0	

See footnotes on next sheet.

TABLE I. Electrical performance characteristics – Continued.

1/ V_{OH} and V_{OL} tests will be tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V. All other voltages are guaranteed, but not tested. Limits shown apply to operation at V_{CC} = 3.3 V ±0.3 V and V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ V_{IH} and V_{IL} tests are guaranteed by the V_{OH} and V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}) determines both the dynamic power consumption (P_D) and the dynamic current consumption (I_S). Where

$P_D = (C_{PD} + C_L) (V_{CC}^2)f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$.

f is the frequency of the input signal and C_L is the external load capacitance.

4/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. AC limits at V_{CC} = 3.6 V are equal to the limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns.

Device type	All	
Case outlines	E and F	2
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{OEa}$	NC
2	S1	$\overline{OEa}$
3	I3a	S1
4	I2a	I3a
5	I1a	I2a
6	I0a	NC
7	Za	I1a
8	GND	I0a
9	Zb	Za
10	I0b	GND
11	I1b	NC
12	I2b	Zb
13	I3b	I0b
14	$\overline{S0}$	I1b
15	$\overline{OEb}$	I2b
16	V_{CC}	NC
17	---	I3b
18	---	$\overline{S0}$
19	---	$\overline{OEb}$
20	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Inputs							Output
S0	S1	I0	I1	I2	I3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance

FIGURE 2. Truth table.

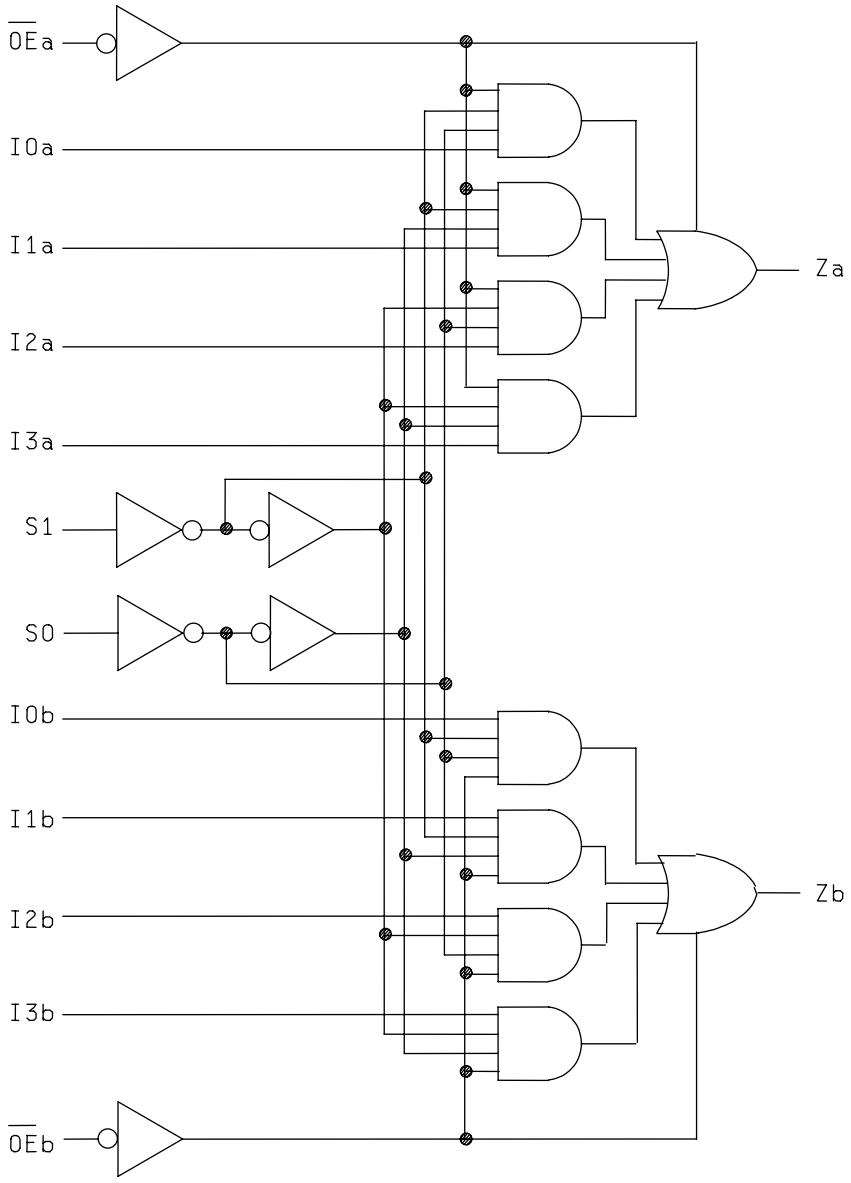


FIGURE 3. Logic diagram.

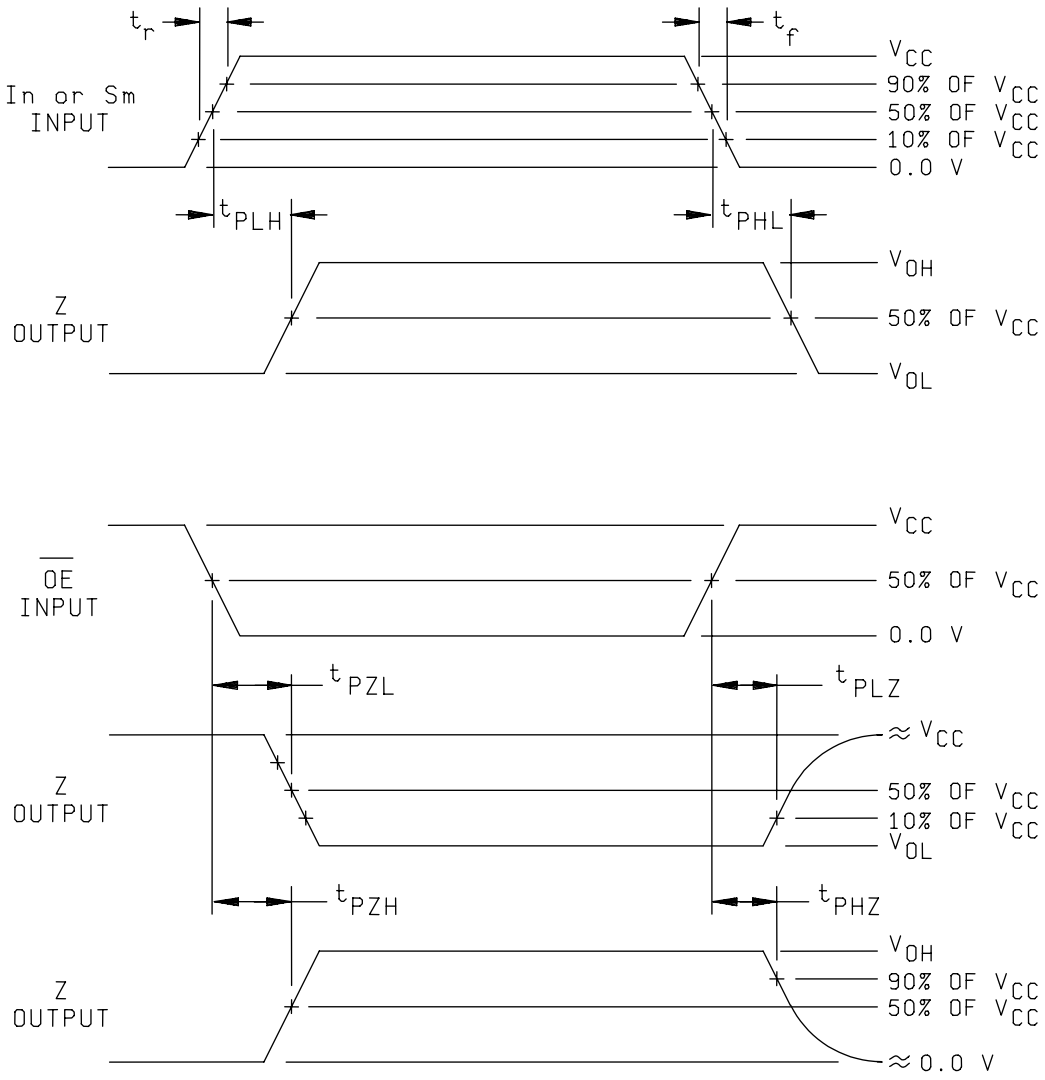
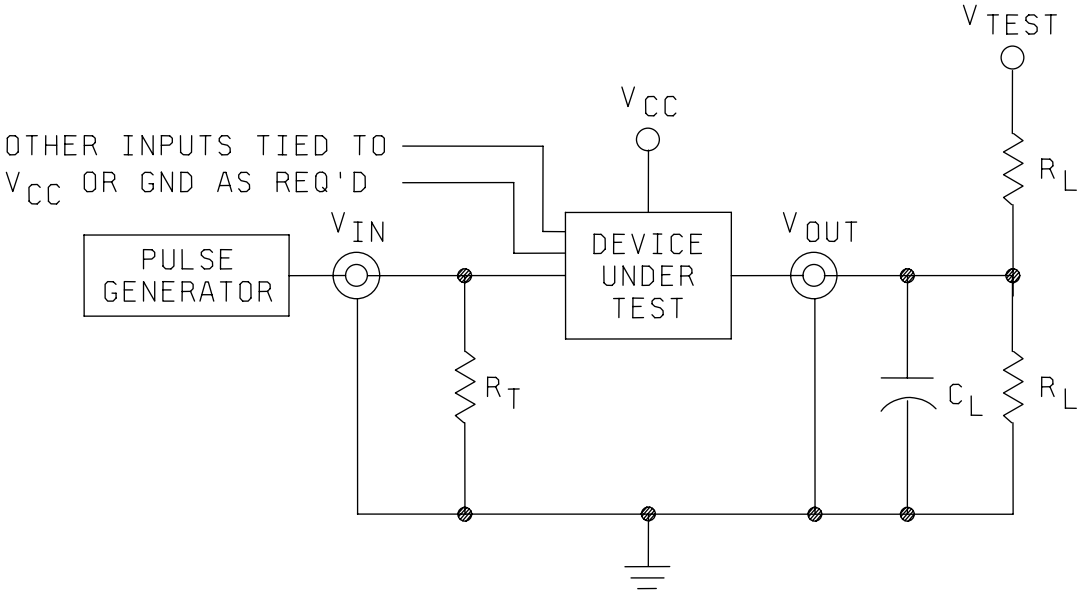


FIGURE 4. Switching waveforms and test circuit.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: $V_{TEST} = 2 \times V_{CC}$.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent; R_T = 50Ω or equivalent.
6. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; $t_r \leq 3.0$ ns; $t_f \leq 3.0$ ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
7. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
8. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-02-07

Approved sources of supply for SMD 5962-87693 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/SMCR/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8769301EA	27014	54AC253DMQB
5962-8769301FA	27014	54AC253FMQB
5962-87693012A	27014	54AC253LMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090