4 Line ESD/EMI Protection for Color LCD Interfaces
UM4401 *DFN8 2.1×1.6*

General Description

The UM4401 is a low pass filter array with integrated TVS diodes. It is designed to suppress unwanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes silicon-avalanche technology for superior clamping performance and DC electrical characteristics. It has been optimized for protection of color LCD panels in cellular phones and other portable electronics.
The device consists of four identical circuits comprised of TVS diodes for ESD protection, and a RC network for EMI filtering. A series resistor value of 100Ω and a capacitance value of 10pF are used to achieve 25dB minimum attenuation from 800 MHz to 2.5GHz. The TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±8kV (contact discharge) per IEC 61000-4-2, level 4.
The UM4401 is in a 8-pin, RoHS compliant DFN8 package. It measures 2.1mm×1.6mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free Ni Pd. The small package makes it ideal for use in portable electronics such as cell phones, digital still cameras, and PDAs.

Applications

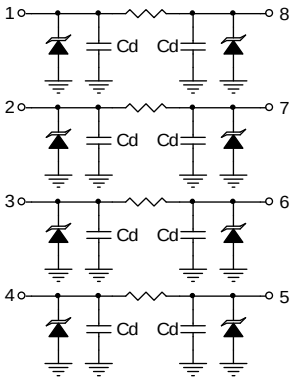
- EMI Filtering and ESD Protection for Data Lines
- Wireless Phones
- Handheld Products
- Notebook Computers
- LCD Displays

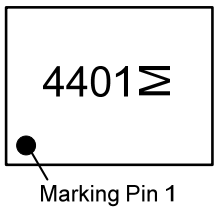
Features

- EMI/RFI Filter with Integrated TVS for ESD Protection
- ESD Protection to IEC 61000-4-2 (ESD) Level 4, ±15kV (Air), ±8kV (Contact)
- 25dB Minimum Attenuation: 800MHz to 2.5GHz
- Working Voltage: 5V
- Resistor: 100Ω ±15%
- Typical Capacitance: 10pF (V_R=2.5V)
- Solid-State Technology
- DFN8 Package: 2.1mm×1.6 mm
- Moisture Sensitivity Level 1

Pin Configurations

Top View





M: Month Code
UM4401
DFN8 2.1×1.6

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM4401	DFN8 2.1×1.6	4401	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Unit
T_J	Junction Temperature	125	°C
P_R	Steady State Power per Resistor @ 25°C	328	mW
T_{OP}	Operating Temperature Range	-40 to 85	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature for Soldering	260	°C

Note 1: Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

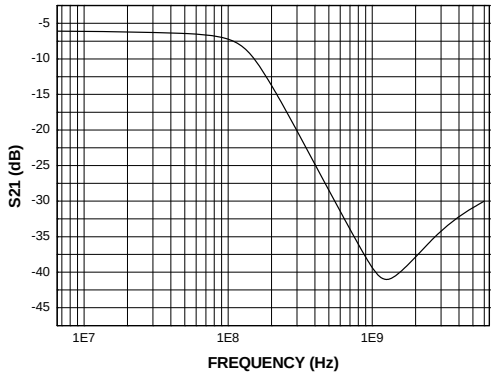
Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Stand-Off Voltage				5.0	V
V_{BR}	Reverse Breakdown Voltage	I_T=1.0mA	6 .0	7.0	8.0	V
I_R	Reverse Leakage Current	V_{RWM}=3.3V			100	nA
R_A	Total Series Resistance	I_R=10mA Each Line	85	100	115	Ω
C_d	Total Capacitance	Input to GND, Each Line V_R=0V, f=1MHz	16	20	24	pF
C_d	Total Capacitance	Input to GND, Each Line V_R=2.5V, f=1MHz	9	10	12	pF
f_{3dB}	Cut-Off Frequency (Note 2)	Above this frequency, appreciable attenuation occurs		150		MHz

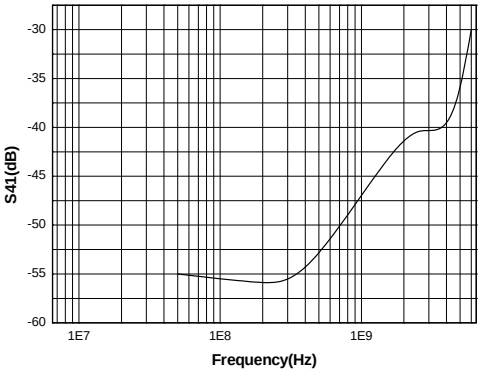
Note 2: 50Ω source and 50Ω load termination.

Typical Operating Characteristics

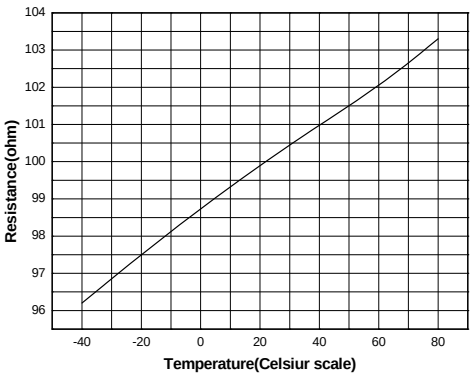
Typical Insertion Loss S21



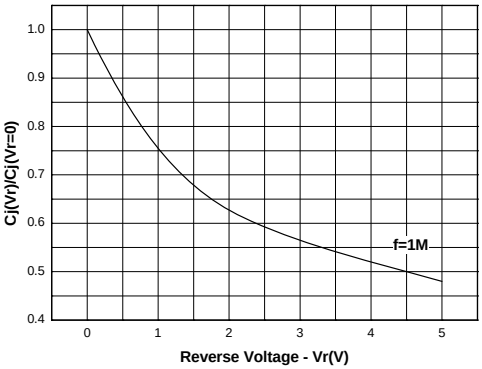
Analog Crosstalk Curve (S41)



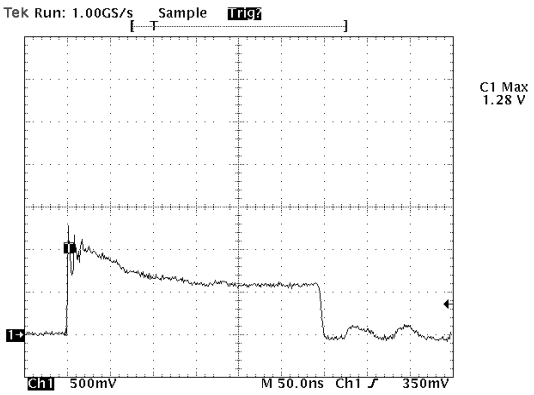
Typical Resistance vs. Temperature



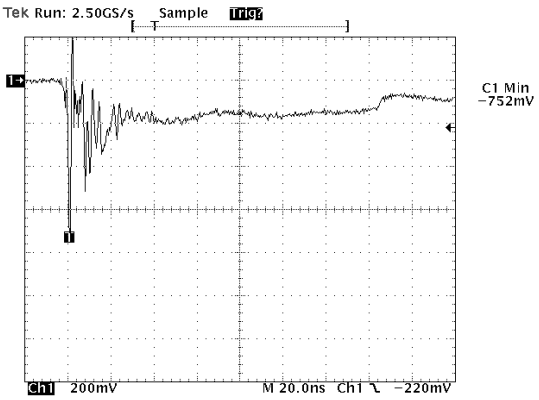
Capacitance vs. Reverse Voltage



ESD Clamping (+8kV Contact)



ESD Clamping (-8kV Contact)



Applications Information

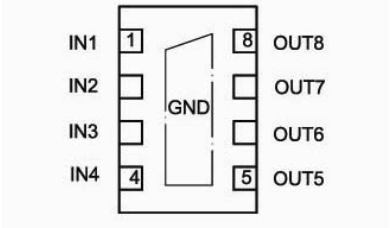
Device Connection

The UM4401 is comprised of four identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 8-pin DFN package. Electrical connection is made to the 8 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

Figure 1-Pin Identification and Configuration
(Top Side View)



Pin	Identification
1 - 4	Input Lines
5 - 8	Output Lines
Center Tab	Ground

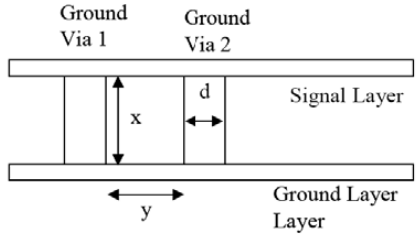
Equation 1: The Impedance of an Inductor at Frequency XLF

$XLF(L,f) = 2\times\pi\times f\times L$

Where:
L= Inductance (H)
f = Frequency (Hz)

Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 2 - Inductance of Rectangular Wire Loops



Equation 2: Inductance of Rectangular Wire Loop

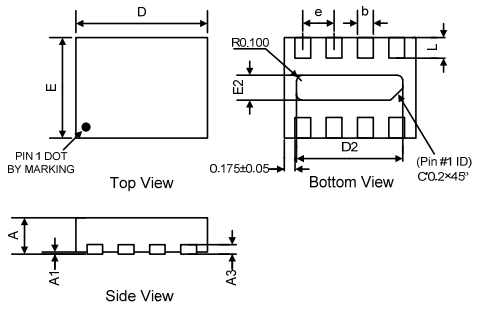
$$LRECT(d,x,y) = 10.16*10^{-9}*\left[x*\ln\left[\frac{2*y}{d}\right]+y*\ln\left[\frac{2*x}{d}\right]\right]$$

Where:
d = Diameter of the wire (in)
x = Length of wire loop (in)
y = Breath of wire loop (in)

Package Information

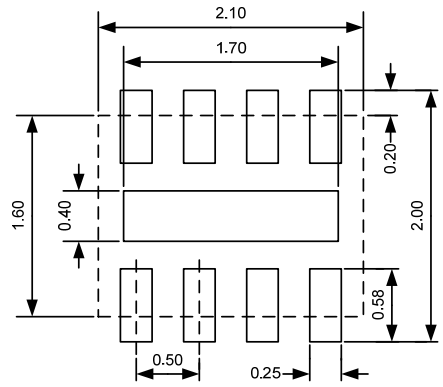
UM4401: DFN8 2.1×1.6

Outline Drawing



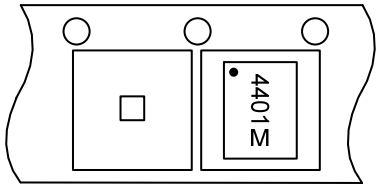
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.575	0.605	0.020	0.023	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15TYP			0.006TYP		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	2.05	2.10	2.175	0.081	0.083	0.086
D2	1.60	1.70	1.80	0.063	0.067	0.071
E	1.55	1.60	1.675	0.061	0.063	0.066
E2	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50TYP			0.020TYP		
L	0.275	-	0.38	0.011	-	0.015

Land Pattern



NOTES:
1. Compound dimension: 2.10×1.60;
2. Unit: mm;
3.General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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