NCP1030GEVB

Isolated 2 W Bias Supply for Telecom Systems Using the NCP1030 Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Introduction

Power converters using secondary side controllers provide better transient response, higher efficiency and usually require less components than their primary side referenced counterparts. However, secondary side controllers require a primary side referenced bias supply to start operation. After start−up, the controller power can be provided from the secondary side.

The NCP1030 incorporates in a single IC all the active power, control logic and protection circuitry required for implementing, with a minimum of external components, a highly integrated isolated bias supply. The features included in the NCP1030 can result in a footprint area reduction by up to 91% compared to a solution implemented using discrete components.

The NCP1030 Power Switch Circuit is rated at 200 V, making it ideal for 48 V Telecom and 42 V automotive applications. In addition, this IC can operate from an existing 12 V supply. The NCP1030 includes an extensive set of features including:

- **On Board Power Switch:** Eliminates the need for an external switch. As the Power Switch characteristics are well known the gate drive is tailored to control switching transitions and help reduce electromagnetic interference (EMI).
- **An Internal Start−up Regulator:** Provides power to the NCP1030 during start−up. After start−up, the regulator is disabled, thus reducing power consumption. The regulator can be powered directly from the input line.
- **Internal Error Amplifier:** Allows the implementation of an isolated supply using primary side regulation without the need for an optocoupler.
- **Internal Cycle by Cycle Current Limit:** Eliminates the need for external sensing components. The programmed current limit is 500 mA.
- **Proprietary Active Leading Edge Blanking (LEB) Circuit:** Provides better current limit control compared to a fixed blanking period. The active LEB circuit masks the current signal during the Power Switch turn ON transition.
- **Individual Line Undervoltage and Overvoltage (UV/OV) Detectors with Hysteresis:** Eliminate the need for external supervisory function. The UV/OV detectors can be disabled if not needed.
- **Single Capacitor Oscillator:** Eliminates traditional timing resistor. Oscillator is optimized for operation up to 1.0 MHz.
- **Internal ±2% Voltage Reference:** Eliminates the need for an external bypass capacitor.
- **Thermal Shutdown Circuit:** Protects the device in the event the maximum junction temperature is exceeded.

Design Specifications

An isolated bias supply for a telecom system is designed and implemented using the NCP1030. The supply delivers 2.0 W at 12 V. The converter specifications are listed in Table 1.

Table 1. BIAS SUPPLY SPECIFICATIONS

Parameter	Symbol	Min	Max
Input Voltage	V_{in}	35 V	76 V
Frequency	f	250 kHz	300 kHz
Peak Efficiency	η	80%	–
Output Voltage	V_{out}	10.8 V	13.2 V
Output Current	I_{out}	0.017 A	0.17 A
Output Power	P_{out}	2.0 W	–

A Flyback topology operating in discontinuous mode is selected because of its simplicity and low part count.

Flyback Converter

A dual output Flyback converter is shown in Figure 1. OUTPUT 1 is regulated by means of OUTPUT 2, providing an isolated OUTPUT 1 without the need for an optocoupler.

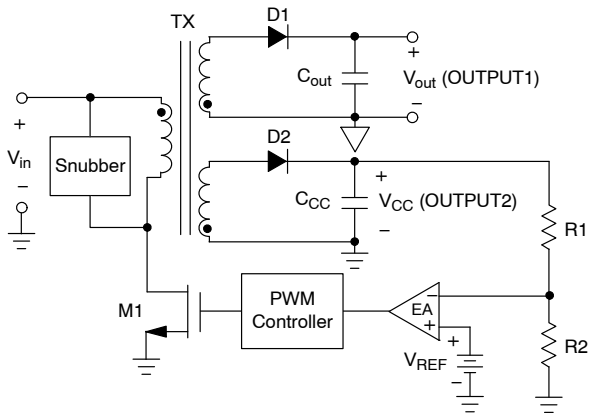

Figure 1. Isolated Flyback Converter

Current flows in the primary side when the Power Switch, M1, is ON. The transformer primary side dot end becomes positive with respect to the non−dot end. While the Power Switch is ON, energy is stored in the transformer and D1 and D2 are reverse biased. When M1 turns OFF, the transformer winding polarities are reversed, forward biasing D1 and D2. Energy is transferred to the secondary outputs during this period. If the secondary current decays to zero before the switch turns ON again, the converter operates in discontinuous mode. Otherwise, it operates in continuous mode.

The converter regulates the output by sampling the output voltage and comparing it to a reference voltage. A signal proportional to their difference is generated and used to adjust the ON time of M1 such that the voltage difference is reduced.

The Snubber limits the voltage across the Power Switch and helps reduce noise.

Design Procedure

The converter is designed to operate at a maximum duty cycle (DC) of 40 % and a primary peak current (I_{PPK}) of 400 mA. The required primary inductance, L_P, is calculated using Equation 1.

$$L_p = \frac{V_{in(min)} \times DC}{f \times I_{PPK}} \quad \text{(eq. 1)}$$

Solving Equation 1, a primary inductance of 127 μH is required. The transformer turns ratio $\left(\frac{Np}{Ns}\right)$ is calculated using Equation 2

$$\frac{N_p}{N_s} \geq \frac{(V_{in} - (I_{PPK} \times R_{DS(on)})) \times DC}{(V_{out} + V_{fD1}) \times (0.8 - DC)} \quad \text{(eq. 2)}$$

where, V_{fD1} is the forward voltage drop across D1 and $R_{DS(on)}$ is the Power Switch on resistance. Equation 2 relates the on−time volt−second product to the reset volt−second product and adds a 20% dead time to insure the converter operates in discontinuous mode. Solving Equation 2 assuming a 0.5 V drop across D1,

$$\frac{N_p}{N_s} \geq \frac{(35\ V - (0.4\ A \times 7\ \Omega)) \times 0.4}{(12\ V + 0.5\ V) \times (0.8 - 0.4)} \quad \text{(eq. 3)}$$

a turns ratio greater than 2.58 is required. A turns ratio of 2.78 is selected.

A maximum stress voltage of 110 V across the primary switch during the turn OFF period is calculated using Equation 4.

$$V_{stress} = V_{in(max)} + \frac{N_p}{N_s} \times (V_{out} + V_{fD1}) \quad \text{(eq. 4)}$$

The voltage is significantly below the 200 V maximum rating of the NCP1030 internal Power Switch.

The transformer winding arrangement includes a split primary with bifilar secondaries. The transformer can be ordered from Coilcraft under part number B0226−E. Table 2 summarizes the specifications of the transformer.

Table 2. TRANSFORMER SPECIFICATIONS

Parameter	Terminals	Min	Max
Magnetizing Inductance @ 0.4 A	1,2−3,4	102 μH	−
Leakage Inductance	1,2−3,4	−	0.955 μH
DC Resistance	1−4 2−3 5−6 7−8	− − − −	0.655 Ω 0.82 Ω 0.248 Ω 0.248 Ω
Resonant Frequency	−	3.8 MHz (typ.)	

Main Output

Two main factors, voltage ripple and frequency compensation, are considered for the selection of the output capacitor, C_{out}. This section will focus on voltage ripple, while frequency compensation is covered in a latter section.

The output capacitor provides the load current during the switch ON time. If the target voltage droop is known, C_{out} is calculated using Equation 5.

$$C_{out} = \frac{I_{out} \times (1 - DC)}{f \times V_{droop}} \quad \text{(eq. 5)}$$

Solving Equation 5, a maximum voltage droop of 50 mV requires a 7.4 μF capacitor. However, C_{out} may be increased to facilitate frequency compensation.

The secondary peak current, I_{SPK}, and the diode blocking voltage, V_{block}, determine the selection of rectification diodes, D1 and D2.

The primary peak current and transformer turns ratio determine the secondary peak current as given by Equation 6.

$$I_{SPK} = I_{PPK} \times \frac{N_p}{N_s} \quad \text{(eq. 6)}$$

The voltage across the rectification diode is given by Equation 7.

$$V_{block} = V_{out} + V_{in(max)} \times \left(\frac{N_s}{N_p}\right) \quad \text{(eq. 7)}$$

Solving Equations 6 and 7, the rectification diode needs to handle 1.11 A and 39.34 V. In addition to the voltage calculated using equation 7, voltage spikes during switching transitions need to be considered when selecting the blocking voltage rating. A Schottky diode is selected to reduce the forward voltage drop, thus reducing power dissipation. On Semiconductor's MBRA160 is selected as it meets all the requirements.

Auxiliary Supply Regulator

The auxiliary supply (OUTPUT 2) provides a means to regulate the main output (OUTPUT 1). In addition, the auxiliary winding disables the internal start−up circuit and provides power to the NCP1030 after initial power up. The same turns ratio and rectification diode used for the main output are used for the auxiliary winding to improve voltage tracking between the outputs.

The auxiliary winding capacitor, C_{CC}, is selected such that a voltage greater than 7.5 V is maintained on the V_{CC} pin while the output reaches regulation. The time the output reaches regulation is measured at 0.8 ms. Once the start−up time is known, C_{CC} is calculated using Equation 8.

$$C_{CC} = \frac{I_{CC} \times t}{2.5\ V} \quad \text{(eq. 8)}$$

where, I_{CC} includes the NCP1030 bias current (I_{CC3}) and any additional current supplied by C_{CC}. Assuming an I_{CC3} of 3.0 mA and a 2.0 mA bias current for the feedback sensing resistors, C_{CC} is calculated at 1.6 μF. The V_{CC} capacitor is set at 2.2 μF. Please note that if C_{CC} is increased to match C_{out}, the transient response of the converter will suffer. This is because the capacitance to current ratio of the auxiliary winding is significantly greater then the output winding, taking it longer for C_{CC} to follow C_{out} during a transient condition.

Feedback Loop

If the feedback loop is not stable, the converter will oscillate. To insure the loop is stable, the open loop frequency response needs to cross 0 dB at a slope of −20 dB/dec, with a phase margin above 45° under all line and load conditions. This is accomplished by shaping the loop response using the internal error amplifier (EA).

The block diagram shown in Figure 2 is used to evaluate the converter open loop response.

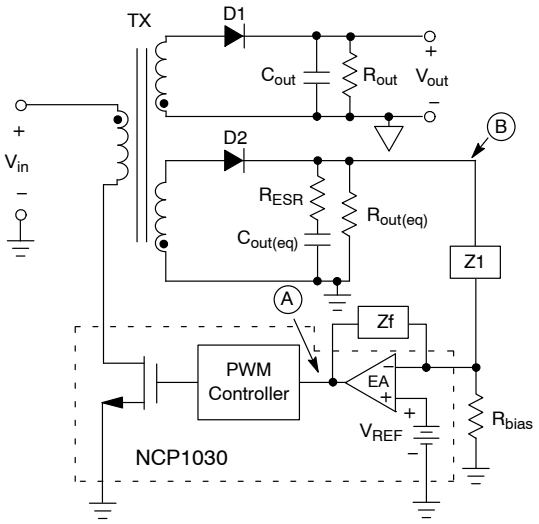

Figure 2. Flyback Converters

The open loop frequency response of the system (from A to B) is approximated by the modulator gain and the output network frequency response. Additional high frequency components are present but are not considered for our analysis as they are far beyond the crossover frequency. The modulator gain, G_{MOD}, is approximated by Equation 9.

$$G_{MOD} = \frac{3}{2} V_{in} \times \sqrt{\frac{R_{out(eq)} \times \eta}{2 \times f \times L_p}} \quad \text{(eq. 9)}$$

The output network block is comprised of C_{out}, R_{ESR} and R_{out}. The frequency response of the output network is given by Equation 10.

$$H(f) = \frac{sR_{ESR}C_{out(eq)} + 1}{sC_{out(eq)}\left(R_{ESR} + R_{out(eq)}\right) + 1} \quad \text{(eq. 10)}$$

The total open loop frequency response is the product of Equations 9 and 10. Please note that $C_{out(eq)}$ includes C_{CC} and C_{out} reflected to the auxiliary winding by the transformer turns ratio. As the same turns ratio is used for both the auxiliary and output windings, C_{out} adds directly to C_{CC}. The output network has one zero and one pole and they are given by Equations 11 and 12, respectively.

$$f_{z1} = \frac{1}{2\pi\, C_{out}\, R_{ESR}} \quad \text{(eq. 11)}$$

$$f_{p1} \approx \frac{1}{2\pi\, R_{out}\, C_{out}} \quad \text{(eq. 12)}$$

The modulator gain response depends on V_{in}. Two extreme conditions, both minimum R_{out} and input voltage (G_{MOD1}) as well as both maximum R_{out} and input voltage (G_{MOD2}) are considered for frequency compensation. In order to facilitate frequency compensation, C_{out} is increased to 22 μF. The simulated open loop frequency responses for G_{MOD1} and G_{MOD2} are shown in Figures 3 and 4, respectively.

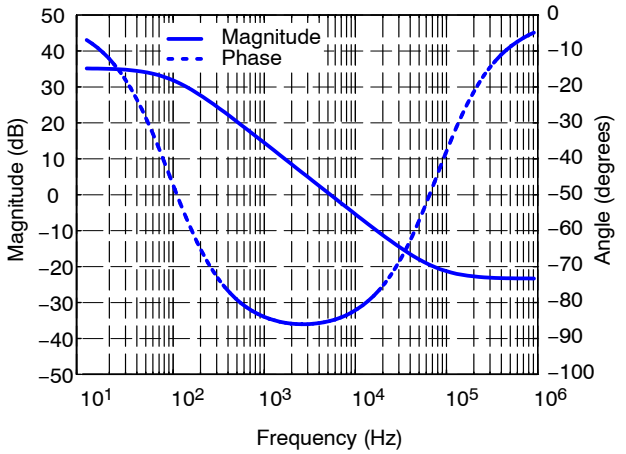

Figure 3. Open Loop Frequency Response for G_{MOD1}

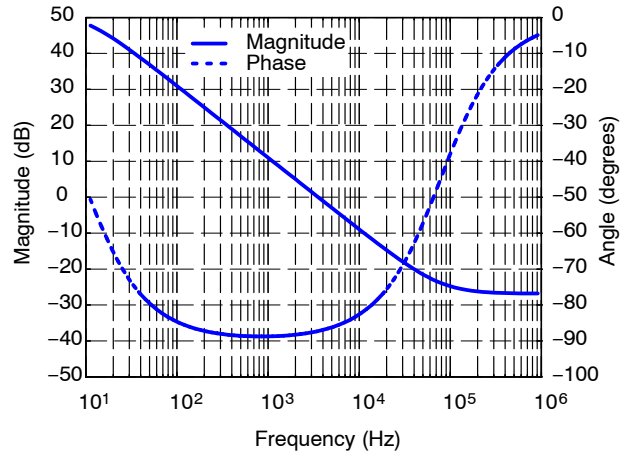

Figure 4. Open Loop Frequency Response for G_{MOD2}

The frequency compensation can be achieved using a type II error amplifier (EA) as the one shown in Figure 5.

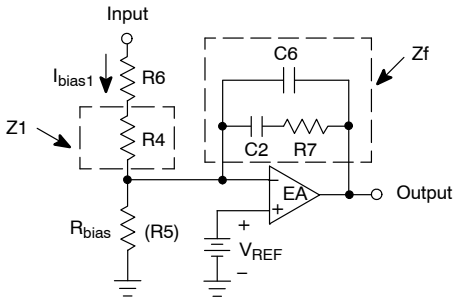

Figure 5. Type II Error Amplifier

A type II error amplifier has 2 poles and 1 zero. The transfer function is given by Equation 13.

$$H(f) = \frac{sR_7C_2 + 1}{sR_4(C_2 + C_6)\left(1 + sR_7\frac{C_7C_6}{C_7 + C_6}\right)} \quad \text{(eq. 13)}$$

One of the poles, f_{p2}, is at the origin. The frequency of the remaining pole and zero are given by Equations 14 and 15, respectively.

$$f_{z2} = \frac{1}{2\pi R_7C_2} \quad \text{(eq. 14)}$$

$$f_{p3} = \frac{(C_2 + C_6)}{2\pi R_7C_2C_6} \quad \text{(eq. 15)}$$

The EA poles and zero locations are selected to achieve the desired crossover frequency, f_{CO}. A system crossover frequency of 10 kHz is selected for G_{MOD1}. As the modulator gain depends on the input voltage, a higher f_{CO} is obtained for the maximum input voltage condition with equivalent output load.

The selection of the compensation components begins by noting that the voltage on the V_{FB} pin should be equal to 2.5 V (V_{REF}) when the output is in regulation (12 V). If the feedback sensing resistor network bias current (I_{bias1}) is known, R_4 and R_5 are calculated using Equations 16 and 17, respectively.

$$R_5 = \frac{V_{REF}}{I_{bias1}} \quad \text{(eq. 16)}$$

$$R_4 = \frac{V_{CC}}{I_{bias1}} - R_5 \quad \text{(eq. 17)}$$

Using a bias current of 2.0 mA, R_4 and R_5 are calculated at 4.99 kΩ and 1.30 kΩ, respectively. Resistor R_6 provides a test point to measure the open loop frequency response. It is set at 10 Ω to avoid disrupting the DC bias point.

The error amplifier DC gain, G_{EA}, is calculated using Equation 18. It is set at 6.03 dB to achieve a gain of 0 dB at 10 kHz for G_{MOD1}.

$$G_{EA} = 20\ \log\left(\frac{R_7}{R_4}\right) \quad \text{(eq. 18)}$$

The error amplifier zero, f_{z2}, is placed before the system response crosses 0 dB. Pole, f_{p3}, is placed after f_{CO} to attenuate high frequency components. Table 3 summarizes the system gain, poles and zeros. Figure 6 shows the EA frequency response.

Table 3. SYSTEM GAIN, POLES AND ZEROS

Parameter	Frequency (kHz)	Magnitude (dB)
f_{P1} (@ G_{MOD1})	0.091	–
f_{P1} (@ G_{MOD2})	0.009	–
f_{P2}	0	–
f_{P3}	23.9	–
f_{Z1}	77.4	–
f_{Z2}	0.482	–
G_{EA}	–	6.03

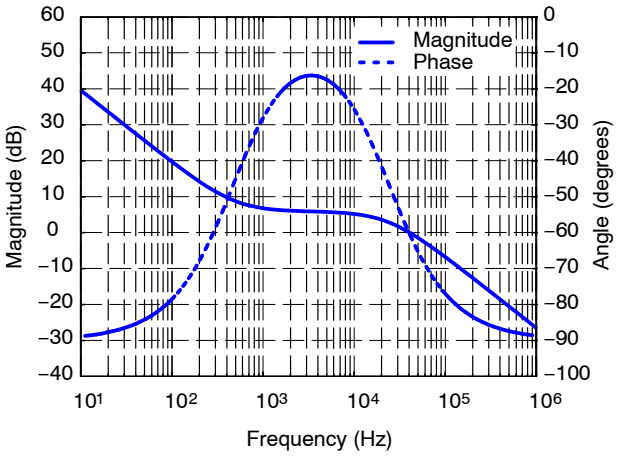

Figure 6. Error Amplifier Frequency Response

The phase contributions of a zero and a pole at the crossover frequency are given by Equations 19 and 20, respectively.

$$\theta_z = \tan^{-1}\left(\frac{f_{CO}}{f_z}\right) \quad \text{(eq. 19)}$$

$$\theta_p = \tan^{-1}\left(\frac{f_{CO}}{f_p}\right) \quad \text{(eq. 20)}$$

The phase margin, θ_M, is evaluated taking into account the phase contribution of all the poles and zeros as shown below in Equation 21.

$$\theta_M^{\circ} = 180 - \theta_{p1} - \theta_{p2} - \theta_{p3} + \theta_{z1} + \theta_{z2} \quad \text{(eq. 21)}$$

$$\theta_M = 180^{\circ} - 89.5^{\circ} - 90^{\circ} - 22.7^{\circ} + 7.33^{\circ} + 87.24^{\circ} = 72.4^{\circ}$$

The calculated phase margin is 72.4°. The 180° term arises because the EA is in an inverting configuration. The simulated system frequency responses for G_{MOD1} and G_{MOD2} are shown in Figure 7.

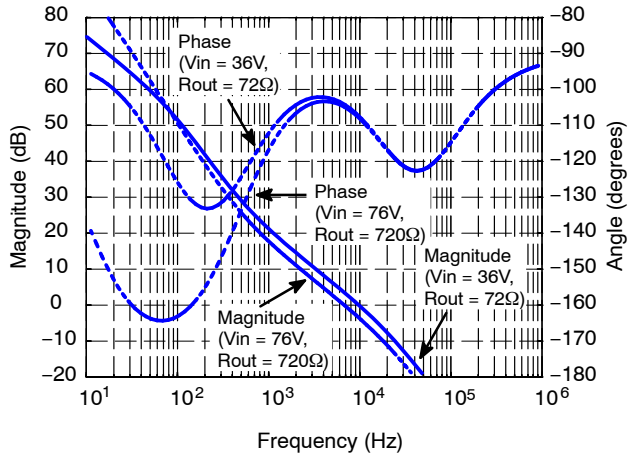

Figure 7. System Frequency Response

Under/Overvoltage Detectors

The NCP1030 eliminates the need for additional supervisory circuitry by incorporating individual under and overvoltage detectors with hysteresis. The controller is enabled if the voltage on the UV pin is above 2.5 V and the voltage on the OV pin is below 2.5 V. The UV/OV detectors can be biased using an external resistor divider as shown in Figure 8.

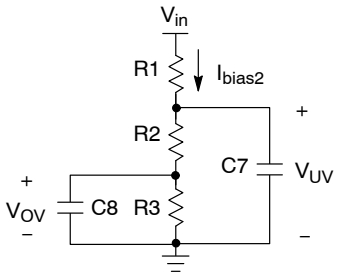

Figure 8. UV/OV Resistor Bias Network

If the resistor network bias current, I_{bias2}, is known, and the V_{OV} and V_{UV} thresholds are equal, R_1, R_3 and R_2 are calculated using Equations 22, 23 and 24, respectively.

$$R_1 \approx \frac{V_{in(max)}}{I_{bias2}} \quad \text{(eq. 22)}$$

$$R_3 \approx \frac{V_{OV} \times R_1 \times V_{in(min)}}{V_{in(min)}V_{in(max)} - V_{OV}(\Delta V_{in} + V_{in(min)})} \quad \text{(eq. 23)}$$

$$R_2 \approx \frac{R_3 \times \Delta V_{in}}{V_{in(min)}} \quad \text{(eq. 24)}$$

Using a bias current of 78 μA, a turn ON voltage of 35 V, a turn OFF voltage of 80 V and a V_{OV} threshold of 2.55 V, R_1, R_2 and R_3 are calculated at approximately 1.0 MΩ, 45.3 kΩ and 34 kΩ, respectively. Capacitors C_7 and C_8 help reduce noise and provide a stable voltage during turn ON and turn OFF transitions. They are set at 10 nF.

Oscillator Frequency

An oscillator frequency of 275 kHz is obtained with a timing capacitor (C_T) of 680 pF. The tolerance of C_T is set at 5%.

Snubber

An RCD snubber as shown in Figure 9 is added to help reduce noise. The snubber is returned to the positive supply rail to reduce the voltage stress on C_9 to V_{in}. If returned to the negative supply rail, the voltage stress is $2V_{in}$.

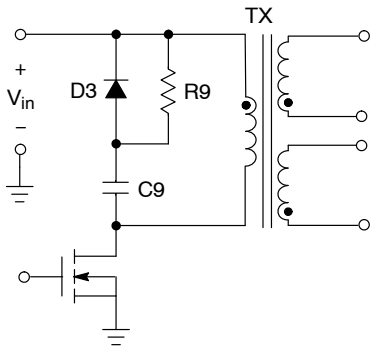

Figure 9. RCD Snubber

The power dissipation of R_9 is determined by C_9 and is given by equation 25.

$$P = \frac{1}{2} C_9 V_{in}^2 f \qquad \text{(eq. 25)}$$

The snubber components are not assembled in the converter. However, electrical connections are provided if the user wants to add the snubber components.

Input Filter

An L–C filter at the converter input is used to reduce EMI. The input L–C filter reduces noise and provides a solid input voltage to the converter. The filter is shown in Figure 10. Capacitor C_{10} is used for common mode noise reduction.

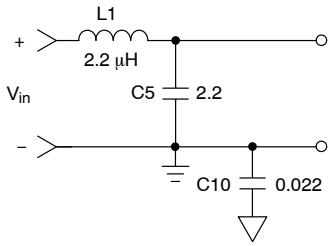

Figure 10. Input L–C Filter Schematic

Oscillation may occur if the converter input impedance, Z_{in}, is lower than the LC filter output impedance[1]. The converter input impedance can be approximated as a negative resistor using Equation 26.

$$Z_{in}(dB - Ohm) \approx -20 \log\left(\frac{V_{out}}{I_{out}}\right) \qquad \text{(eq. 26)}$$

The converter closed loop input impedance is ultimately determined by the converter feedback loop as well as the open loop input impedance. However, a resistor is a good approximation and will be used for our analysis. Figure 11 shows the theoretical input filter output impedance and the approximated converter input impedance.

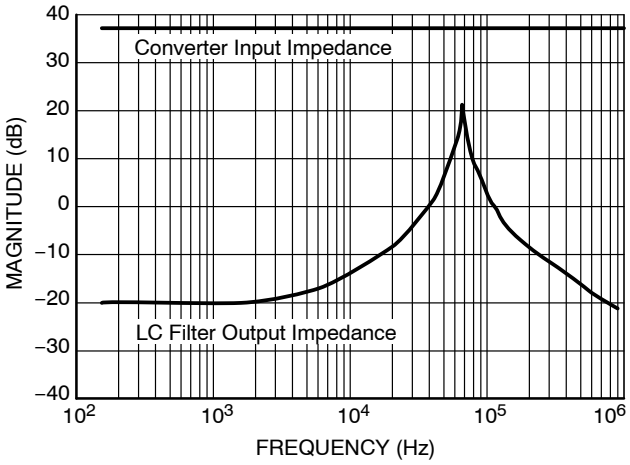

Figure 11. LC Filter Output Impedance and Approximated Converter Input Impedance

Layout Considerations

Switching regulators can be noisy! However, with careful layout, noise is reduced. A few things to remember are:

1. Keep switching elements and high current traces away from the controller and sensitive nodes.
2. Keep trace lengths to a minimum, especially important for high current paths and timing components.
3. Use wide traces for high current paths.
4. Place bypass capacitors close to the components.
5. Use a ground plane if possible or a single point ground system.

The bias supply is built using a single layer FR4, board. The board size is 2.0 in x 3.5 in. The complete circuit schematic is shown in Figure 12 and an actual size picture of the board is shown in Figure 13. The Bill of Material is listed in Table 4.

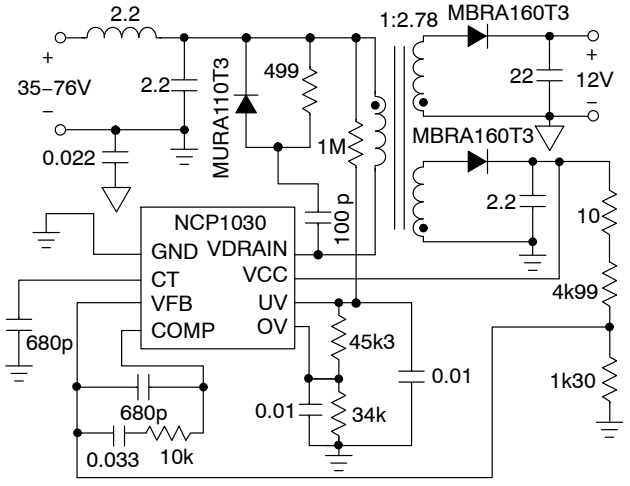

Figure 12. Complete Circuit Schematic

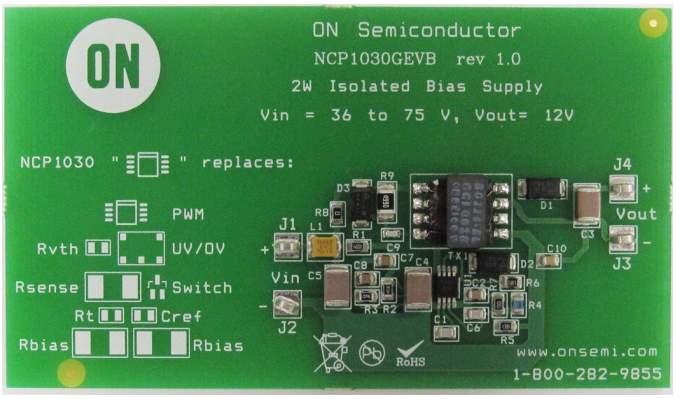

Figure 13. Evaluation Board (Actual Size)

Table 4. BILL OF MATERIALS

Designator	QTY	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	RoHS Compliant
C1, C6	2	Ceramic Chip Capacitor	680 pF, 25 V	5%	0805	Vishay	VJ0805A681JXA	Yes	Yes
C2	1	Ceramic Chip Capacitor	0.033 μF, 50 V	10%	0805	AVX Corporation	08055C333KAT2A	Yes	Yes
C3	1	Ceramic Chip Capacitor	22 μF, 25 V	20%	1812	TDK	C4532X5R1E226M	Yes	Yes
C4	1	Ceramic Chip Capacitor	2.2 μF, 25 V	20%	1812	TDK	C4532X7R1H225M	Yes	Yes
C5	1	Ceramic Chip Capacitor	2.2 μF, 100 V	20%	1812	TDK	C4532X7R2A225M	Yes	Yes
C7, C8	2	Ceramic Chip Capacitor	0.01 μF, 50 V	10%	0805	AVX Corporation	08055C103KAT2A	Yes	Yes
C9	1	Ceramic Chip Capacitor Optional	100 pF, 100 V	5%	0603	TDK	C1608C0G2A101J	Yes	Yes
C10	1	Ceramic Chip Capacitor	0.022 μF, 250 V	10%	0805	TDK	C2012X7R2E223K	Yes	Yes
D1, D2	2	Shottky Power Rectifier	1 A, 60 V	NA	SMA	ON Semiconductor	MBRA160T3G	No	Yes
D3	1	Ultrafast Power Rectifier Optional	1 A, 100 V	NA	SMA	ON Semiconductor	MURA110T3G	No	Yes
J1−J4	4	Printed Circuit Pin	NA	NA	NA	Mill−Max	0912−0−00−80−00−00−03−0	Yes	Yes
L1	1	Surface Mount Inductor	2.2 μH, 0.32 A	10%	1210	Vishay	IMC1210ER2R2K	Yes	Yes
R1	1	Thick Film Chip Resistor	1.00 MΩ, 1/8 W	1%	0805	Yageo	RC0805FR−071ML	Yes	Yes
R2	1	Thick Film Chip Resistor	45.3 kΩ, 1/8 W	1%	0805	Yageo	RC0805FR−0745K3L	Yes	Yes
R3	1	Thick Film Chip Resistor	34 kΩ, 1/8 W	1%	0805	Yageo	RC0805FR−0734KL	Yes	Yes
R4	1	Thick Film Chip Resistor	4.99 kΩ, 1/8 W	1%	0805	Yageo	RC0805FR−074K99L	Yes	Yes
R5	1	Thick Film Chip Resistor	1.30 kΩ, 1/8 W	1%	0805	Yageo	RC0805FR−071K3L	Yes	Yes
R6	1	Thick Film Chip Resistor	10.0 Ω, 1/8 W	1%	0805	Yageo	RC0805FR−0710RL	Yes	Yes
R7	1	Thick Film Chip Resistor	10.0 kΩ, 1/8 W	1%	0805	Yageo	RC0805FR−0710KL	Yes	Yes
R8	1	Thick Film Chip Resistor	0 Ω, 1/8 W	5%	0805	Vishay	CRCW08050000Z0EA	Yes	Yes

Table 4. BILL OF MATERIALS

Desig-nator	QTY	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substi-tution Allowed	RoHS Com-pliant
R9	1	Thick Film Chip Resistor Optional	499 Ω, 1/3 W	1%	1210	Vishay	CRCW1210499RFKEA	Yes	Yes
TX1	1	Flyback Transformer	120 μH, 12 V	10%	10.16 x 12.07 mm	Coilcraft	B0226−EL	Yes	Yes
U1	1	PWM Controller	NA	NA	Micro8	ON Semiconductor	NCP1030DMR2G	No	Yes

Design Verification

The final step in our design includes validation and test of the bias supply. Before powering the supply, it should be inspected for potential problems. A few suggestions include:

1. Verify all connections. Check for shorts and opens, especially on the input and output terminals.
2. Verify component values.
3. Slowly increase the input voltage while monitoring the input current. If the input current exceeds 10 mA, repeat steps 1 to 3.
4. Once the input voltage reaches 25 V, measure the voltage on critical nodes. The NCP1030 start−up regulator should be ON. If the voltages are not correct, remove power and repeat steps 1 to 3.
5. Increase the input voltage to 36 V. Measure the output voltage. If it is not approximately 12 V, repeat steps 1 to 3.
6. Increase the input voltage above 80 V. The output should turn OFF.

Please be careful when probing and testing the converter. High voltage may be present. Exercise CAUTION!

Once the converter functionality is verified, the board performance is evaluated and compared to our original goals. The evaluation criteria includes:

1. Open loop frequency response.
2. Efficiency.
3. Line and load regulation.
4. Step load response.
5. Start−up response.

The open loop response is measured injecting an AC signal across R_6 using a network analyzer as shown in Figure 14.

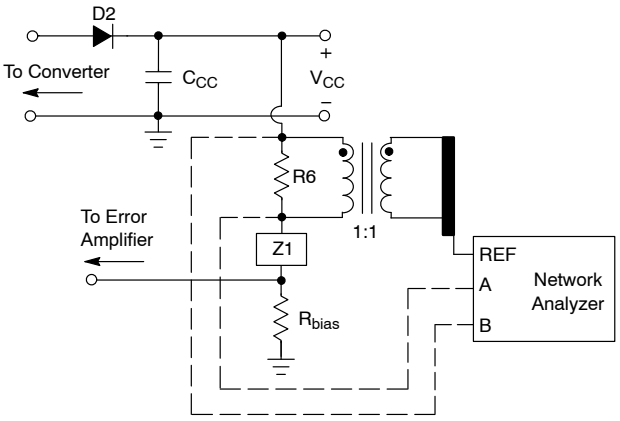

Figure 14. Open Loop Frequency Response Measurement Set−up

The measured frequency response is shown in Figure 15. The crossover frequency is measured at 9 kHz.

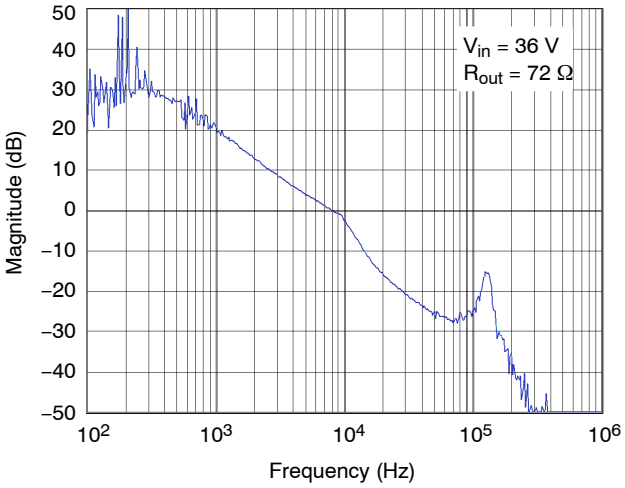

Figure 15. Open Loop Frequency Response

Peak efficiency is measured at 83%. Figure 16 shows the efficiency vs. output current under several input voltage conditions.

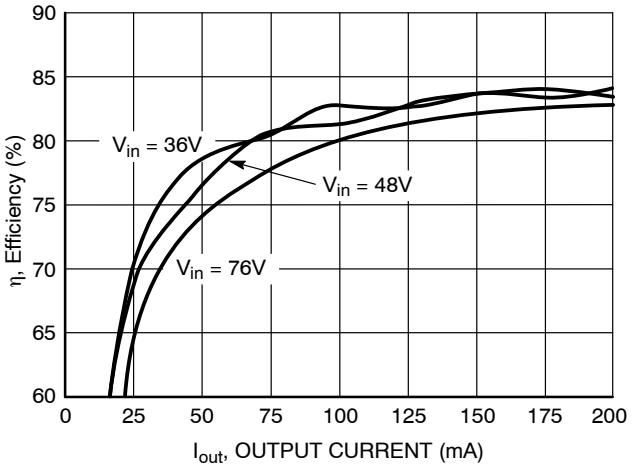

Figure 16. Efficiency vs Output Current

Line and load regulation are calculated using Equations 27 and 28, respectively.

$$Reg_{LINE} = \frac{\Delta V_{out}}{\Delta V_{in}} \quad \text{(eq. 27)}$$

$$Reg_{LOAD} = \frac{V_{out(No\ Load)} - V_{out(Full\ Load)}}{V_{out(No\ Load)}} \quad \text{(eq. 28)}$$

Line regulation is measured below 0.5% and load regulation is measured below 8%. Figure 17 shows the output voltage variation to output current under several input voltage conditions.

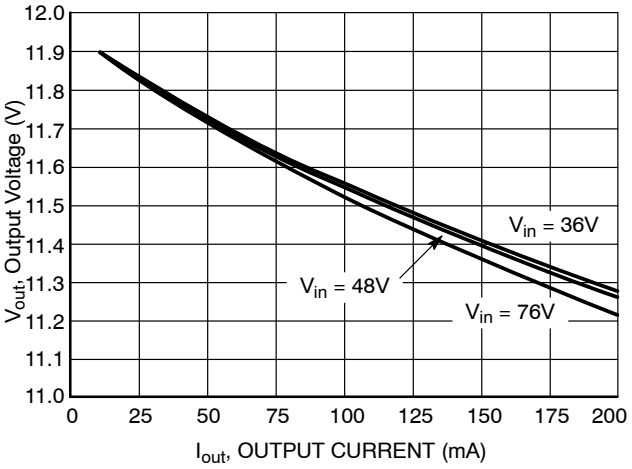

Figure 17. Output Voltage vs. Output Current

The dynamic response of the converter is evaluated stepping the load current from 50% to 75% and from 75% to 50% of $I_{out(max)}$. The step load transient responses are shown in Figures 18 and 19.

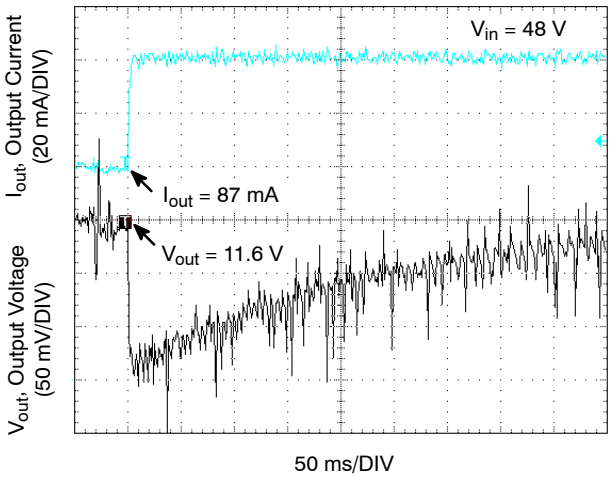

Figure 18. Output Voltage Response to a Step Load from 87 mA to 127 mA

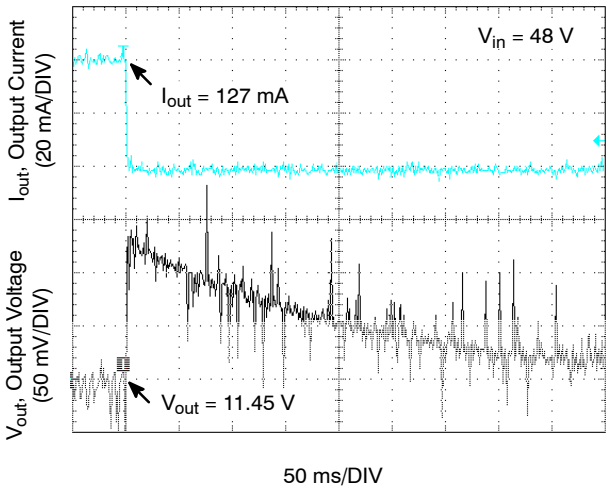

Figure 19. Output Voltage Response to a Step Load from 127 mA to 87 mA

Output voltage ripple is measured at 25 mV for an output current of 170 mA. It is significantly below the 50 mV target. The output voltage ripple waveform is shown in Figure 20.

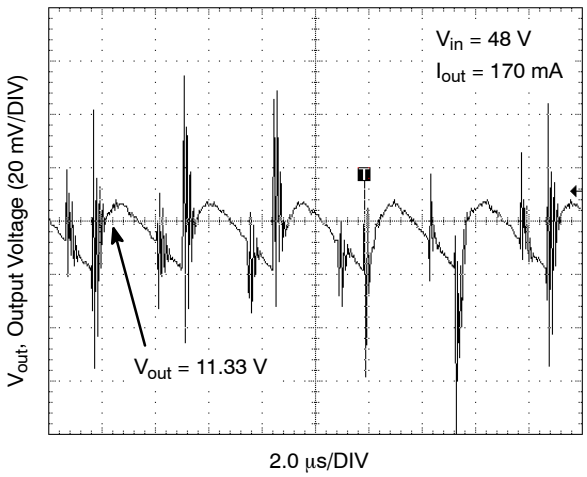

Figure 20. Output Voltage Ripple

Finally, the converter turn ON response at full load is evaluated. Figure 21 shows the output turn ON transient response at full load.

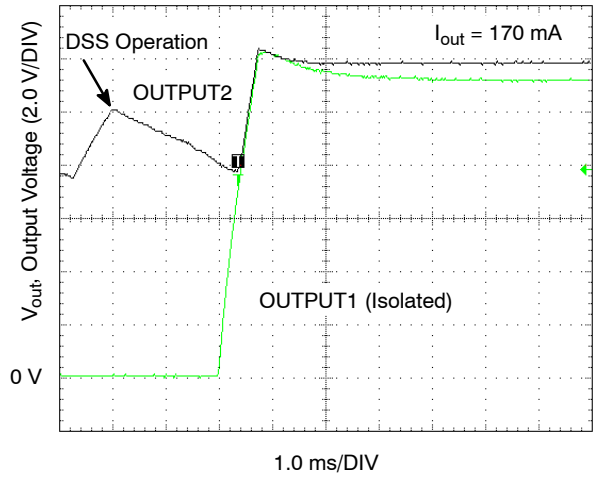

Figure 21. Output Voltage During Turn ON at Full Load

Output 2 operates in DSS while the converter is disabled. Once the converter is enabled, Output 1 tracks Output 2.

Summary

An isolated 12 V bias supply for a 48 V telecom system is implemented using the NCP1030. The converter achieves a peak efficiency of 83% while providing good transient response.

References

1. Ridley, Ray. “The Evolution of Power Electronics”, *Switching Power Magazine*, Fall 2001:16–30.
2. Pressman, Abraham I. *Switching Power Supply Design.* 2nd ed. New York, NY: MacGraw Hill.

TEST PROCEDURE FOR THE NCP1030GEVB

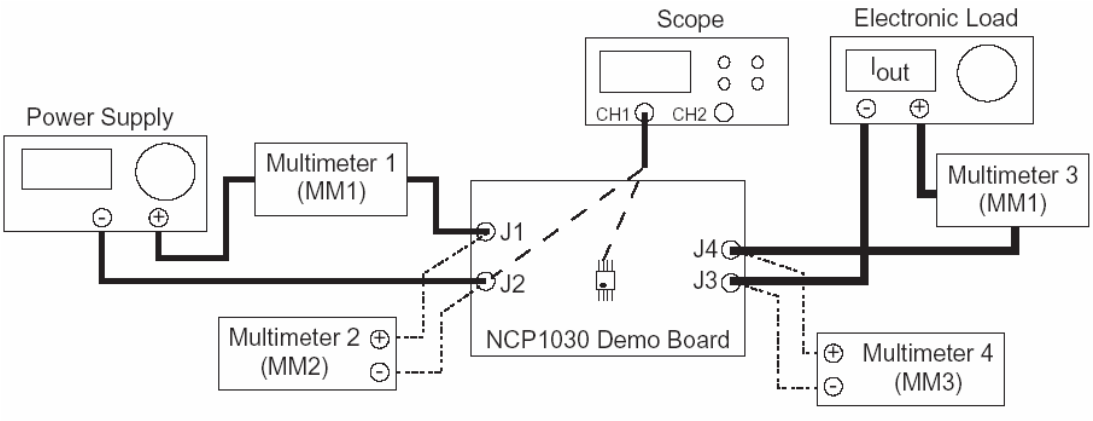

Figure 22. Test Setup

Table 5. REQUIRED EQUIPMENT

Equipment	Quantity
Dual Channel Oscilloscope	1
Keithley 179A Multimeter or Similar	4
Test Leads	4
Positive and Negative Probe Leads for the Oscilloscope	1
KIKUSUI PLZ303W Load	1
(76 V, 1 A) Power Supply	1
NCP1030 Evaluation Board	1

Test Procedure:

1. Connect the test setup as shown above.
2. Apply an input voltage, V_{IN} = 25 V across J1 and J2.
3. Check the switching waveform at scope CH1 to see whether the start−up circuit is enabled.
4. Apply an input voltage, V_{IN} = 36 V across J1 and J2. Measure the output voltage across J4 and J3. It should be approximately 12 V.
5. Apply 175 mA loading from the electronic load after powering up the evaluation board.
6. Measure V_{IN}, I_{IN}, I_{OUT}, V_{OUT}.
7. Increase V_{IN} to 80 V. The output should turn OFF.

Table 6. DESIRED RESULTS

V_{IN} = 36 V	I_{IN} = 70 mA to 80 mA V_{OUT} = 11.1 V to 11.5 V
V_{IN} = 48 V	I_{IN} = 50 mA to 60 mA V_{OUT} = 11.1 V to 11.5 V
V_{IN} = 76 V	I_{IN} = 30 mA to 40 mA V_{OUT} = 11.0 V to 11.5 V

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