MOSFET - N-Channel Shielded Gate PowerTrench®
150 V, 15 mΩ, 50 A

NTDS015N15MC

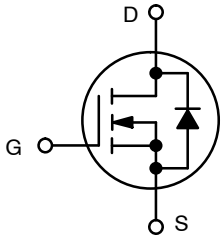
ON Semiconductor®

www.onsemi.com

Features
- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 15 mΩ at V_{GS} = 10 V, I_D = 29 A
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Primary Side for 48 V Isolated Bus
- SR for MV Secondary Applications

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
150 V	15 mΩ @ 10 V	50 A



N−CHANNEL MOSFET

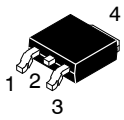
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	150	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	50	A
Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	P_D	83	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	11	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	P_D	3.8	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs		I_{DM}	246	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy (I_L = 10 A_{pk}, L = 3 mH)			E_{AS}	150	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

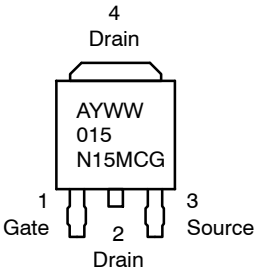
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM



DPAK
CASE 369C



015N15MCG = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTDS015N15MCT4G	DPAK (Pb−Free)	2500 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	1.8	°C/W
Junction−to−Ambient − Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		150			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			83		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V	T_J = 25°C			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 162 μA		2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 162 μA, ref to 25°C			−8.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 29 A			11.8	15	mΩ
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 8 V, I_D = 15 A			12.6	16.8	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 29 A			58		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 75 V			2120		pF
Output Capacitance	C_{OSS}				595		
Reverse Transfer Capacitance	C_{RSS}				10.5		
Gate−Resistance	R_G				0.6	1.2	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 75 V; I_D = 29 A			27		nC
Threshold Gate Charge	$Q_{G(TH)}$				7		
Gate−to−Source Charge	Q_{GS}				11		
Gate−to−Drain Charge	Q_{GD}				4		
Plateau Voltage	V_{GP}				5.5		V
Output Charge	Q_{OSS}	V_{DD} = 75 V, V_{GS} = 0 V			66		nC
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 75 V, I_D = 29 A, R_G = 6 Ω			16		ns
Rise Time	t_r				5		
Turn−Off Delay Time	$t_{d(OFF)}$				21		
Fall Time	t_f				4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 29 A	T_J = 25°C		0.89	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V dI_S/dt = 300 A/μs, I_S = 29 A			49		ns
Reverse Recovery Charge	Q_{RR}				197		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V dI_S/dt = 1000 A/μs, I_S = 29 A			34		ns
Reverse Recovery Charge	Q_{RR}				345		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

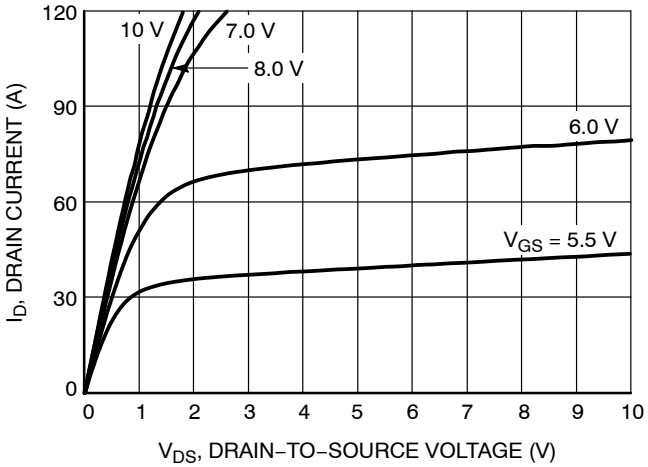

Figure 1. On−Region Characteristics

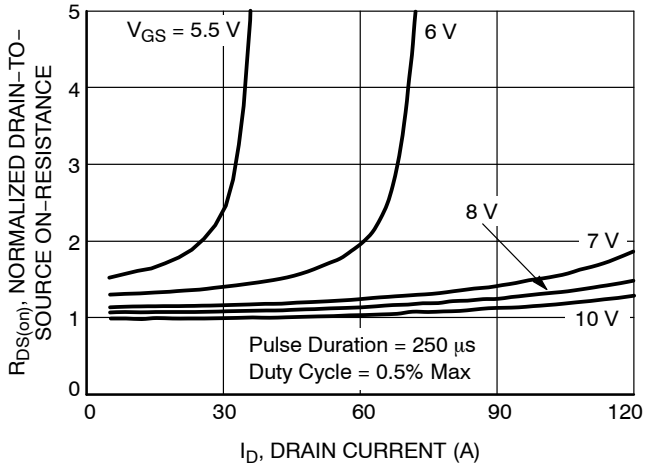

Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

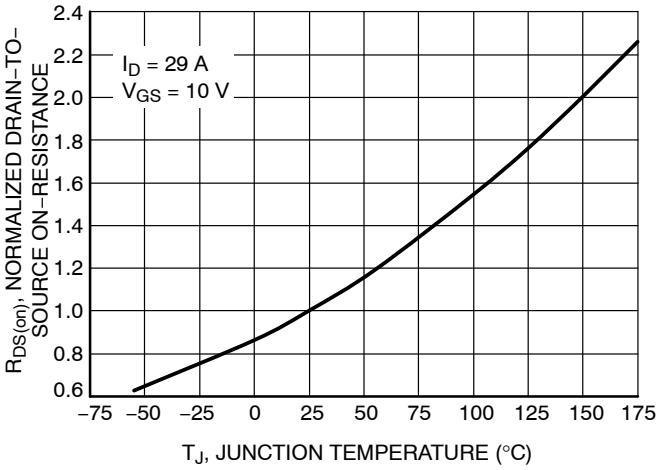

Figure 3. Normalized On−Resistance vs. Junction Temperature

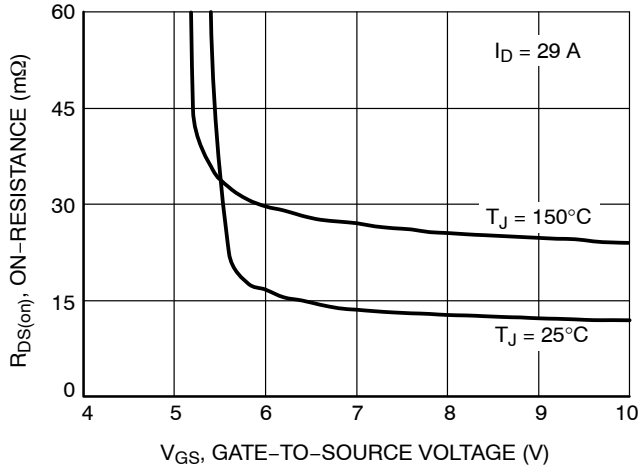

Figure 4. On−Resistance vs. Gate−to−Source Voltage

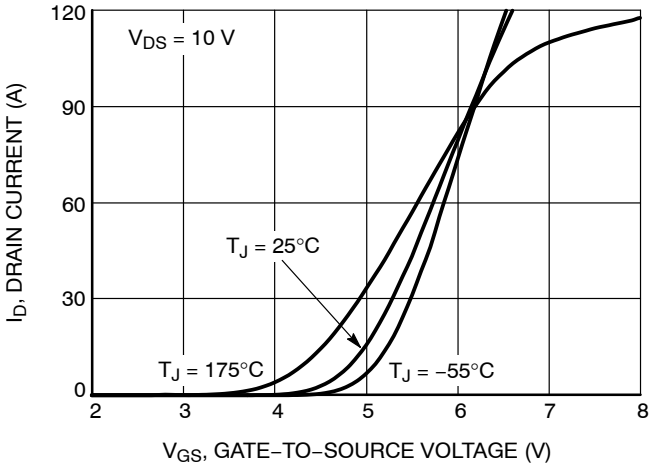

Figure 5. Transfer Characteristics

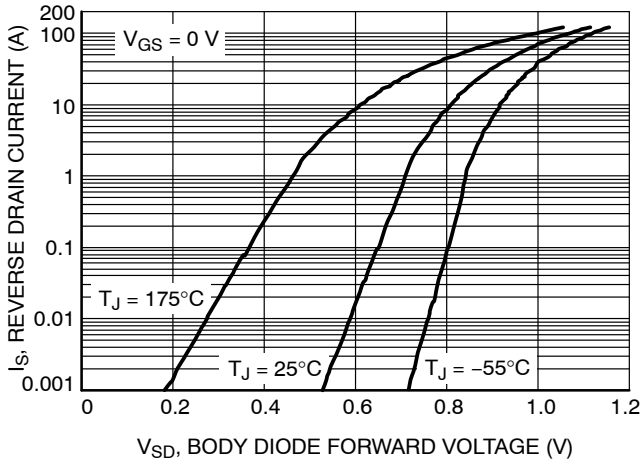

Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS

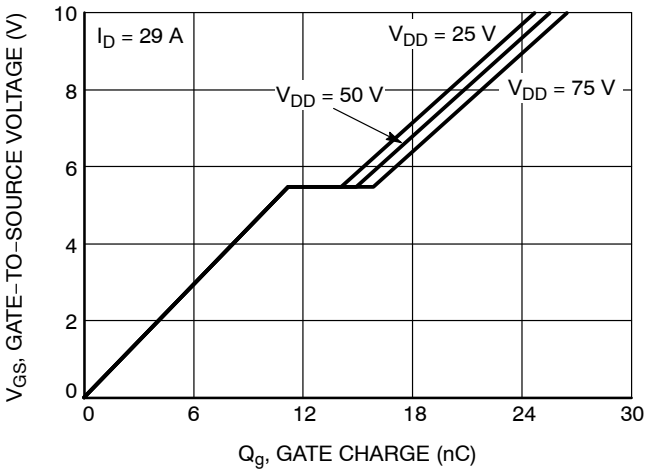

Figure 7. Gate Charge Characteristics

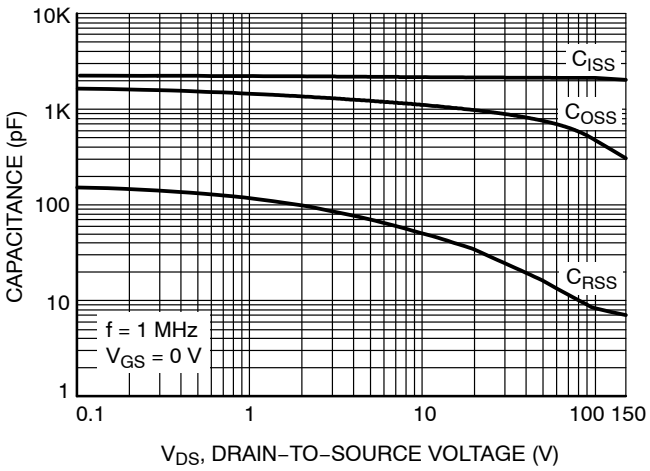

Figure 8. Capacitance vs. Drain−to−Source Voltage

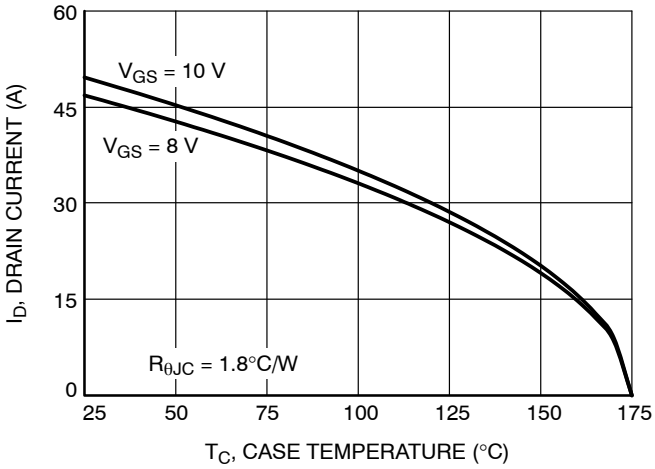

Figure 9. Drain Current vs. Case Temperature

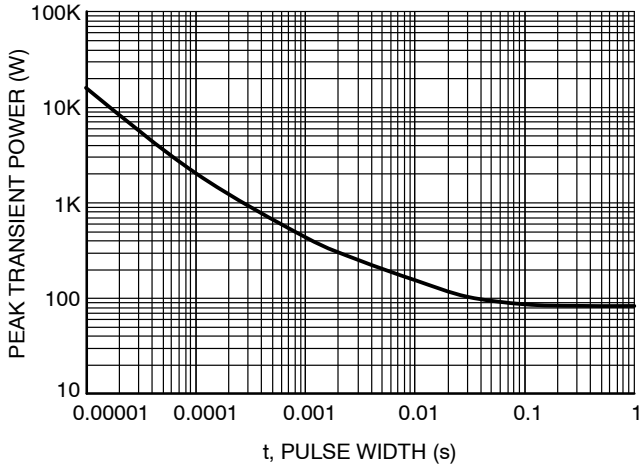

Figure 10. Peak Power

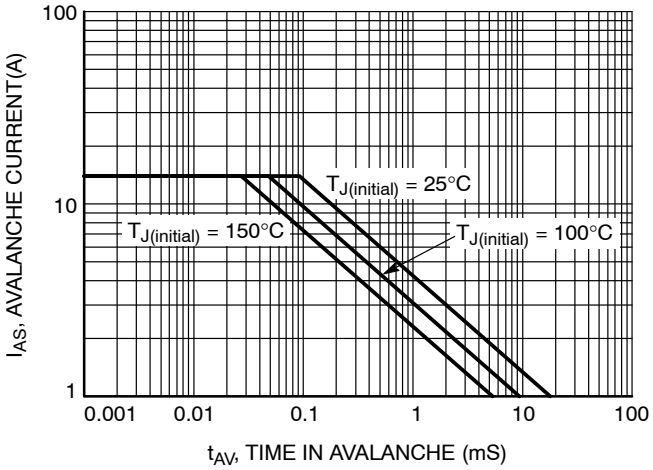

Figure 11. Unclamped Inductive Switching Capability

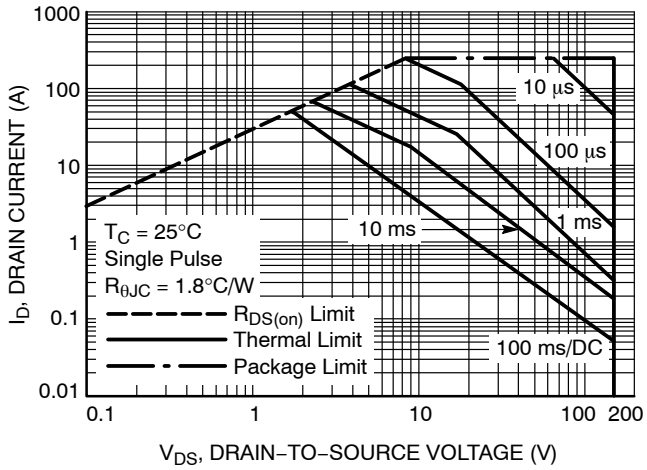

Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

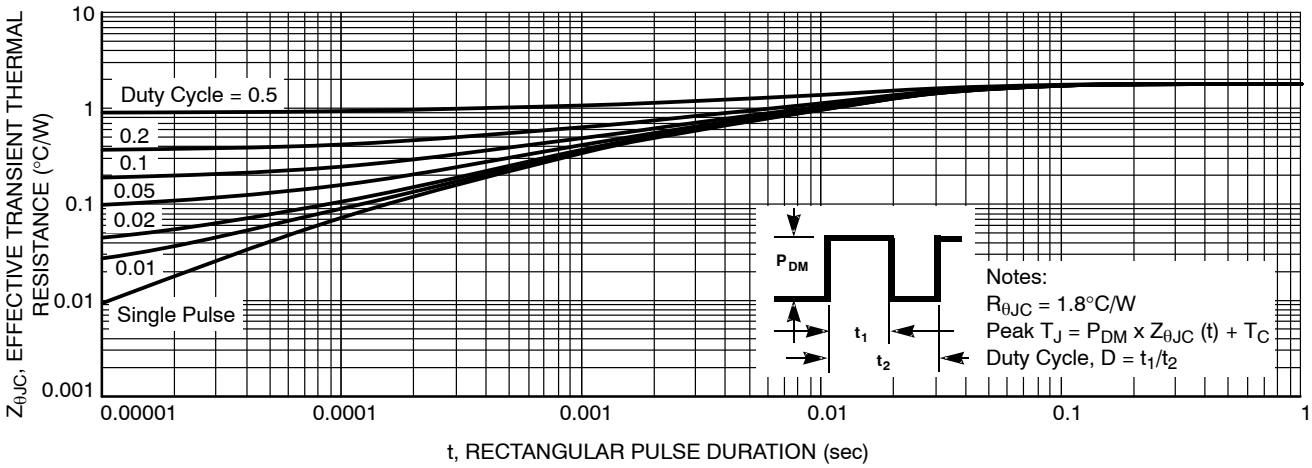

Figure 13. Transient Thermal Impedance

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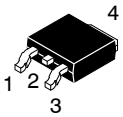
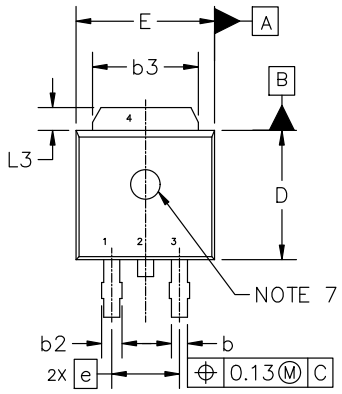


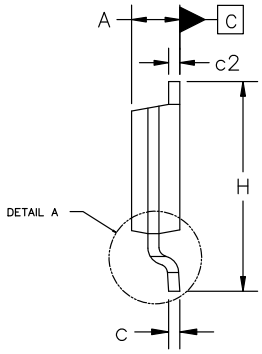
SCALE 1:1

DPAK–3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

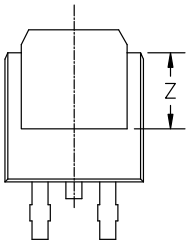


TOP VIEW

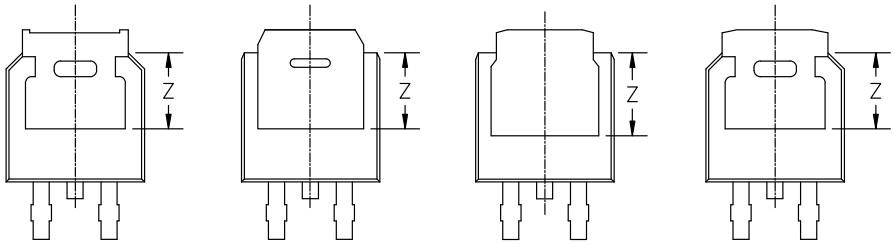


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



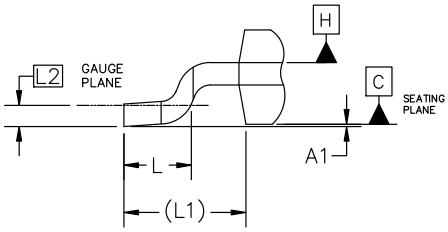
BOTTOM VIEW



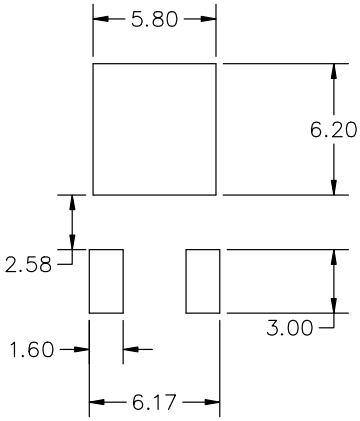
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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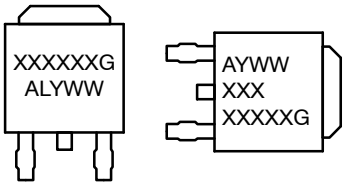
DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 13 MAY 2026

GENERIC
MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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