



LTC2311/LTC2310 Single 16-Bit/14-Bit/12-Bit, 5Msps/2Msps, Serial, High Speed SAR ADCs

DESCRIPTION

Demonstration circuit 2425A features the LTC®2311 family. With up to 5Msps, these differential, single channel, 16-bit, serial, high speed successive approximation register (SAR) ADCs are available in a 16-lead MSOP package. The LTC2311 family has an internal 20ppm/°C maximum drift reference and an SPI-compatible serial interface that supports CMOS and LVDS logic. Note the demo board is configured for CMOS operation by default; see the note under JP3 for LVDS operation. The following text refers to the LTC2311, but applies to all members of the family, the only difference being the sample rate and/or the

number of bits. The DC2425A demonstrates the DC and AC performance of the LTC2311 in conjunction with the DC890 PScope™ data collection board. Alternatively, by connecting the DC2425A into a customer application, the performance of the LTC2311 can be evaluated directly in that circuit.

Design files for this circuit board are available at http://www.linear.com/demo/DC2425A

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BOARD PHOTO

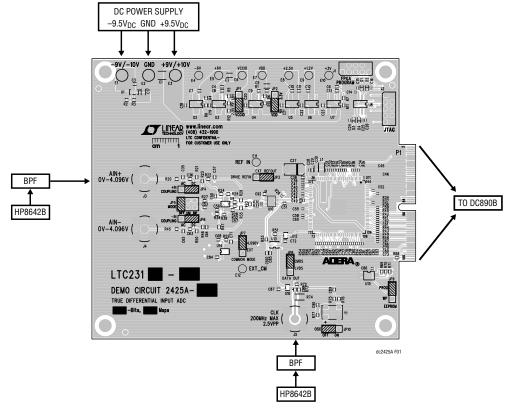


Figure 1. DC2425A Connection Diagram

ASSEMBLY OPTIONS

Table 1. DC2425A Assembly Options

VERSION	U1 PART NUMBER	MAX CONVERSION RATE	# OF BITS	MAX CLOCK FREQUENCY
DC2425A-A	LTC2311CMSE-16#PBF	5Msps	16	105MHz
DC2425A-B	LTC2310CMSE-16#PBF	2Msps	16	42MHz
DC2425A-C	LTC2311CMSE-14#PBF	5Msps	14	105MHz
DC2425A-D	LTC2310CMSE-14#PBF	2Msps	14	42MHz
DC2425A-E	LTC2311CMSE-12 #PBF	5Msps	12	105MHz
DC2425A-F	LTC2310CMSE-12#PBF	2Msps	12	42MHz

QUICK START PROCEDURE

Demonstration circuit 2425A is easy to set up and evaluate for performance. Refer to Figure 1 and follow the procedure below.

- Connect the DC2425A to a DC890 USB high speed data collection board using edge connector P1.
- Connect the DC890 to a host PC with a standard USB A/B cable.
- Apply a low jitter signal source to J3 to test channel 1. Note that the DC2425A is capable of accepting a differential input signal as well as a single-ended signal. See the Hardware Setup section for the jumper positions that correspond to these configurations.
- As a clock source, apply a low jitter 10dBm sine wave or square wave to connector J5. See Table 1 for maximum clock frequencies. Note that J5 has a 50Ω termination resistor to ground.
- Run the PScope software (Pscope.exe version K73, or later) supplied with the DC890 or download it from www.linear.com/software. Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically, as new features may be added. The PScope software should recognize the DC2425A and configure itself automatically.

Click the Collect button (Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be used to stop data acquisition.

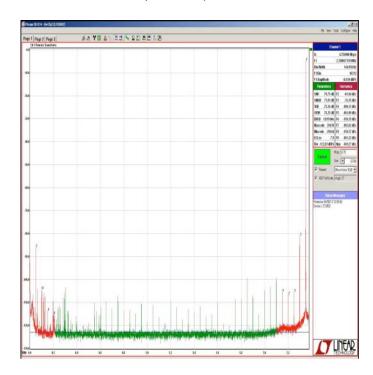


Figure 2. DC2425A PScope Screenshot

QUICK START PROCEDURE

DRIVE OPTIONS

There are several ways to drive the LTC2311 on the DC2425A.

If a true differential signal source is available, apply the signal to the differential inputs J3 and J4; make the following changes to the DC2425A:

- Remove R27, R38.
- Install 0Ω 0603 resistors at R39, R47.

If a single-ended signal source is available, the LTC2311 may be driven differentially by applying the signal to J3.

The LTC2311 may be driven in the pseudo-differential bipolar mode by applying the single-ended signal to J3; make the following changes to the DC2425A:

- Move JP5 to the BIP position.
- Install a 10µF 0603 capacitor at C56.

The LTC2311 may be driven in the pseudo-differential unipolar mode by applying the single-ended signal to J3; make the following changes to the DC2425A:

- Move JP5 to the UNI position.
- Install a 10µF 0603 capacitor at C56.



HARDWARE SETUP

SIGNAL CONNECTIONS

J1 FPGA Program: Factory use only.

J2 JTAG: Factory use only.

J3 AIN+ Input: In the single-ended configuration, this is the signal input. For differential operation, this serves as the positive signal input.

J4 AIN— **Input**: This input is used only for differential operation. It serves as the negative signal input.

J5 CLK: This input has a 50Ω termination resistor, and is intended to be driven by a low jitter 10dBm sine or square wave. To achieve the full AC performance of this part, the clock jitter should be kept under 2ps. This input is capacitively coupled so that the input clock can be either OV to 2.5V or ± 1.25 V. This eliminates the need for level shifting. To run at the maximum conversion rate, apply the frequency specified in the Table 1.

JP1 VCCIO: Use this jumper to select the VCCIO supply voltage. The default setting is **2.5V**. The **1.8V** setting selects a 1.8V supply voltage.

JP2 VDD: Use this jumper to select the VDD supply voltage. The default setting is **5V**. The **3.3V** setting selects a 3.3V supply voltage.

JP3: Use this jumper to select the reference source for the LTC2311. The default setting is DRIVE REFOUT. This setting uses the voltage applied to Pin 3 of the LTC2311 as the reference voltage. The EXT setting will accept a voltage applied to E11 as the reference voltage. If no voltage is applied to E11, the LTC2311 will use it's internal reference, which is 4.096V.

JP4 +IN Coupling: Use this jumper to select AC- or DC-coupling of the signal applied to J3. The default setting is **DC**. At very low input frequencies, using AC-coupling may degrade the distortion performance.

JP5 Mode: Use this jumper to select the signal input mode for the LTC2311. The default setting is DIFF. The DIFF setting accepts a single-ended signal from J3 but applies it as a differential signal to the LTC2311. The BIP setting accepts a single-ended signal from J3 and applies it as a single-ended bipolar signal to the LTC2311. The UNI setting also accepts a single-ended signal from J3, and applies it as a unipolar signal to the LTC2311. See Drive Options section fro more details.

JP6 –IN Coupling: Use this jumper to select AC- or DC-coupling of the signal applied to J4. The default setting is **DC**. At very low input frequencies, using AC-coupling may degrade the distortion performance.

JP7 CM: Use this jumper to set the DC bias point for the signal applied to J3 when JP4 (+IN coupling) is in the AC position. The default setting is 4.096V which sets the common mode voltage at 2.048V. The EXT setting allows the use of an externally applied common mode voltage applied at E12 (EXT CM1).

JP8 Data Out: Use this jumper to select the data output format from the LTC2311. The default setting is CMOS. The output data will not be valid if the jumper is moved to the LVDS position unless the following changes have been made:

Install 100Ω 0402 resistors at R26, 75, 76, 99

Reprogram the CPLD through J1 using the programming file LTC2311.pof found at:

http://www.linear.com/demo/DC2425A

Move JP8 to the **LVDS** position.

JP9 EEPROM: Factory use only.

JP10 OSC: Use this jumper to enable the onboard encode clock source. The default setting is **OFF**. The **ON** setting energizes this source. Refer to the DC2425A schematic for additional passive elements required to use the onboard source.

LINEAR TECHNOLOGY

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Require	ed Circ	uit Components		
1	13	C4, C6, C11, C12, C36, C48, C53, C63, C71, C92, C93, C95, C100	CAP., X5R, 10µF, 6.3V 20% 0603	NIC, NMC0603X5R106M6.3TRPF4KF
2	0	C35, C37, C56, C64, C65	CAP., 0603	OPT
3	1	C54	CAP, NP0, 200pF, 50V 5%, 0603	MURATA, GRM1885C1H201JA01D
4	9	C3, C18, C19, C20, C21, C23, C51, C84, C99	CAP., X7R, 1μF, 25V 10%, 0603	TDK, C1608X7R1E105K
5	2	C106, C119	CAP, X5R, 4.7µF, 6.3V 10%, 0603	AVX, 06036D475KAT2A
6	1	C68	CAP., X5R, 2.2µF, 10V 10%, 0603	MURATA, GRM188R61A225KE34D
7	1	C1	CAP, X7R, 47µF, 10V 10%, 1210	MURATA, GRM32ER71A476KE15L
8	5	C7, C8, C9, C10, C13	CAP, X7R, 0.01µF, 6.3V 10%, 0603	MURATA, GRM188R70J103KA01D
9	3	C2, C5, C17	CAP, X7R, 10µF, 10V 10%, 0805	MURATA, GRM21BR71A106KE51L
10	1	C22	CAP, X5R, 3.3µF, 6.3V 10%, 0603	AVX, 06036D335KAT2A
11	40	C14, C26, C31, C32, C33, C34, C42, C44, C45, C46, C49, C50, C52, C55, C57, C58, C59, C60, C61, C62, C66, C67, C69, C70, C72, C73, C74, C75, C76, C79, C81, C85, C86, C87, C88, C89, C90, C94, C96, C97	CAP., X7R, 0.1µF, 16V 10%, 0402	NIC, NMC0402X7R104K16TRPF
12	1	C30	CAP., X5R, 47µF, 6.3V 20%, 0805	TAIYO YUDEN, JMK212BJ476MG-T
13	3	C40, C43, C78	CAP, X7R, 0.01µF, 16V 10%, 0402	NIC, NMC0402X7R103K16TRPF
14	1	C80	CAP., X7R, 1nF, 16V 10%, 0402	AVX, 0402YC102KAT2A
15	3	C28, C82, C83	CAP., X7R, 22nF, 16V 10%, 0402	AVX, 0402YC223KAT2A
16	2	C77, C41	CAP., X7R, 4.7nF, 16V 10%, 0402	AVX, 0402YC472KAT2A
17	4	C15, C16, C24, C25	CAP., NP0, 10pF, 16V 10%, 0402	AVX, 0402YA100KAT2A
18	1	C27	CAP., TANT, 470µF 10V 20%, 7343	AVX, TPSE477M010R0050
19	1	C39	CAP., X7R, 2.2nF, 16V 10%, 0402	AVX, 0402YC222KAT2A
20	4	D1, D2, D3, D4	DIODE, SCHOTTKY 30V 200MW, SOD323	DIODE INC., BAT54WS-7-F
21	9	E4, E5, E6, E7, E8, E9, E10, E11, E12	TEST POINT, TURRET, 0.064"	MILL MAX, 2308-2-00-80-00-00-07-0
22	3	E1, E2, E3	TEST POINT, TURRET, 0.094"	MILL MAX, 2501-2-00-80-00-00-07-0
23	9	JP1, JP2, JP3, JP4, JP6, JP7, JP8, JP9, JP10	HEADER, 1X3, 0.100"	SAMTEC, TSW-103-07-L-S
24	1	JP5	HEADER, 2X3, 0.100"	SAMTEC, TSW-103-07-L-D
25	3	J3, J4, J5	CONN BNC FEM JACK PC MNT STRGHT	AMPHENOL CONNEX, 112404
26	2	J1, J2	HEADER, 2X5, 0.100"	SAMTEC, TSW-105-07-L-D
27	2	L1, L2	IND., FERRITE CHIP 390Ω 2000mA 1206	MURATA, BLM31PG391SN1L
28	10	R2, R8, R9, R10, R11, R23, R38, R58, R72, R73	RES., CHIP, 1k, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF1001V
29	0	R21, R24, R27, R29, R31, R35, R46, R50, R75	RES., CHIP, 0603	ОРТ
30	1	R53	RES., CHIP, 33Ω, 1/10W, 5% 0603	PANASONIC, ERJ-3GEYJ330V

DEMO MANUAL DC2425A

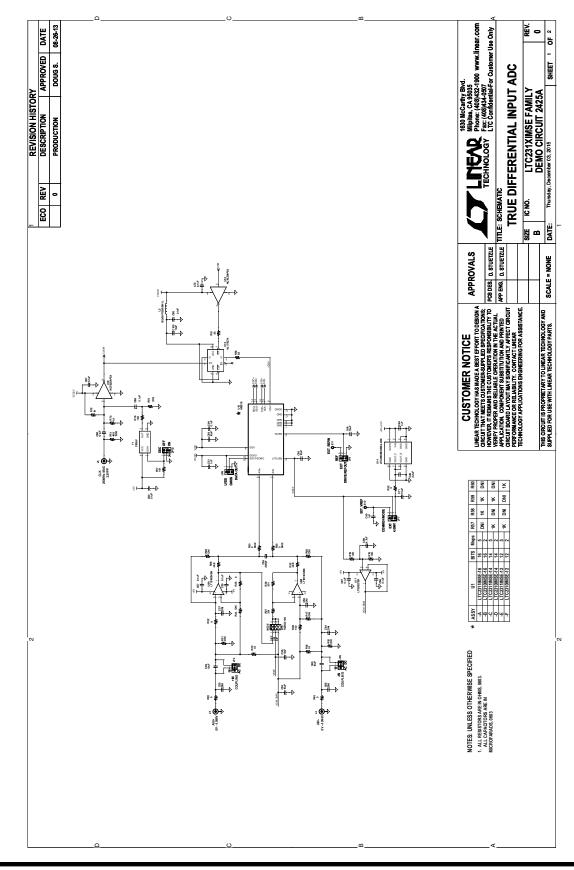
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
31	7	R20, R22, R25, R39, R45, R47, R52	RES., CHIP, 0Ω, 1/10W, 0603	PANASONIC, ERJ-3GEY0R00V
32	2	R30, R33	RES., CHIP, 0Ω, 1/16W, 0402	PANASONIC, ERJ-2GEJ0R00V
33	2	R28, R32	RES., CHIP, 49.9Ω, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF49R9V
34	1	R74	RES., CHIP, 49.9Ω, 1/4W, 1% 1206	PANASONIC, ERJ-8ENF49R9V
35	0	R26, R31	RES., CHIP, 0402	OPT OPT
36	2	R3, R4	RES., CHIP, 3.92k, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF3921V
37	1	R5	RES., CHIP, 499Ω, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF4990V
38	1	R12	RES., CHIP, 866Ω, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF8660V
39	1	R6	RES., CHIP, 3.09k, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF3091V
40	1	R1	RES., CHIP, 4.02k, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF4021V
41	1	R7	RES., CHIP, 1.43k, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF1431V
42	18	R19, R34, R36, R37, R40, R41, R42, R43, R44, R48, R49, R51, R53, R54, R55, R56, R65, R66, R67	RES., CHIP, 33Ω, 1/16W, 5% 0402	PANASONIC, ERJ-2GEJ330X
43	1	R15	RES., CHIP, 1k, 1/16W, 1% 0402	PANASONIC, ERJ-2RKF1001X
44	4	R68, R69, R70, R71	RES., CHIP, 4.99k, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF4991V
45	9	R13, R14, R16, R17, R18, R61, R62, R63, R64	RES., CHIP, 10k, 1/16W, 5% 0402	PANASONIC, ERJ-2GEJ103X
46	3	R77, R78, R79	RES., CHIP, 10k, 1/10W, 5% 0603	PANASONIC, ERJ-3GEYJ103V
47	1	R76	RES., CHIP, 100, 1/10W, 1% 0603	PANASONIC, ERJ-3EKF1000V
48	2	U12, U16	IC, INVERTER UHS SINGLE SC70-5	FAIRCHILD, NC7SZ04P5X
49	1	U9	IC, 400MHz AMPLIFIER, MS8	LINEAR TECH., LT1819CMS8#PBF
50	1	U13	IC, FLIP FLOP D-TYPE LOG, US8	ON SEMI., NL17SZ74USG
51	1	U14	IC, VOLTAGE REFERENCE, MSOP8	LINEAR TECH., LTC6655BHMS8-4.096#PBF
52	1	U17	IC, OP-AMP, TSOT23-5	LINEAR TECH., LT6202CS5#PBF
53	4	U2, U3, U4, U7	IC, MICROPOWER REGULATOR, S08	LINEAR TECH., LT1763CS8#PBF
54	1	U1	IC, MICROPOWER NEG. REGULATOR, SOT-23	LINEAR TECH., LT1964ES5-SD#PBF
55	1	U5	IC, MICROPOWER REGULATOR, S08	LINEAR TECH., LT1763CS8-2.5#PBF
56	1	U6	IC, LINEAR REGULATOR, SO8	LINEAR TECH., LT3021ES8-1.2#PBF
57	1	U11	IC, CYCLONE III FPGA 5k, EQFP144	ALTERA, EP3C5E144C7N
58	1	U8	IC, CONFIG DEVICE 4MBIT, SO8	ALTERA, EPCS4SI8N
59	1	U15	IC, EEPROM 2kBIT 400kHz, TSSOP8	MICROCHIP, 24LC024-I/ST
60	1	Y1	OSCILLATOR, 106.2500 MHz 3.3V SMD, Y-CB3LV	CTS-FREQUENCY, CB3LV-3I-106M2500
61	10	SHUNTS AS SHOWN ON ASSY DWG	SHUNT, 0.100	SAMTEC, SNT-100-BK-G
62	4	MH1-MH4	STANDOFF, NYLON 0.25"	KEYSTONE, 8831 (SNAP ON)

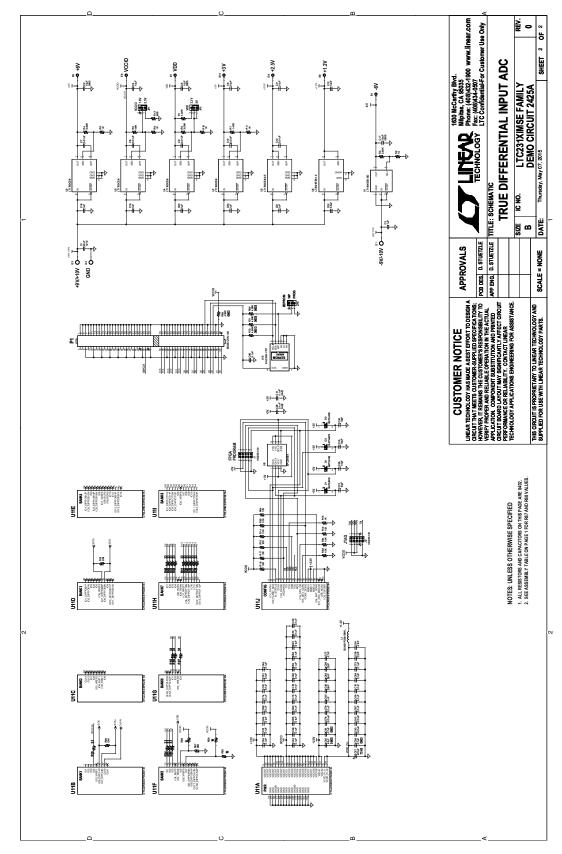
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC2425	A-A Re	equired Circuit Components		
1	1	DC2425A	General BOM	
2	2	R58, R59	RES., CHIP, 1k, 1/10W, 1% 0402	PANASONIC, ERJ-2EKF1001V
3	0	R57, R60	RES, 0402 DNI	
4	1	U10	I.C., SAR ADC, MSOP-4X5	LINEAR TECH., LTC2311CMSE-16#PBF
DC2425	A-B Re	equired Circuit Components		
1	1	DC2425A	General BOM	
2	2	R58, R59	RES., CHIP, 1k, 1/10W, 1% 0402	PANASONIC, ERJ-2EKF1001V
3	0	R57, R60	RES, 0402 DNI	
4	1	U10	I.C., SAR ADC, MSOP-4X5	LINEAR TECH., LTC2310CMSE-16#PBF
DC2425	A-C Re	equired Circuit Components		
1	1	DC2425A	General BOM	
2	2	R57, R59	RES., CHIP, 1k, 1/10W, 1% 0402	PANASONIC, ERJ-2EKF1001V
3	0	R58, R60	RES, 0402 DNI	
4	1	U10	I.C., SAR ADC, MSOP-4X5	LINEAR TECH., LTC2311CMSE-14#PBF
DC2425	5A-D R	equired Circuit Components		
1	1	DC2425A	General BOM	
2	2	R57, R59	RES., CHIP, 1k, 1/10W, 1% 0402	PANASONIC, ERJ-2EKF1001V
3	0	R58, R60	RES, 0402 DNI	
4	1	U10	I.C., SAR ADC, MSOP-4X5	LINEAR TECH., LTC2310CMSE-14#PBF
DC2425	5A-E Re	equired Circuit Components		
1	1	DC2425A	General BOM	
2	2	R57, R60	RES., CHIP, 1k, 1/10W, 1% 0402	PANASONIC, ERJ-2EKF1001V
3	0	R58, R59	RES, 0402 DNI	
4	1	U10	I.C., SAR ADC, MSOP-4X5	LINEAR TECH., LTC2311CMSE-12#PBF
DC2425	A-F Re	equired Circuit Components		
1	1	DC2425A	General BOM	
2	2	R57, R60	RES., CHIP, 1k, 1/10W, 1% 0402	PANASONIC, ERJ-2EKF1001V
3	0	R58, R59	RES, 0402 DNI	
4	1	U10	I.C., SAR ADC, MSOP-4X5	LINEAR TECH., LTC2310CMSE-12#PBF

SCHEMATIC DIAGRAMS



SCHEMATIC DIAGRAMS



tion that the interconnection of its circuits as described herein will not infringe on existing patent rights.

dc2425af

DEMO MANUAL DC2425A

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LTC currently services a variety of customers for products around the world, and therefore this transaction is not exclusive.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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