

C3M0075120K1

Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- Optimized package with separate driver source pin
- Lower profile TO-247-4 package body
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters
- Solar/ESS
- UPS
- Enterprise PSU

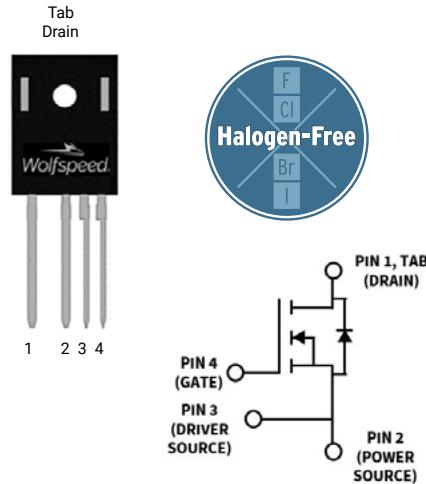
Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V	$T_c = 25^\circ C$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			32	A	$V_{GS} = 15 V, T_c = 25^\circ C, T_j \leq 175^\circ C$	Fig. 19 Note 2
				23		$V_{GS} = 15 V, T_c = 100^\circ C, T_j \leq 175^\circ C$	
Pulsed Drain Current	I_{DM}			80		t_{Pmax} limited by T_{jmax} $V_{GS} = 15 V, T_c = 25^\circ C$	Fig. 22
Power Dissipation	P_D			145	W	$T_c = 25^\circ C, T_j = 175^\circ C$	Fig. 20
Operating Junction and Storage Temperature	T_j, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design

Package



Part Number	Package	Marking
C3M0075120K1	TO-247-4L LP	C3M0075120K1

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	1200			V	$V_{\text{GS}} = 0 \text{ V}, I_{\text{D}} = 100 \mu\text{A}$	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.8	2.6	3.8	V	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 5 \text{ mA}$	Fig. 11
			2.1		V	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 5 \text{ mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{\text{DS}} = 1200 \text{ V}, V_{\text{GS}} = 0 \text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{\text{GS}} = 15 \text{ V}, V_{\text{DS}} = 0 \text{ V}$	
$R_{\text{DS}(\text{on})}$	Drain-Source On-State Resistance		75	97.5	$\text{m}\Omega$	$V_{\text{GS}} = 15 \text{ V}, I_{\text{D}} = 17.9 \text{ A}$	Fig. 4, 5, 6
			135			$V_{\text{GS}} = 15 \text{ V}, I_{\text{D}} = 17.9 \text{ A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		11		S	$V_{\text{DS}} = 20 \text{ V}, I_{\text{DS}} = 17.9 \text{ A}$	Fig. 7
			10.5			$V_{\text{DS}} = 20 \text{ V}, I_{\text{DS}} = 17.9 \text{ A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		1480		pF	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 0 \text{ V to } 1000 \text{ V}$ $F = 1 \text{ MHz}$ $V_{\text{AC}} = 25 \text{ mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		58				
C_{rss}	Reverse Transfer Capacitance		2.7				
E_{oss}	C_{oss} Stored Energy		32		μJ		Fig. 16
$C_{\text{o(er)}}$	Effective Output Capacitance (Energy Related)		67		pF	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 0 \dots 800 \text{ V}$	Note: 3
$C_{\text{o(tr)}}$	Effective Output Capacitance (Time Related)		96		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		280		μJ	$V_{\text{DS}} = 800 \text{ V}, V_{\text{GS}} = -4 \text{ V/15 V}, I_{\text{D}} = 20 \text{ A}, R_{\text{G(ext)}} = 2.5 \Omega, L = 98 \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		56				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		280		μJ	$V_{\text{DS}} = 800 \text{ V}, V_{\text{GS}} = -4 \text{ V/15 V}, I_{\text{D}} = 20 \text{ A}, R_{\text{G(ext)}} = 2.5 \Omega, L = 156 \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		63				
$t_{\text{d(on)}}$	Turn-On Delay Time		8		ns	$V_{\text{DD}} = 800 \text{ V}, V_{\text{GS}} = -4 \text{ V/15 V}$ $I_{\text{D}} = 20 \text{ A}, R_{\text{G(ext)}} = 2.5 \Omega,$ Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		22				
$t_{\text{d(off)}}$	Turn-Off Delay Time		29				
t_f	Fall Time		11				
$R_{\text{G(int)}}$	Internal Gate Resistance		9.0		Ω	$f = 1 \text{ MHz}, V_{\text{AC}} = 25 \text{ mV}$	
Q_{gs}	Gate to Source Charge		17		nC	$V_{\text{DS}} = 800 \text{ V}, V_{\text{GS}} = -4 \text{ V/15 V}$ $I_{\text{D}} = 17.9 \text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		18				
Q_g	Total Gate Charge		55				

Note (3): $C_{\text{o(en)}}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 800V

$C_{\text{o(tr)}}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 800V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 9\text{ A}$, $T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 9\text{ A}$, $T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		27	A	$V_{GS} = -4\text{ V}$, $T_c = 25^\circ\text{C}$	
I_{SM}	Diode pulse Current		80	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recover time	20		ns	$V_{GS} = -4\text{ V}$, $I_{SD} = 20\text{ A}$, $V_R = 800\text{ V}$ $dif/dt = 5280\text{ A}/\mu\text{s}$, $T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	376		nC		
I_{rrm}	Peak Reverse Recovery Current	25		A		
t_{rr}	Reverse Recover time	28		ns		
Q_{rr}	Reverse Recovery Charge	338		nC	$V_{GS} = -4\text{ V}$, $I_{SD} = 20\text{ A}$, $V_R = 800\text{ V}$ $dif/dt = 1305\text{ A}/\mu\text{s}$, $T_J = 175^\circ\text{C}$	
I_{rrm}	Peak Reverse Recovery Current	16		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta,JC}$	Thermal Resistance from Junction to Case	0.88	°C/W		Fig. 21

Typical Performance

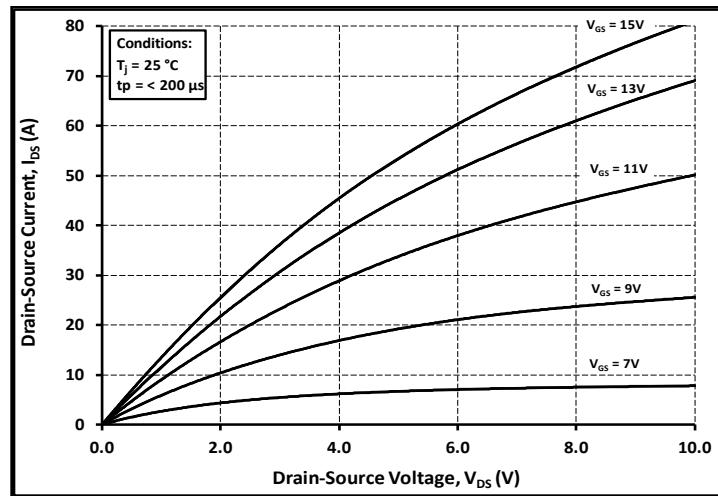
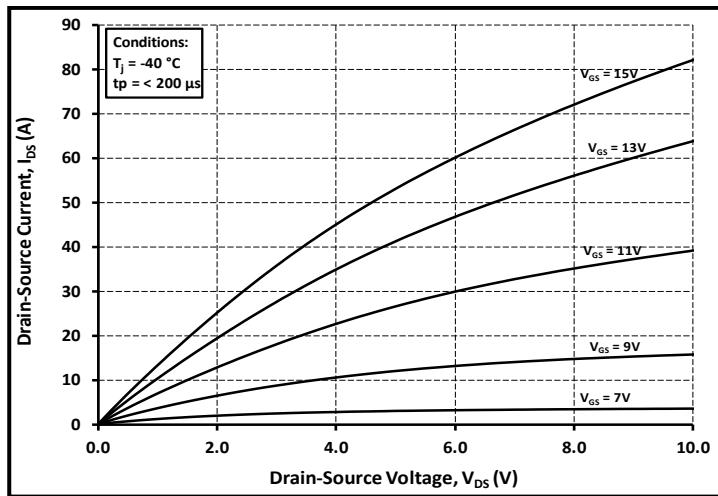
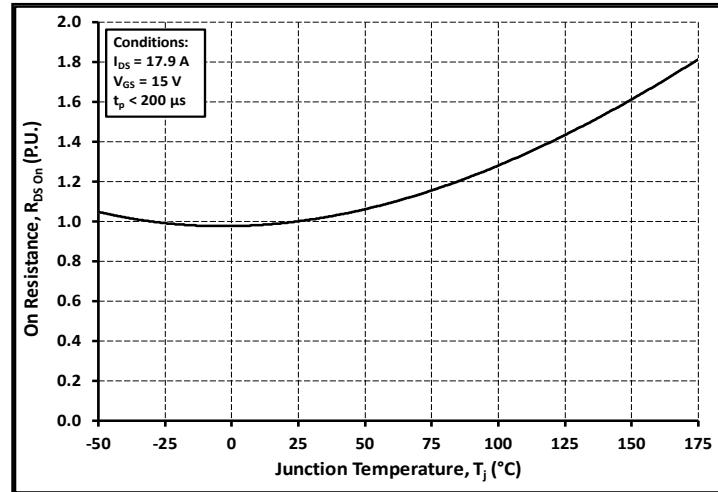
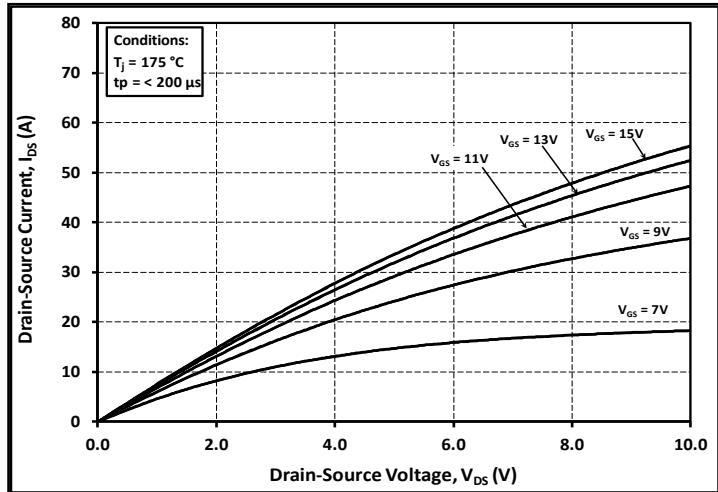
Figure 1. Output Characteristics $T_J = -40\text{ }^{\circ}\text{C}$ Figure 2. Output Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ Figure 3. Output Characteristics $T_J = 175\text{ }^{\circ}\text{C}$

Figure 4. Normalized On-Resistance vs. Temperature

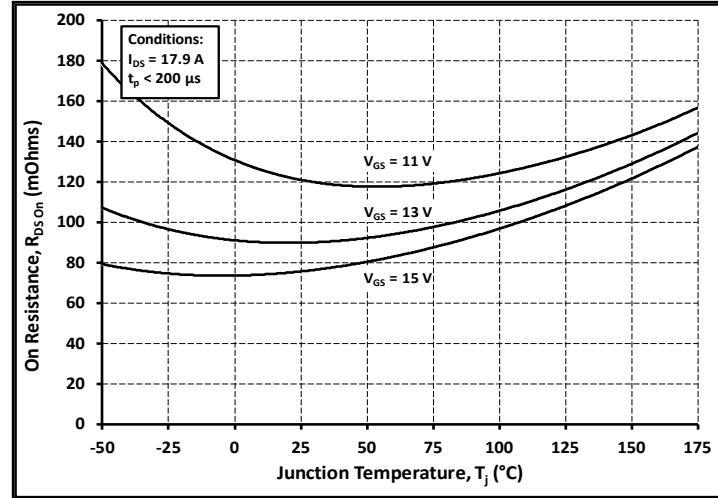
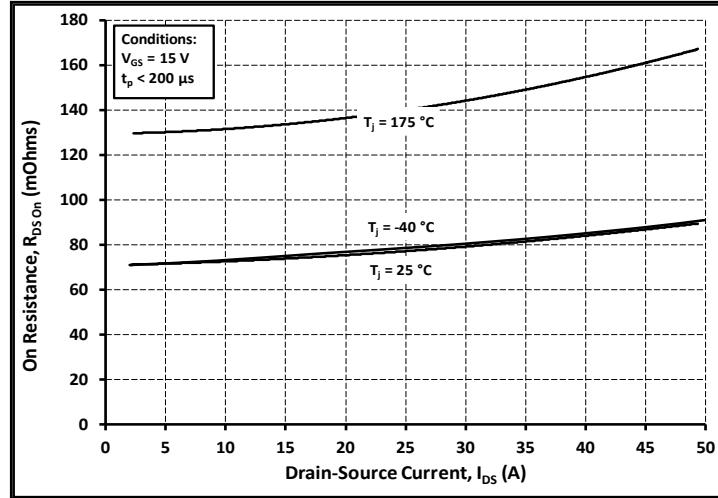
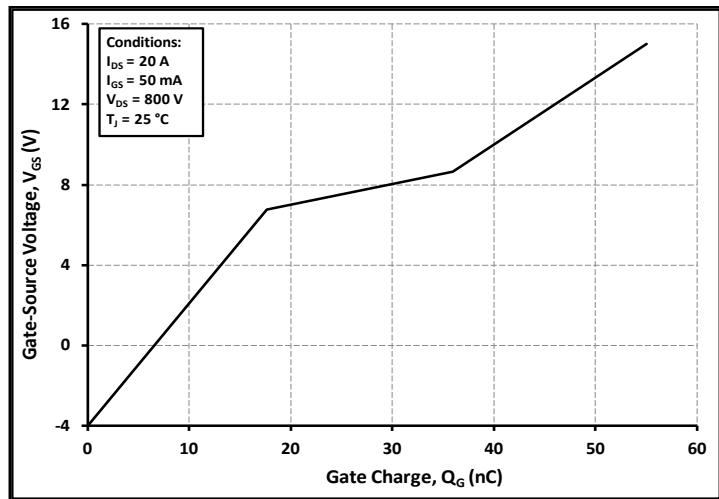
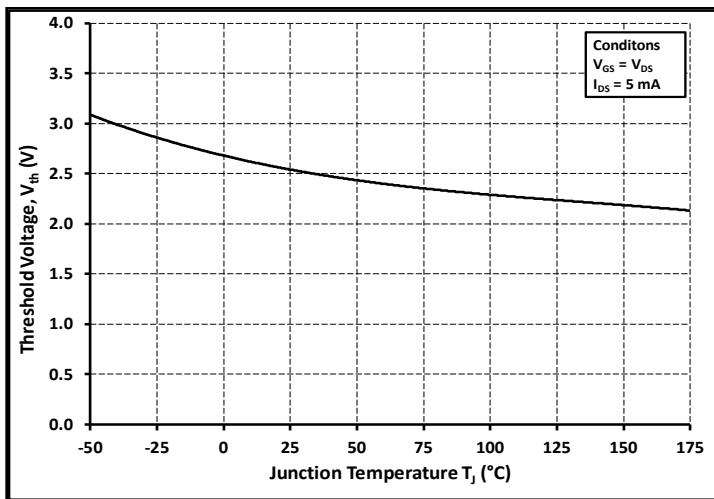
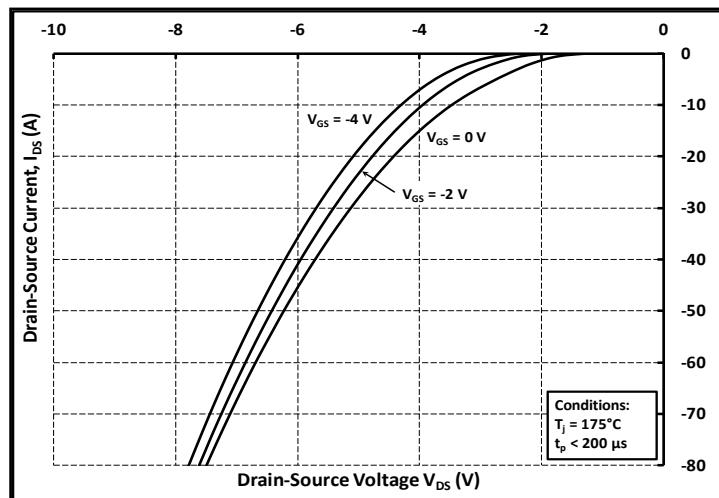
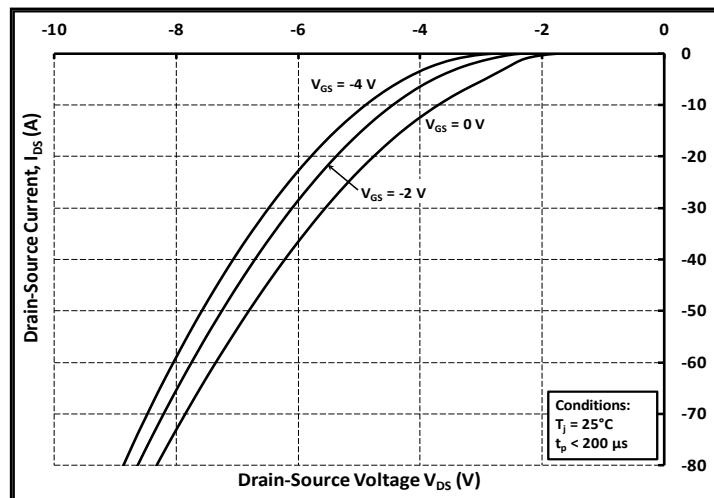
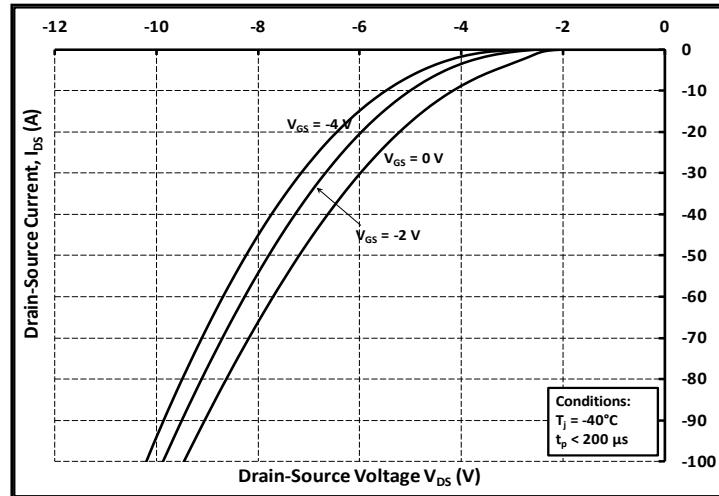
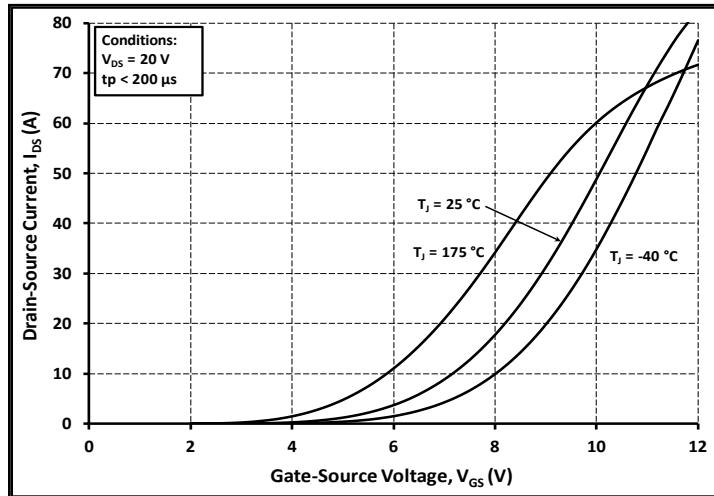


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance



Typical Performance

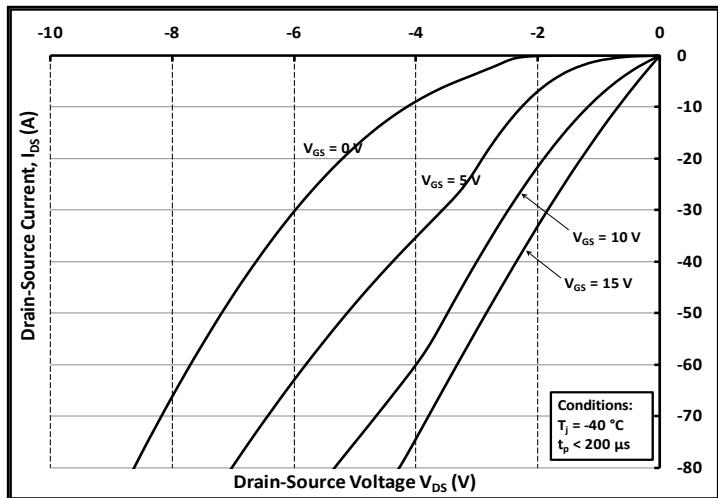
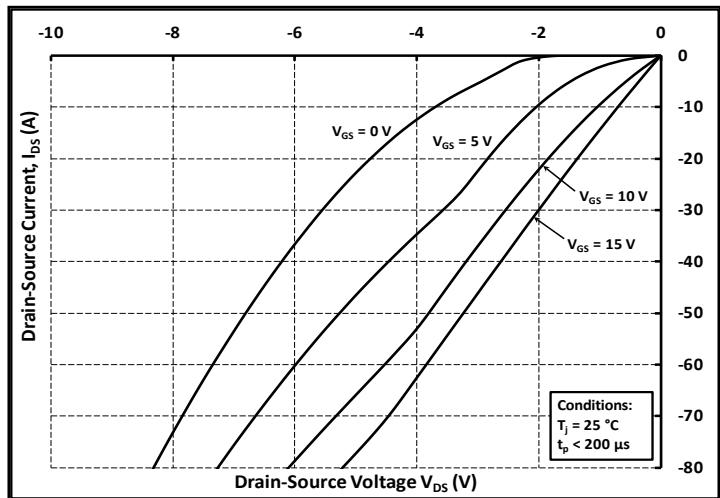
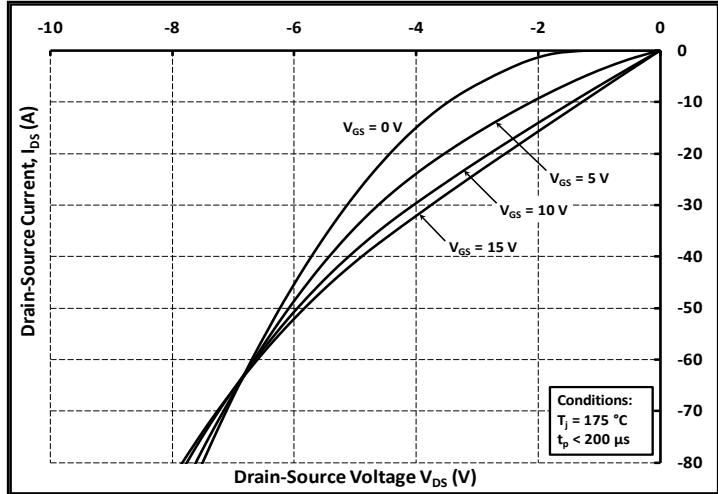
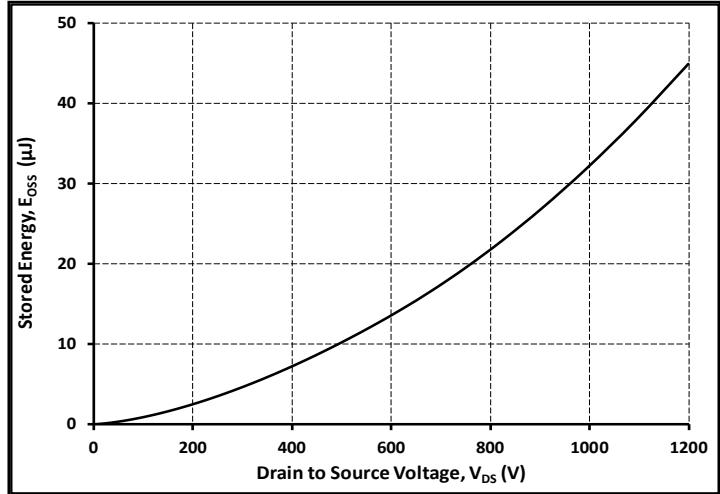
Figure 13. 3rd Quadrant Characteristic at $-40\text{ }^{\circ}\text{C}$ Figure 14. 3rd Quadrant Characteristic at $25\text{ }^{\circ}\text{C}$ Figure 15. 3rd Quadrant Characteristic at $175\text{ }^{\circ}\text{C}$ 

Figure 16. Output Capacitor Stored Energy

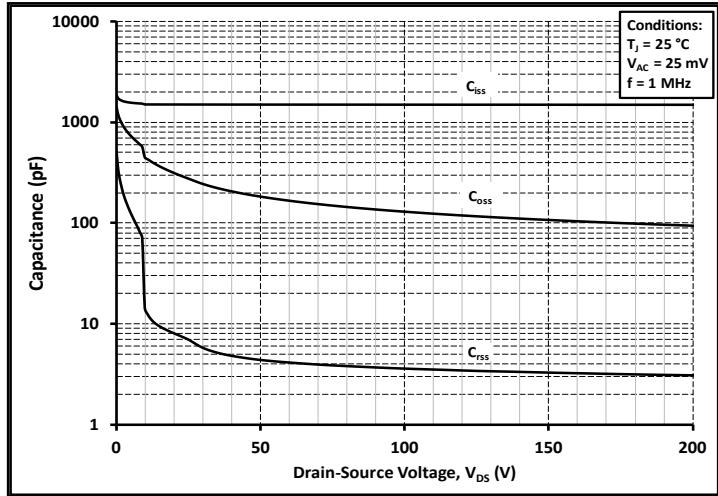


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

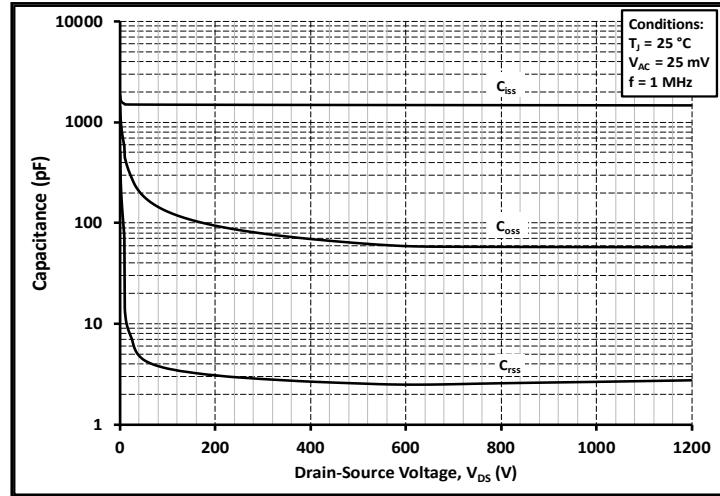


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

Typical Performance

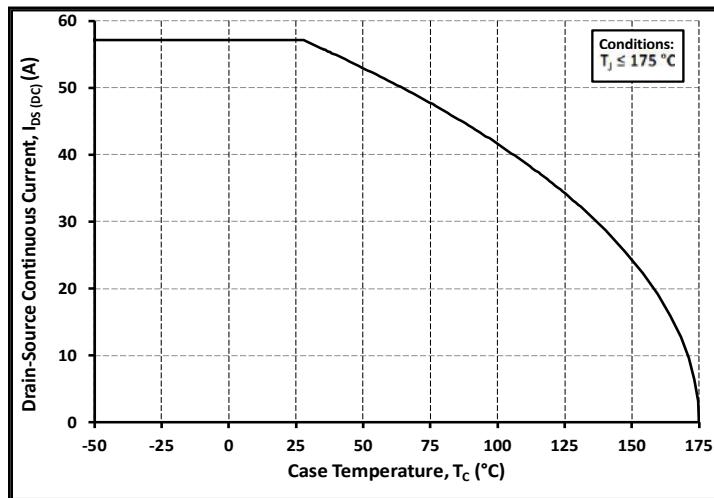


Figure 19. Continuous Drain Current Derating vs. Case Temperature

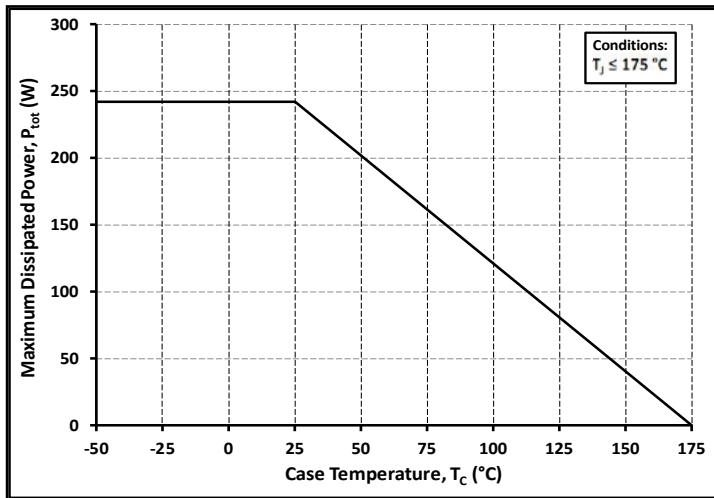


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

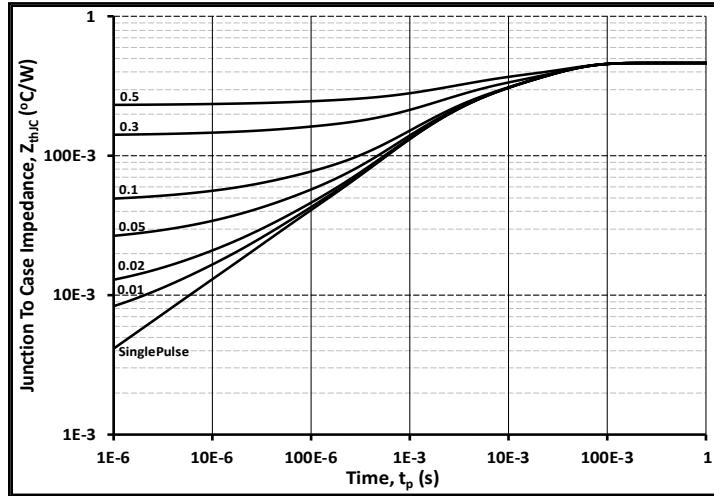


Figure 21. Transient Thermal Impedance (Junction - Case)

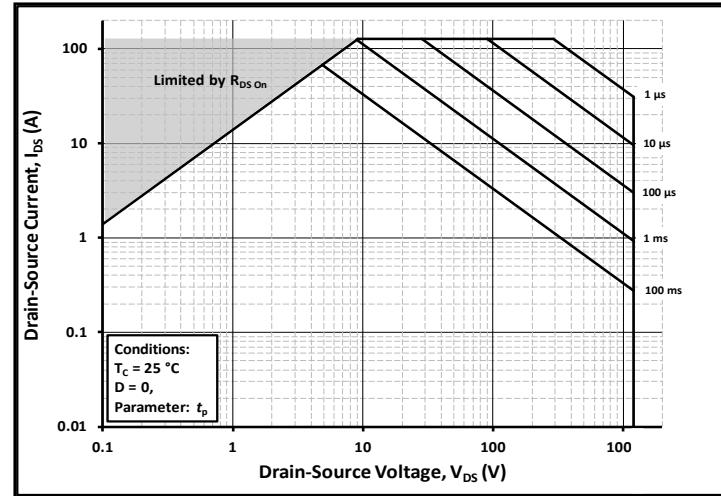


Figure 22. Safe Operating Area

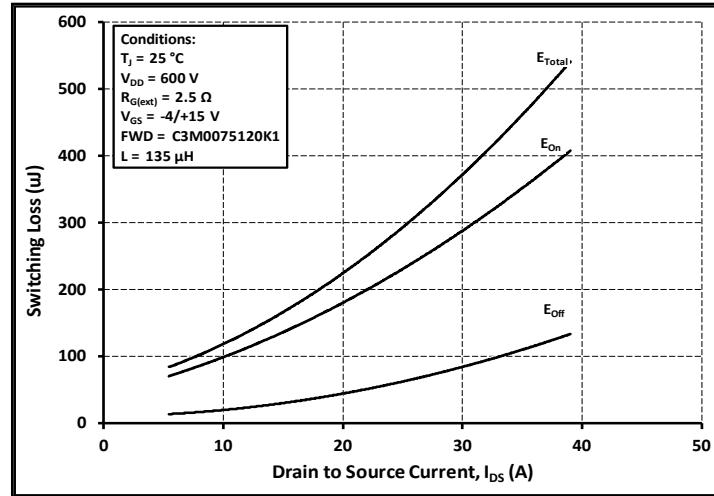


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600V$)

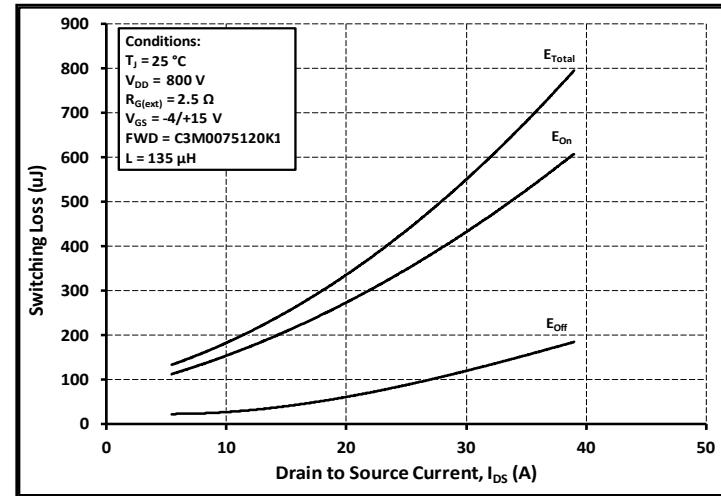


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800V$)

Typical Performance

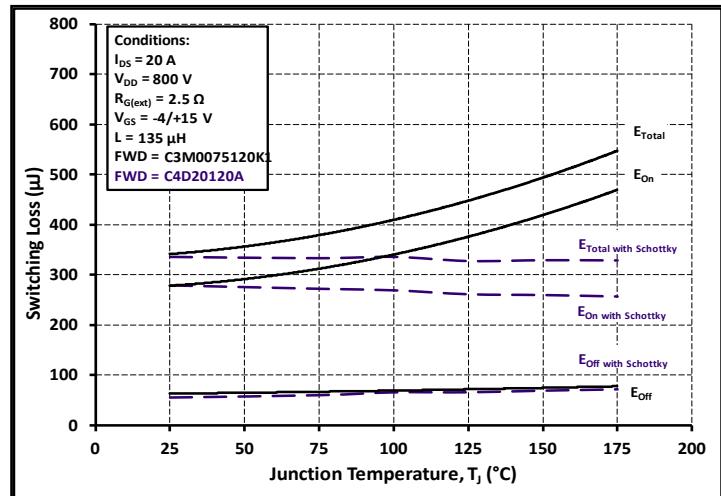
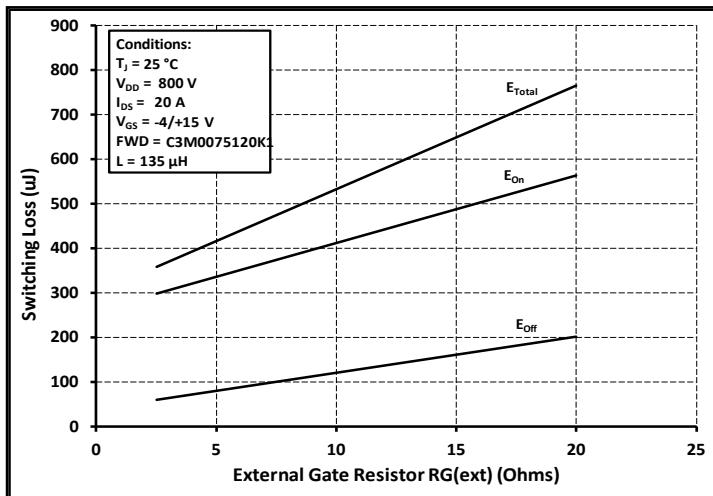
Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$

Figure 26. Clamped Inductive Switching Energy vs. Temperature

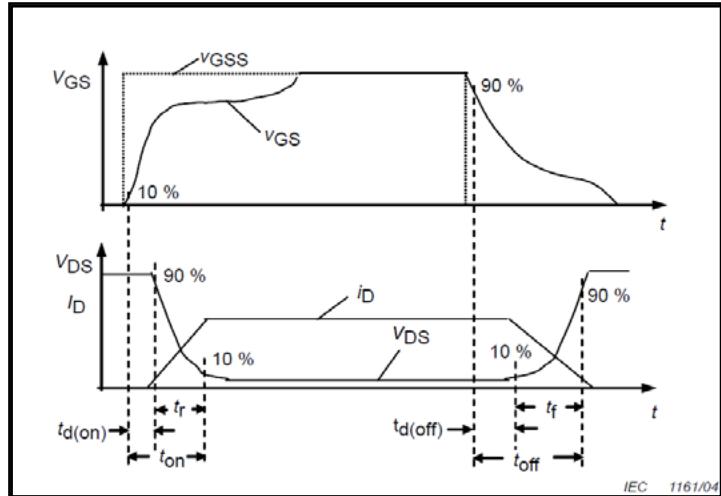
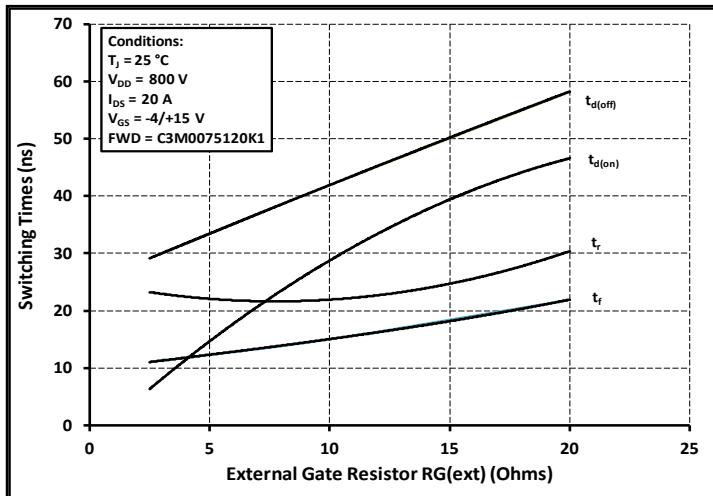
Figure 27. Switching Times vs. $R_{G(\text{ext})}$

Figure 28. Switching Times Definition

Test Circuit Schematic

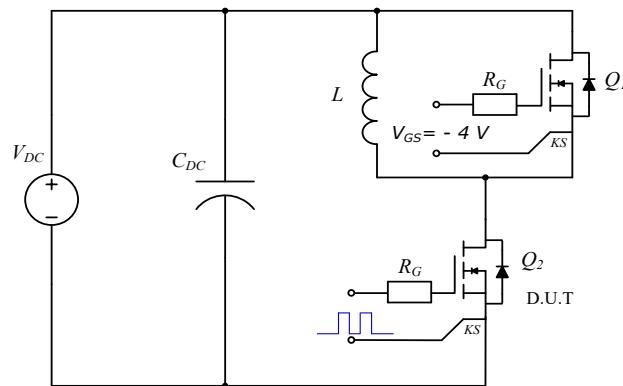
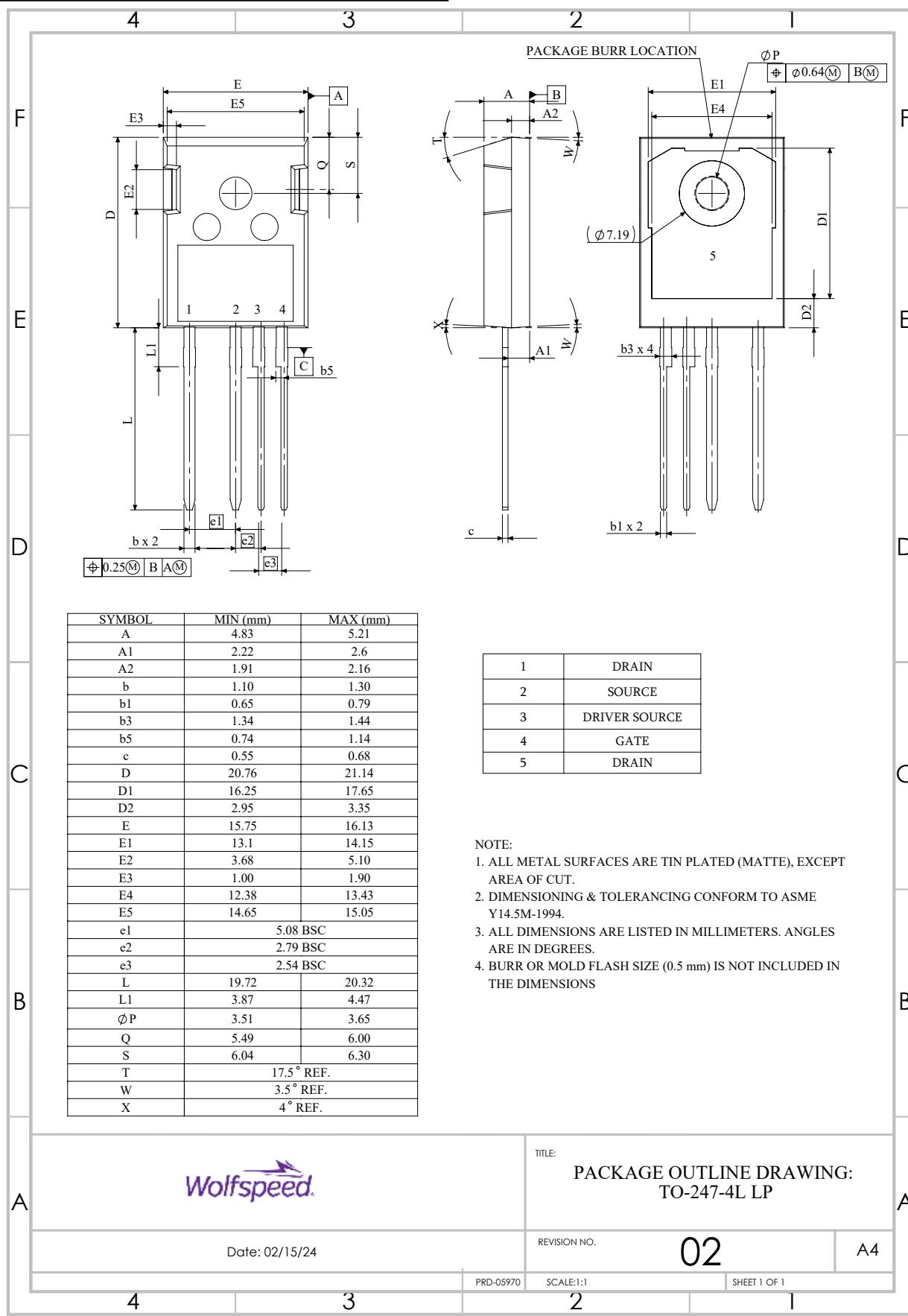


Figure 29. Clamped Inductive Switching Waveform Test Circuit

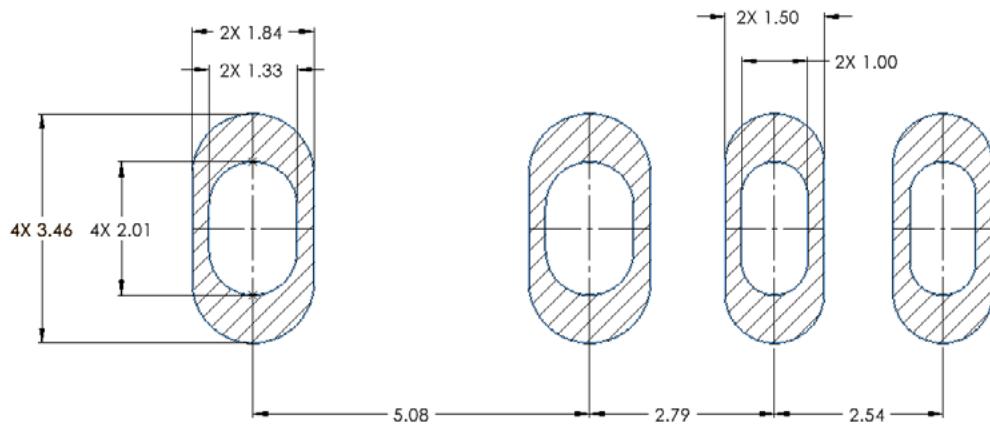
Package Dimensions





Recommended Solder Pad Layout

All dimensions in mm





Revision history

Document Version	Date of release	Description of changes
1.0	April-2024	Initial datasheet



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Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power

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