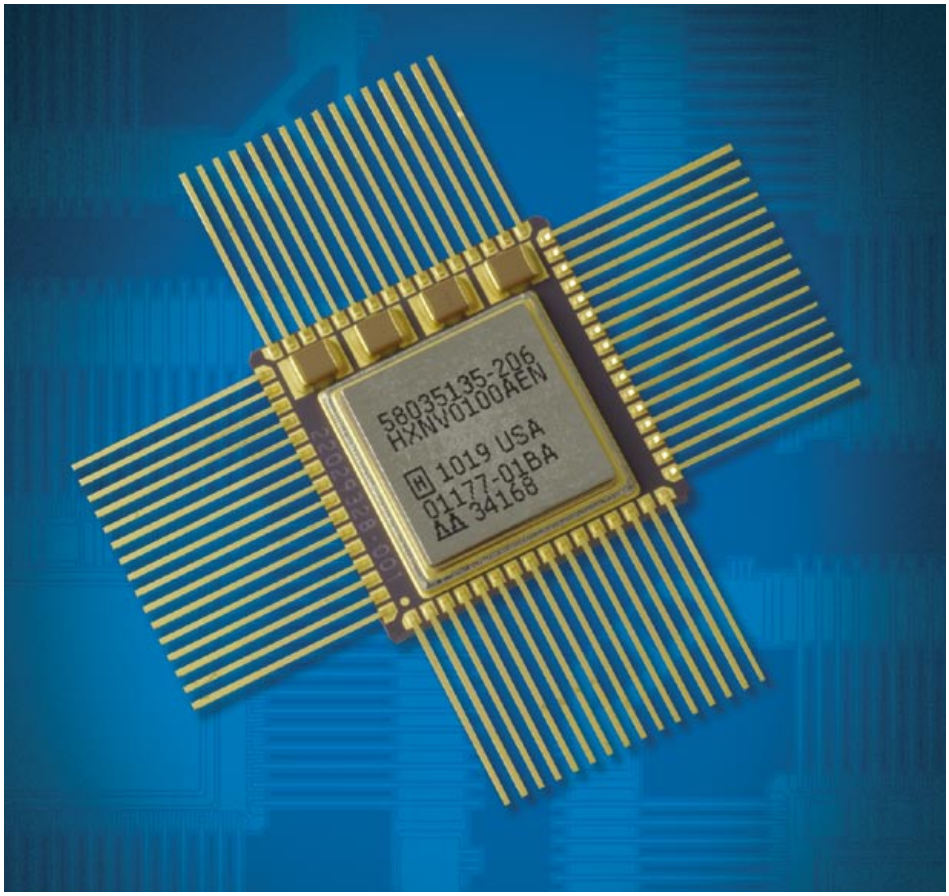
HXNV0100

Honeywell

HXNV0100 1Megabit
64K x 16 Non-Volatile Magneto-Resistive RAM

Features

- Fabricated on S150 Silicon On Insulator (SOI) CMOS Underlayer Technology
- 150 nm Process (Leff = 130 nm)
- Total Dose Hardness ≥ $1x10^6$ rad (Si)
- Dose Rate Upset Hardness ≥ $1x10^9$ rad(Si)/s
- Dose Rate Survivability ≥$1x10^{12}$ rad(Si)/s
- Soft Error Rate ≤$1x10^{-10}$ upsets/bit-day
- Neutron Hardness ≥ $1x10^{14}$ N/cm^2
- No Latchup
- Read Access Time ≤ 80 ns
- Read Cycle Time ≤ 110 ns
- Write Cycle Time ≤ 140 ns
- Typical Operating Power ≤500 mW
- Unlimited Read (>$1x10^{15}$ Cycles)
- > 15 years Data Retention
- Synchronous Operation
- Single-Bit Error Detection & Correction (ECC)
- Dual Power Supplies
- 1.8 V ± 0.15V, 3.3 V ± 0.3V
- 3.3V CMOS Compatible I/O
- Standard Operating Temperature Range is -40°C to +105°C
- Package: 64 Lead Shielded Ceramic Quad Flat Pack

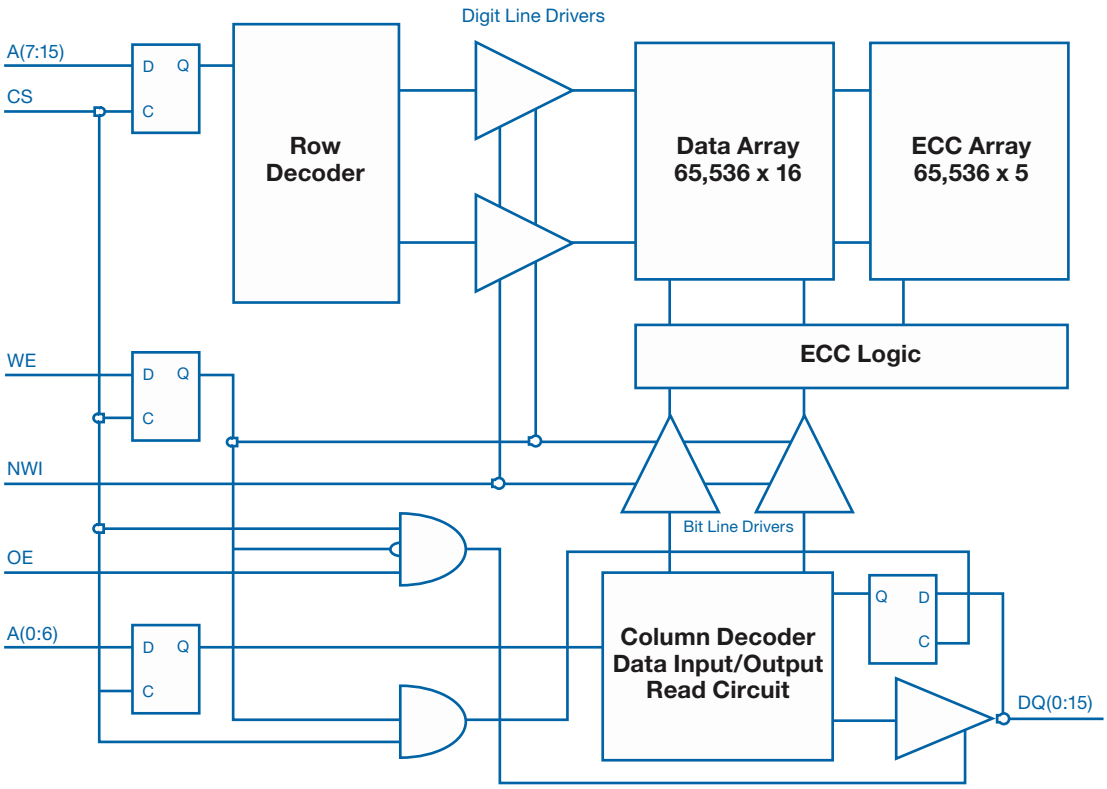


The 64K x 16 radiation hardened low power non-volatile Magneto-Resistive Random Access Memory (MRAM) is a high performance 65,536 word x 16-bit Magneto-Resistive RAM with industry-standard functionality.

The MRAM is designed for very high reliability. Redundant write control lines, error correction coding and low-voltage write protection ensure the correct operation of the memory and protection from inadvertent writes.

Integrated Power Up and Power Down circuitry controls the condition of the device during power transitions. It is fabricated with Honeywell's radiation hardened Silicon On Insulator (SOI) technology, and is designed for use in low-voltage systems operating in radiation environments. The MRAM operates over a temperature range of -40°C to +105°C and is operated with 3.3 ± 0.3V and 1.8 ± 0.15V power supplies.

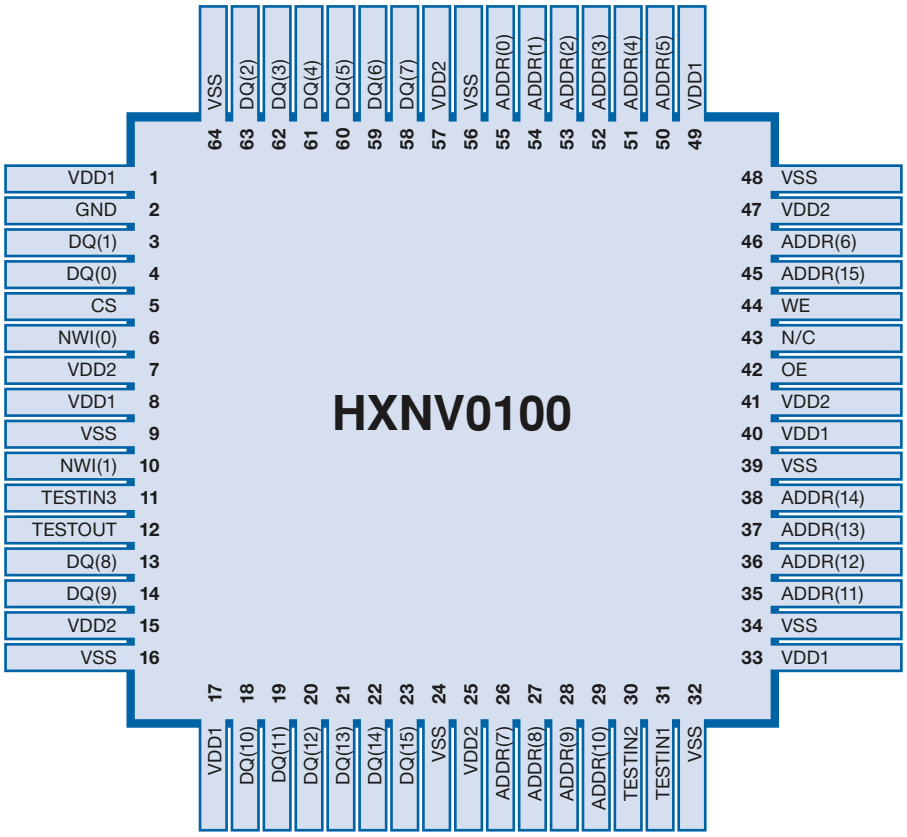
Functional Block Diagram



Signal Description

Signal	Definition
A(0:6)	Column Select Address Input. Signals which select a column within the memory array.
A(7:15)	Row Select Address Input. Signals which select a row within the memory array.
DQ(0:15)	Data Input/Output Signals. Bi-directional data pins which serve as data outputs during a read operation and as data inputs during a write operation.
CS	Chip select. The rising edge of CS will clock in the address and WE signals and latch the DQ outputs.
WE	Write Enable. Active high write enable. High state at rising edge of CS initiates a write cycle. Low state at rising edge of CS initiates a read cycle.
OE	Output Enable. Active high output enable.
NWI0 NWI1	Not Write Inhibit – When set low, these signals inhibit writes to the memory. A high level allows the memory to be written. NWI0 controls lower order 32K A(15)=0. NWI1 controls the upper order 32K A(15)=1. (Note the VIL and VIH requirements for NWI)
TESTOUT	This output signal is for Honeywell test purposes only. It must be left floating.
TESTIN1 TESTIN2 TESTIN3	These signals are for Honeywell test purposes only. These must be grounded. (Failure to hold these pins low may result in permanent loss of functionality)
VDD1	DC Power Source Input: 1.8V
VDD2	DC Power Source Input: 3.3V
N/C	No Connect, (can be tied to any supply)

Package Pinout



Signal Description

Function Truth Table

NWI	CS	OE	WE	Data Outputs	Function
1	_/ (rising edge)	X	1	Hi Z	Write cycle
X	_/ (rising edge)	1	0	Lo Z	Read Cycle
0	X	X	X	Dependent on controls	Writes inhibited

Output Driver Truth Table

NWI	CS	OE	WE(1)	Data Outputs	Function
X	0	X	X	Hi Z	Outputs Disabled
X	X	0	X	Hi Z	Outputs Disabled
X	X	X	1	Hi Z	Outputs Disabled
X	1	1	0	Low Z	Outputs Enabled

(1) Latched by rising edge of CS

RAM and ROM Functional Capability

This MRAM incorporates two write control signals allowing the two sections of the memory to be controlled independently. The two NOT WRITE INHIBIT signals, NWI(0) and NWI(1), allow one section of the device to operate as a RAM and the other to operate as a ROM at the full control of the user. These signals should be hard wired to VDD2 or ground if active control is not needed. If control is desired, maximum 5K ohms pull up or down resistor should be used with care taken to insure that the VIH and VIL for the NWI pins are met.

SOI and Magnetic Memory Technology

Honeywell's S150 Silicon On Insulator (SOI) CMOS is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. The 150 nm process is a technology with a 31Å gate oxide for 1.8 V transistors and 59Å gate oxide for 3.3 V transistors. The memory element is a magnetic tunnel junction (MTJ) that is non-volatile and composed of a magnetic storage layer structure and a magnetic pinned layer structure separated by an insulating tunnel barrier. During a write cycle, the storage layer is written by the application of two orthogonal currents using row-and-column addressing. The resistance of the MTJ depends on the magnetic state of the storage layer structure, which uses the pinned layer structure as a reference, and which enables signal sensing, amplification, and readback. The resistance change from the memory element is a result of the change in Tunneling Magneto-Resistance (TMR) between the storage and pinned layers that depends on the magnetic state of the storage layer. The HXNV0100 is not subject to memory related wear out mechanisms.

Error Correction Code (ECC)

Hamming 5-Bit ECC

A 5-bit Hamming ECC is generated for all data written into memory. This code allows for the correction of all single-bit errors per address. On a read cycle, a data word is read from memory and corrected, if necessary, before being placed on the output data bus.

There is no change made to the actual data in the memory cells based on the ECC results. Actual data in memory are changed only upon writing new values.

Radiation Characteristics

Total Ionizing Radiation Dose

The MRAM will meet all stated functional and electrical specifications after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications, post rebound, after an operational period of 15 years. Total dose hardness is assured by wafer level testing of process monitor transistors using 10 KeV X-ray. Parameter correlations have been made between 10 KeV X-rays applied at a dose rate of 5x105 rad(SiO2)/min at T= 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The MRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse, up to the specified transient dose rate upset specification, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ±10%), it is suggested that stiffening capacitance be placed near the package VDD2 and ground (GND) and near the package VDD1 and ground (GND).

It is also recommended that the inductance between the MRAM package leads and the stiffening capacitance be less that 1.0 nH. If there are no operate through or valid stored-data requirements, typical circuit board mounted de-coupling capacitors are recommended. The MRAM will meet any functional or electrical specification after exposure to a radiation pulse up to the transient dose rate survivability specification, when applied under recommended operating conditions. Note that the current conducted during the pulse by the MRAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The MRAM will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions. This assumes equivalent neutron energy of 1 MeV.

Soft Error Rate

The MRAM is capable of meeting the specified Soft Error Rate (SER) under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment for geosynchronous orbits.

Latchup

The MRAM will not latch up under any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR-type latchup structures. Sufficient transistor body tie connections to the p-channel and n-channel substrates are made to ensure no source/drain snapback occurs.

Radiation-Hardness Ratings

Parameter	Limits	Units	Test Conditions VDD1 = 1.65 TO 1.95 VOLTS VDD2 = 3.00 TO 3.60 VOLTS TC = -40 TO 105 °C
Total Dose: H-Level	≥ 1 x 10^{6}	Rads(Si)	TA =25°C, X-Ray or Co60
Soft Error Rate:	≤ 1 x 10^{-10}	Upsets/bit-day (1)	Read or Write
Transient Dose Rate Upset	≥ 1 x 10^{9}	Rads(Si)/s	Pulse Width = 20ns +/- 5ns FWHM, X-Ray
Transient Dose Rate Survivability	≥ 1 x 10^{12}	Rads(Si)/s	Pulse Width = 18-52ns FWHM, X-Ray
Neutron Fluence	1x10^{14}	N/cm^2	1 MeV equivalent energy

(1) Adams 90% Worst-Case environment under worst-case operating conditions for voltage, temperature and memory operating conditions (e.g. static or dynamic operation).

Magnetic Field Characteristics

The MRAM will meet all stated functional and electrical specifications over the entire operating temperature range when exposed to magnetic fields up to the rating supplied below. Exposure to larger magnetic fields may permanently affect functionality.

Magnetic Field Rating

Parameter	Limits	Units	Test Conditions
Magnetic Field	50	Oe	VDD1 = 1.8 Volts, VDD2 = 3.3 Volts T_C = -40°C to 105°C

Recommended Operating Conditions (1)

Symbol	Parameter	Limits Min	Typical	Max	Units
VDD1	Positive Supply Voltage	1.65	1.80	1.95	Volts
VDD2	Positive Supply Voltage	3.0	3.3	3.6	Volts
T_C	External Package Temperature	-40	25	105	°C
V_{PIN}	Voltage On Any Pin	-0.3		VDD2+0.3	Volts

(1) Voltages referenced to GND

Electrical Specifications

Absolute Maximum Ratings (1)

Symbol	Parameter	Ratings Min	Max	Units
VDD1	Positive Supply Voltage (2)	-0.5	2.5	Volts
VDD2	Positive Supply Voltage (2)	-0.5	4.6	Volts
V_{PIN}	Voltage on Any Pin (2)	-0.5	VDD2+ 0.5	Volts
T_{Exp}	Maximum Junction Temperature for Sustained Exposure		125 (6)	°C
T_{SOLDER}	Soldering Temperature		260°C	°C *sec(5)
P_D	Package Power Dissipation (3)		2.5	W
P_{JC}	Package Thermal Resistance (Junction to Case)		4.0	°C /W
V_{PROT}	Electrostatic Discharge Protection Voltage (4)	2000		V
T_J	Junction Temperature Silicon		175	°C
T_{MTJ}	MTJ Temperature		160	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS
(3) MRAM power dissipation due to IDDS, IDDOP, and IDDSEI, plus MRAM output driver power dissipation due to external loading must not exceed this specification
(4) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015
(5) Maximum soldering temp of 260°C can be maintained for no more than 180 seconds over the lifetime of the part.
(6) Not to exceed 24 hours duration (or equivalent at temperature using Ea = 1.235 eV)

Capacitance

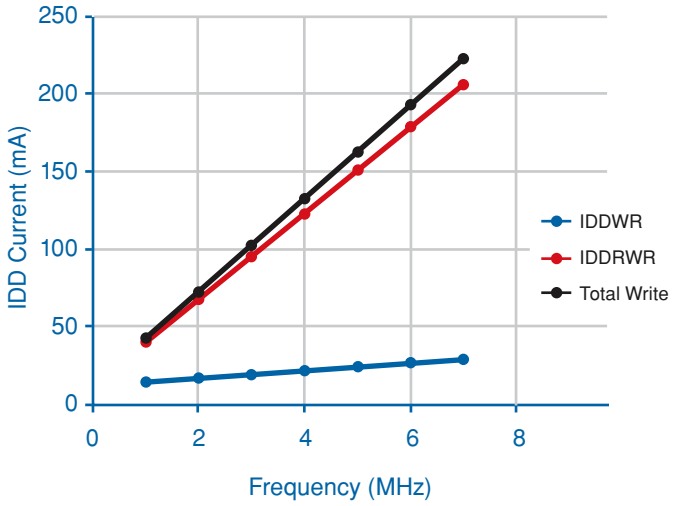
Symbol	Parameter	Limits Min	Max	Units	Test Conditions
C_{IO}	Data I/O Capacitance		15	pF	Vio = VDD2 or VSS, f=1 MHz
C_I	Input Capacitance		12	pF	VI = VDD2 or VSS, f=1 MHz
C_{NWI}	Not Write Inhibit Capacitance		100	pF	

DC Electrical Characteristics (1)

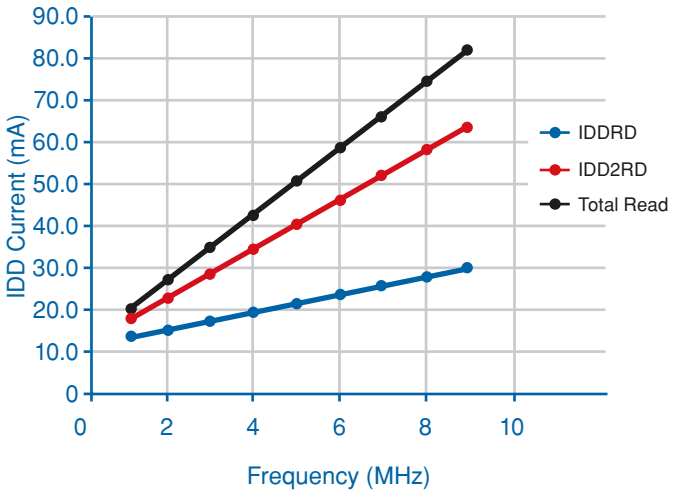
Parameter	Symbol	Min	Max	Units	Comments
VIL	Low Level Input Voltage		0.3*VDD2	V	All inputs except NWI
VIH	High-level Input Voltage	0.7*VDD2		V	All inputs except NWI
VIL (NWI)	Low Level Input Voltage (NWI Signals)		0.5	V	NWI Inputs
VIH (NWI)	High-level Input Voltage (NWI Signals)	0.9*VDD2			NWI Inputs
VOL	Low-level Output Voltage		0.5	V	IOL = 6 mA
VOH	High-level Output Voltage	VDD2-0.5		V	IOH = -6 mA
IOZ	Output Leakage Current	-100	100	µA	Chip deselected or output disabled (CS=0V, OE=0V)
II	Input Leakage Current	-10	10	µA	IIL : Vin=0V, IIH : Vin=VDD2 All inputs except TEST pins
IDDSB	Standby Current				
	VDD1 (1.95V)		12	mA	
	VDD2 (3.60V)		2	mA	
IDDOPWR1	VDD1 current at 1 MHZ write frequency (frequency of CS rising edges)		15	mA	This is the average current comprised of 30 ma during each 140 ns internal MRAM write, and 12 ma standby in between each write
IDDOPWR7	VDD1 current at 7 MHZ write frequency (frequency of CS rising edges)		30	mA	This is the average current comprised of 30 ma during each 140 ns internal MRAM write, and 12 ma standby in between each write
IDD2OPWR1	VDD2 current at 1 MHZ of write frequency (frequency of CS rising edges)		30	mA	This is the average current comprised of 200 ma during each 140 ns internal MRAM write and 2 ma standby in between each write.
IDD2OPWR7	VDD2 current at 7 MHZ of write frequency (frequency of CS rising edges)		196	mA	This is the average current comprised of 200 ma during each 140 ns internal MRAM write and 2 ma standby in between each write.
IDDOPR1	VDD1 current at 1 MHZ of read frequency (frequency of CS rising edges)		14	mA	This is the average current comprised of 30 ma during each 110 ns internal MRAM read, and 12 ma standby in between each read
IDDOPR9	VDD1 current at 9 MHZ of read frequency (frequency of CS rising edges)		30	mA	This is the average current comprised of 30 ma during each 110 ns internal MRAM read, and 12 ma standby in between each read
IDD2OPR1	VDD2 current at 1 MHZ of read frequency (frequency of CS rising edges)		8	mA	Dynamic current is due to driving load capacitance, assumes all 16 outputs switching every read cycle I = 16 * C * V * F + standby current with 70 pF load per output
IDD2OPR9	VDD2 current at 9 MHZ of read frequency (frequency of CS rising edges)		54	mA	Dynamic current is due to driving load capacitance, assumes all 16 outputs switching every read cycle I = 16 * C * V * F + standby current with 70 pF load per output

(1) Post-radiation performance guaranteed at 25°C per MIL-STD-883 method 1019 up to 1MRad(Si) total dose

Max Write Cycle IDDOP



Max Read Cycle IDDOP



Data Endurance

Parameter	Ratings Min	Max	Units	Test Conditions
Data Read Endurance	$1x10^{15}$		Cycles	
Data Write Endurance	$1x10^{12}$		Cycles	

Data Retention

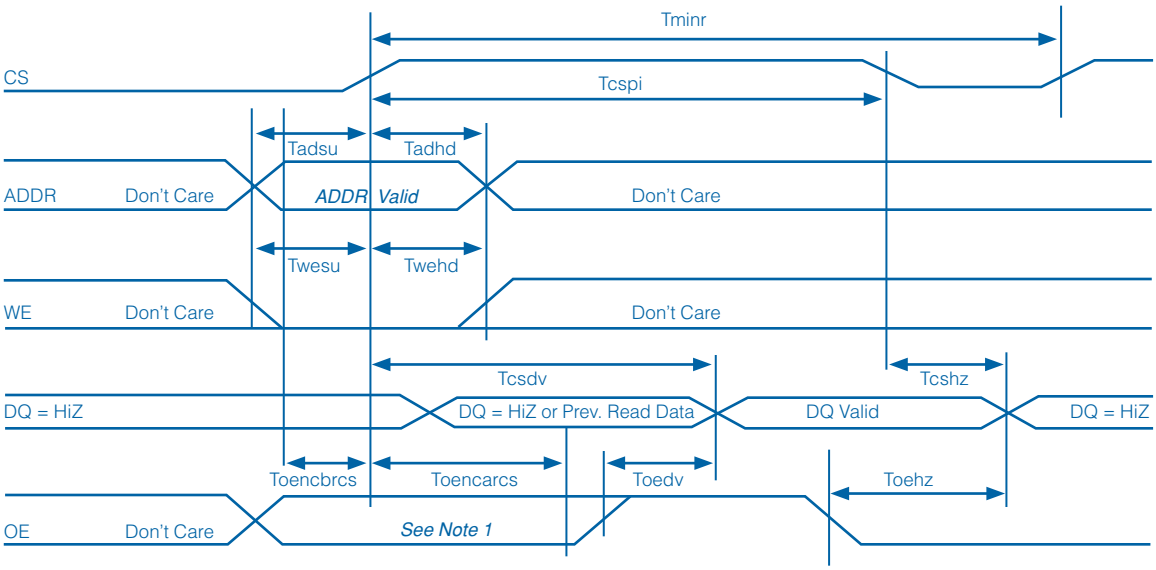
Parameter	Ratings Min	Max	Units	Test Conditions
Data Retention	>15		years	Chip Power On or Off

Read Cycle

The MRAM is synchronous in operation relative to the rising edge of the Chip Select (CS) signal. With the initiation of a CS signal, the address and the Write Enable (WE) signal are latched into the device and the read operation begins. The memory locations are read and compared with the ECC values. Any single bit errors are detected and corrected.

If WE was low when latched in, the data word is sent to the output drivers. In addition to WE low being latched, Output Enable (OE) must be set to a high value to enable the DQ output buffers. OE is not latched, and may be set high before or after the rising edge of CS.

Read Cycle AC Timing Characteristics



(1) If OE is held high during no change window (Toencbrcs+Toencarcs), the DQ pins will drive the previously read data after rising CS.

If OE is held low during no change window, the DQ pins will remain at HiZ.

Name	Description	Min	Max	Units
TADSU	Address Setup Time	5	–	ns
TADHD	Address Hold Time	15	–	ns
TWESU	WE Setup Time	5	–	ns
TWEHD	WE Hold Time	15	–	ns
TCSDV	DQ valid with respect to rising edge of CS	–	80	ns
TOEDV	OE access time	–	15	ns
TOEHZ	OE de-asserted to outputs Hi z	–	15	ns
TCSHZ	CS de-asserted to outputs Hi z	–	20	ns
TMINR	Read Cycle Time	110	–	ns
TCSPI	CS ignored pulse width (glitch tolerance)	–	4	ns
TOENCBRCS	OE rising or falling edge to rising CS time	15	–	ns
TOENCARCS	CS rising edge to OE rising or falling edge	65	–	ns

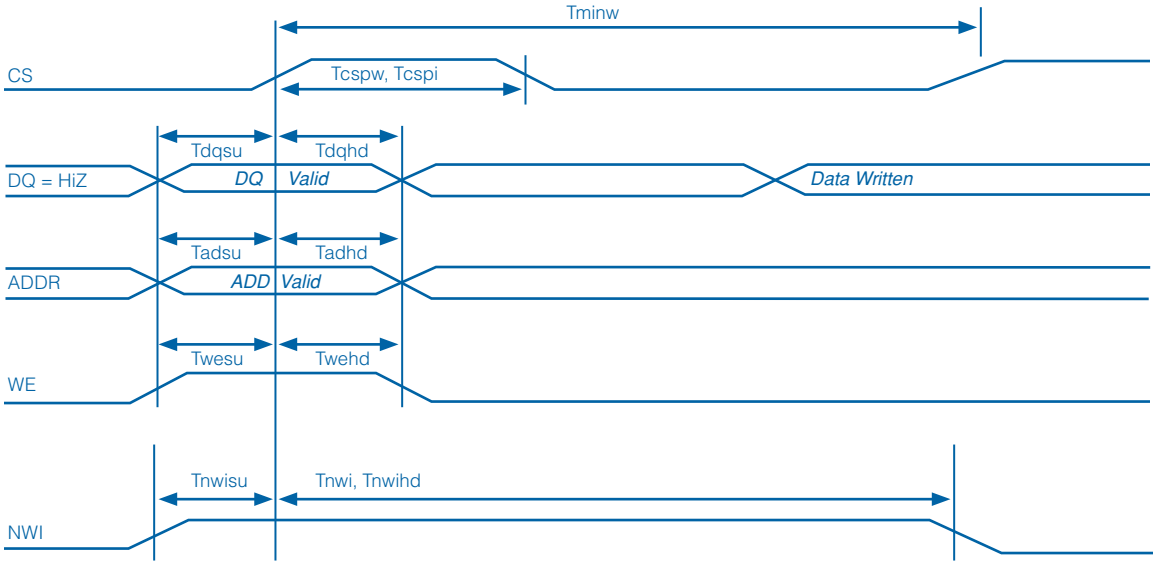
Write Cycle

The MRAM is synchronous in operation relative to the rising edge of the Chip Select (CS) signal. With the initiation of a CS signal, the address and the Write Enable (WE) signal are latched into the device.

The WRITE CYCLE begins by reading the currently addressed value in memory. The current memory data are compared to the data to be written. If the location needs to change value, the data are then written.

The bit cell construction of this device does not provide a method of simply writing a “1” or a “0” to match the data. The “write” to a bit can only change its state, thus the need to read the bit locations first. Only the bits which need to “change state” are actually written.

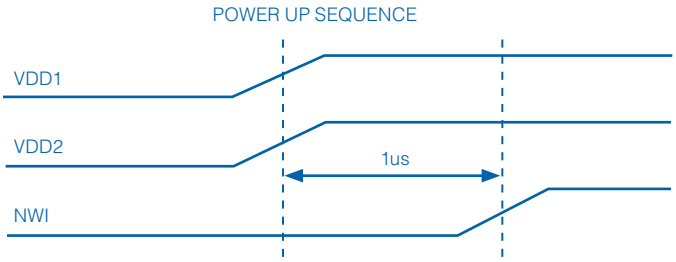
Write Cycle AC Timing Characteristics



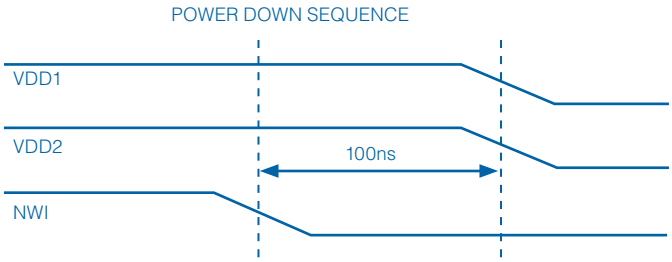
Name	Description	Min	Max	Units
TADSU	Address Setup Time	5	–	ns
TADHD	Address Hold Time	15	–	ns
TWESU	WE Setup Time	5	–	ns
TWEHD	WE Hold Time	15	–	ns
TCSPW	CS Pulse Width (for valid write)	10	–	ns
TCSPI	CS ignored pulse width (glitch tolerance)	–	4	ns
TDQSU	Data Setup Time (relative to CS rising edge)	5	–	ns
TDQHD	Data Hold Time (relative to CS rising edge)	15	–	ns
TNWI	NWI falling edge with respect to CS rising edge to inhibit write	–	40	ns
TMINW	Write Cycle Time	140	–	ns

Power Up Timing

During power-up there are no restrictions on which supply comes up first provided NWI is asserted (low). NWI is de-asserted within 1us of both supplies reaching their 90% values.



Power Down Timing



Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electro migration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Qualification and Screening

The SOI CMOS technology is qualified by Honeywell after meeting the criteria of the General Manufacturing Standards and is also QML Qualified. This qualification is the culmination of years of development, testing, documentation, and on-going process control.

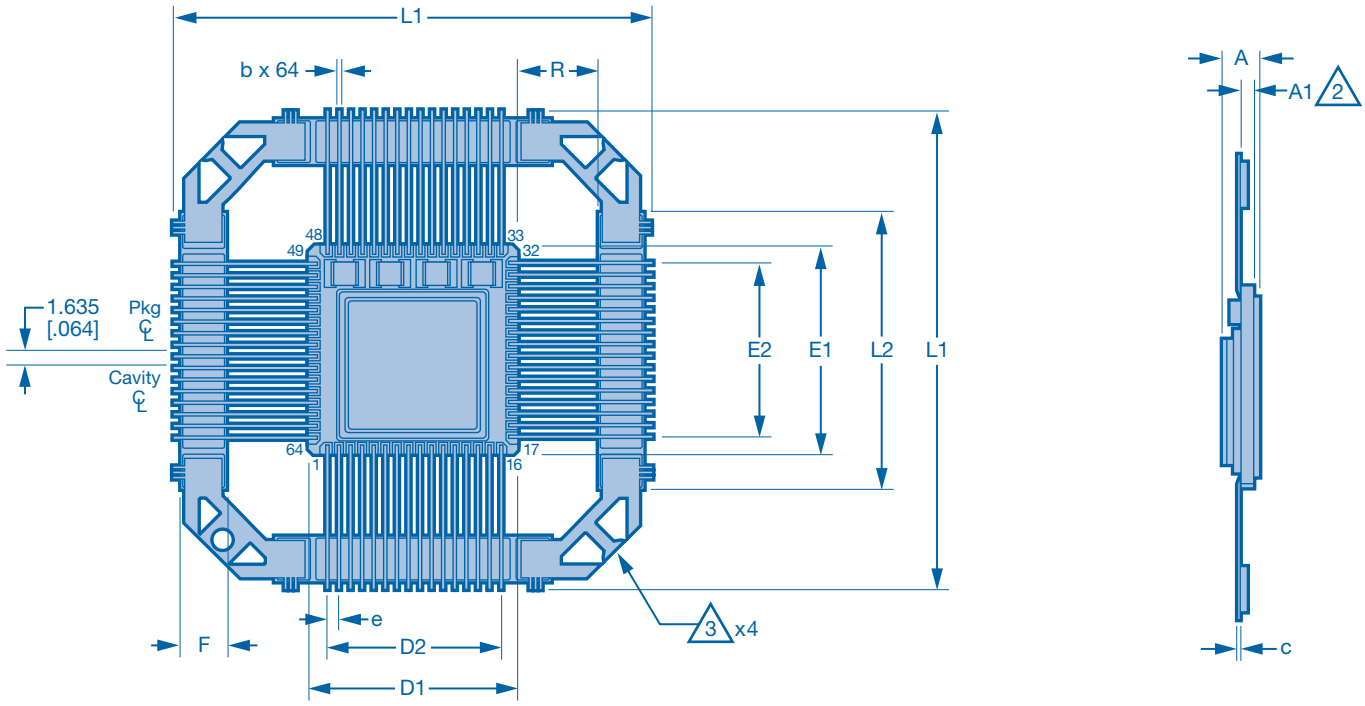
The test flow includes screening units with the defined flow (Class V and Q+ equivalent) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the process and the products are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively, as defined by Honeywell's Quality Management Plan.

Group A	Final Lot Acceptance Electrical Tests
Group B	Mechanical – Dimensions (1), Bond Strength, Solvents, Die Shear, Solderability, Lead Integrity, Seal, Acceleration
Group C	Life Tests – 1000 hours at 105°C or equivalent
Group D	Package related mechanical tests – Shock, Vibration, Accel, Salt (1), Seal, Lead Finish Adhesion, Lid Torque, Thermal Shock, Temp Cycle, Moisture Resistance
Group E	Radiation Tests

(1) Testing performed by package supplier.

Package Outline

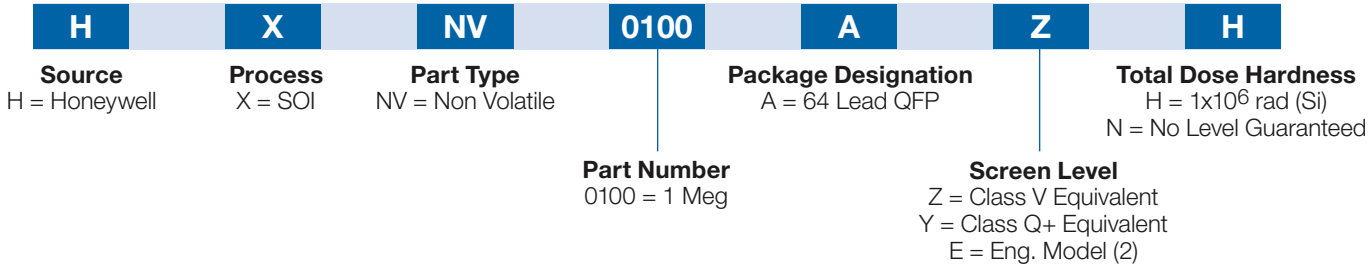
The 64 Lead Shielded Ceramic QFP Package, including external capacitors. Magnetic shielding is tied to ground on the package.



1. Controlling dimensions are in millimeters.
2. A1 is the total thickness of the top shield, lid, sear ring, ceramic body, bottom shield, and shield adhesives.
3. Lead frame corners are trimmed to fit into carriers.

Symbol	Common Dimensions - Millimeters			Common Dimensions - Inches		
	Min	Nom	Max	Min	Nom	Max
A	3.86	4.29	4.75	.152	.169	.187
A1	1.44	1.60	1.76	.057	.063	.070
b	0.41	0.46	0.51	.016	.018	.020
c	0.10	0.15	0.20	.004	.006	.008
D1/E1	22.63	22.86	23.09	.891	.900	.909
D2/E2	18.92	19.05	19.18	.745	.750	.755
e	---	1.27	---	---	.050	---
F	4.44	5.08	5.72	.175	.200	.225
L1	---	---	52.58	---	---	2.070
L2	30.10	30.48	30.86	1.185	1.200	1.215
R	8.03	---	---	.316	---	---

Ordering Information (1)



(1) To order parts or obtain technical assistance, call 1-800-323-8295
(2) Engineering Model Description: Parameters are tested from -40°C to 105°C, 24-hour burn-in, no radiation guarantee.

QCI Testing (1)

Classification	QCI Testing
QML Q+ Equivalent	No lot specific testing performed. (2)
V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywell.com/microelectronics.

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N61-0995-000-000
June 2010