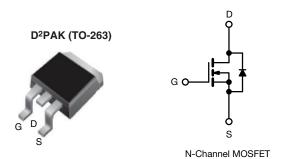
Vishay Siliconix

COMPLIANT

HALOGEN

**FREE** 

# **E Series Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V) at T <sub>J</sub> max. 650				
R <sub>DS(on)</sub> typ. (Ω) at 25 °C	$V_{GS} = 10 \text{ V}$	0.057		
Q <sub>g</sub> max. (nC)	74			
Q <sub>gs</sub> (nC) 19				
Q <sub>gd</sub> (nC)	15			
Configuration	Single			

#### **FEATURES**

- 4<sup>th</sup> generation E series technology
- ullet Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance (Co(er))
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

### **APPLICATIONS**

- · Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)			
Lead (Pb)-free and halogen-free	SiHB065N60E-GE3			
Lead (Pb)-free and halogen-free	SiHB065N60E-T1-GE3			

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	600	V	
Gate-source voltage			$V_{GS}$	± 30	7 v	
Continuous dusin surrent /T 150 °C\	V <sub>GS</sub> at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I <sub>D</sub>	40	А	
Continuous drain current (T <sub>J</sub> = 150 °C)		T <sub>C</sub> = 100 °C		25		
Pulsed drain current a			I <sub>DM</sub>	116	İ	
Linear derating factor				2	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	226	mJ	
Maximum power dissipation			P <sub>D</sub>	250	W	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Drain-source voltage slope $T_J = 125 ^{\circ}\text{C}$		dV/dt	100	V/ns		
Reverse diode dV/dt d			50			
Soldering recommendations (peak temperature) <sup>c</sup> For 10 s				260	°C	

#### **Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b.  $V_{DD}$  = 120 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_q$  = 25  $\Omega$ ,  $I_{AS}$  = 4 A
- c. 1.6 mm from case
- d.  $I_{SD} \leq I_D$ , dI/dt = 400 A/ $\mu$ s, starting  $T_J = 25$  °C



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THERMAL RESISTANCE RATINGS					
PARAMETER SYMBOL TYP. MAX. UNIT					
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W	
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.5	G/ <b>V</b> V	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = 250 μA	600	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.72	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	· V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	-	5	V
Coto pouros logicos	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Gate-source leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zava sata valtasa duain avuvant		V <sub>DS</sub> =	600 V, V <sub>GS</sub> = 0 V	-	-	1	μΑ
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 V	, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	10	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 16 A	-	0.057	0.065	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub>	= 20 V, I <sub>D</sub> = 16 A	-	12	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>		$V_{GS} = 0 V$ ,	-	2700	-	
Output capacitance	C <sub>oss</sub>	,	V <sub>DS</sub> = 100 V,	-	102	-	
Reverse transfer capacitance	C <sub>rss</sub>		f = 1 MHz		5	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	93	-	pF
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	593	-	
Total gate charge	Qg			-	49	74	
Gate-source charge	Q <sub>gs</sub>	$V_{GS} = 10 \text{ V}$ $I_D = 16 \text{ A}, V_{DS} = 480 \text{ V}$		-	19	-	nC
Gate-drain charge	Q <sub>gd</sub>			-	15	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 16 A,		-	28	56	ns
Rise time	t <sub>r</sub>			-	46	92	
Turn-off delay time	t <sub>d(off)</sub>		$V_{GS} = 10 \text{ V}, R_g = 9.1 \Omega$		54	108	
Fall time	t <sub>f</sub>	1		-	13	26	
Gate input resistance	$R_g$	f = 1 MHz, open drain		0.3	0.7	1.4	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	40	^
Pulsed diode forward current	I <sub>SM</sub>			-	-	116	- A
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 16 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 16 A, di/dt = 100 A/µs, V <sub>R</sub> = 400 V		-	382	764	ns
Reverse recovery charge	Q <sub>rr</sub>			-	7.1	14.2	μC
Reverse recovery current	I <sub>RRM</sub>			_	34	-	Α

#### Notes

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$
- b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

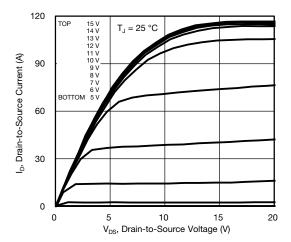


Fig. 1 - Typical Output Characteristics

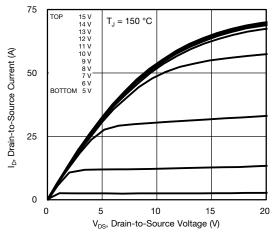


Fig. 2 - Typical Output Characteristics

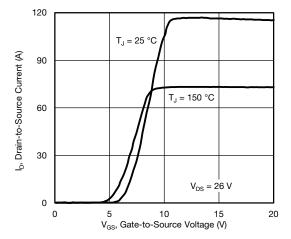


Fig. 3 - Typical Transfer Characteristics

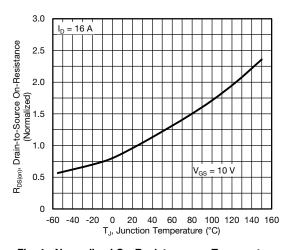


Fig. 4 - Normalized On-Resistance vs. Temperature

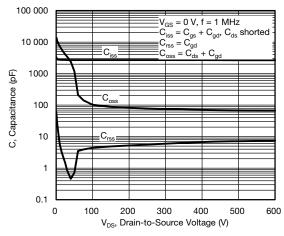


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

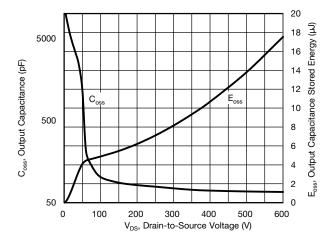


Fig. 6 - Coss and Eoss vs. VDS



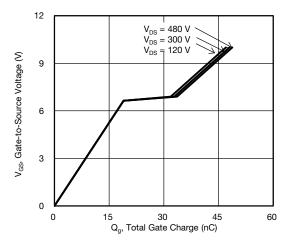


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

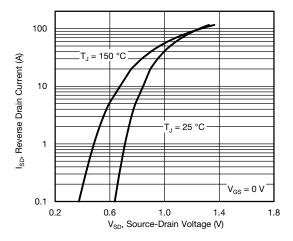


Fig. 8 - Typical Source-Drain Diode Forward Voltage

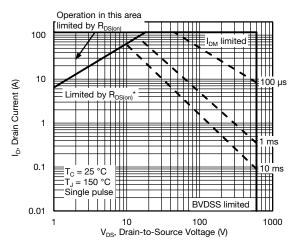


Fig. 9 - Maximum Safe Operating Area

#### Note

a. V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

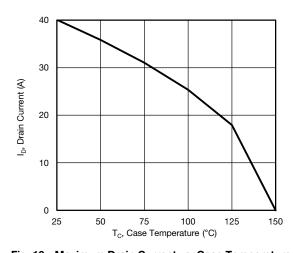


Fig. 10 - Maximum Drain Current vs. Case Temperature

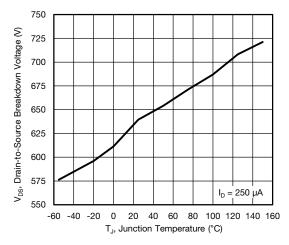


Fig. 11 - Temperature vs. Drain-to-Source Voltage



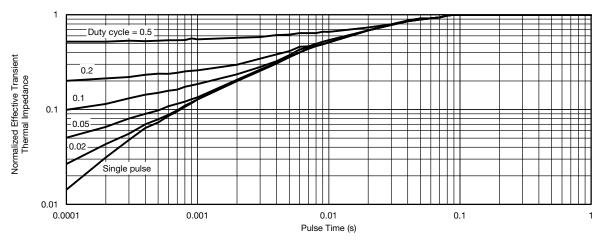


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

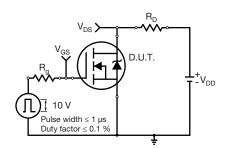


Fig. 13 - Switching Time Test Circuit

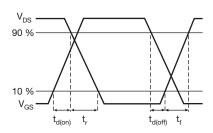


Fig. 14 - Switching Time Waveforms

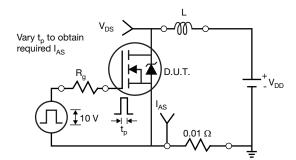


Fig. 15 - Unclamped Inductive Test Circuit

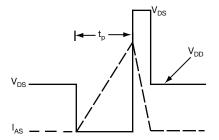


Fig. 16 - Unclamped Inductive Waveforms

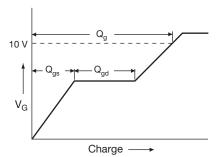


Fig. 17 - Basic Gate Charge Waveform

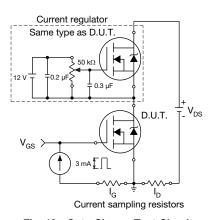
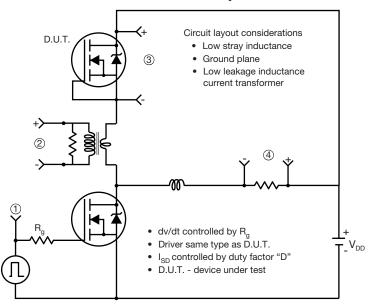


Fig. 18 - Gate Charge Test Circuit



#### Peak Diode Recovery dv/dt Test Circuit



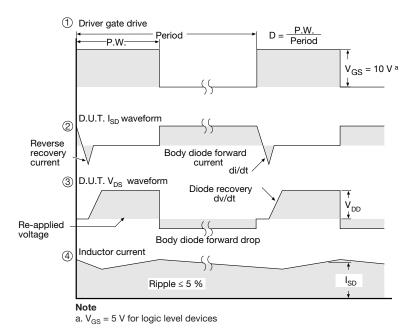


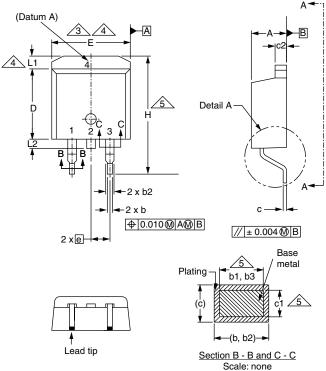
Fig. 19 - For N-Channel

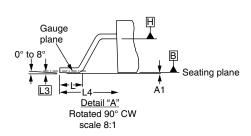
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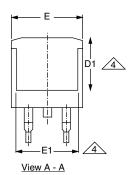


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## **TO-263AB (HIGH VOLTAGE)**







				Scale:
	MILLIN	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

9.65

0.330

0.380

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	i
е	2.54 BSC		0.100 BSC	
Н	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	ı	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

8.38 ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

D

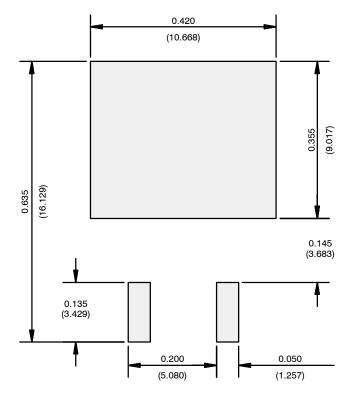
- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

Document Number: 91364 www.vishay.com Revision: 15-Sep-08





## RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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