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## FDMS10C4D2N

### N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 124 A, 4.2 mΩ

#### Features

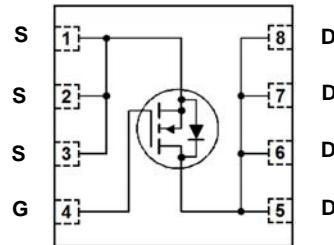
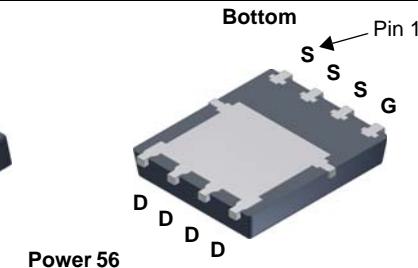
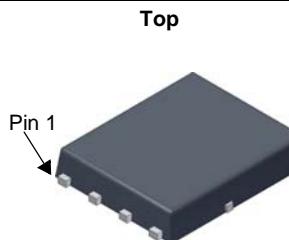
- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 4.2 mΩ at  $V_{GS} = 10$  V,  $I_D = 44$  A
- Max  $r_{DS(on)}$  = 14 mΩ at  $V_{GS} = 6$  V,  $I_D = 22$  A
- ADD
- 50% lower Qrr than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

#### General Description

This N-Channel MV MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

#### Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated Tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

| Symbol         | Parameter  | Ratings                 | Units |
|----------------|--|-------------------------|-------|
| $V_{DS}$       | Drain to Source Voltage                          | 100                     | V     |
| $V_{GS}$       | Gate to Source Voltage                           | $\pm 20$                | V     |
| $I_D$          | Drain Current -Continuous                        | $T_C = 25$ °C (Note 5)  | A     |
|                | -Continuous                                      | $T_C = 100$ °C (Note 5) |       |
|                | -Continuous                                      | $T_A = 25$ °C (Note 1a) |       |
|                | -Pulsed  | (Note 4)                |       |
| $E_{AS}$       | Single Pulse Avalanche Energy                    | (Note 3)                | mJ    |
| $P_D$          | Power Dissipation                                | $T_C = 25$ °C           | W     |
|                | Power Dissipation                                | $T_A = 25$ °C (Note 1a) |       |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +150             | °C    |

#### Thermal Characteristics

|                 |   |     |                             |
|-----------------|---|-----|-----------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case              | 1.0 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50  | $^{\circ}\text{C}/\text{W}$ |

#### Package Marking and Ordering Information

| Device Marking | Device      | Package  | Reel Size | Tape Width | Quantity   |
|----------------|-------------|----------|-----------|------------|------------|
| FDMS10C4D2N    | FDMS10C4D2N | Power 56 | 13 "      | 12 mm      | 3000 units |

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol                                       | Parameter                                 | Test Conditions  | Min | Typ | Max | Units                      |
|--|---|--|-----|-----|-----|----------------------------|
| <b>Off Characteristics</b>                   |   |  |     |     |     |                            |
| $\text{BV}_{\text{DSS}}$                     | Drain to Source Breakdown Voltage         | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$              | 100 |     |     | V                          |
| $\Delta \text{BV}_{\text{DSS}} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ |     | 60  |     | $\text{mV}/^\circ\text{C}$ |
| $I_{\text{DSS}}$                             | Zero Gate Voltage Drain Current           | $V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$              |     |     | 1   | $\mu\text{A}$              |
| $I_{\text{GSS}}$                             | Gate to Source Leakage Current            | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$          |     |     | 100 | nA                         |

## On Characteristics

|   |  |  |     |     |     |                            |
|---|--|--|-----|-----|-----|----------------------------|
| $V_{GS(\text{th})}$                     | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$                             | 2.0 | 3.1 | 4.0 | V                          |
| $\Delta V_{GS(\text{th})} / \Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$           |     | -9  |     | $\text{mV}/^\circ\text{C}$ |
| $r_{DS(\text{on})}$                     | Static Drain to Source On Resistance                     | $V_{GS} = 10 \text{ V}, I_D = 44 \text{ A}$                          |     | 3.3 | 4.2 | $\text{m}\Omega$           |
|   |  | $V_{GS} = 6 \text{ V}, I_D = 22 \text{ A}$                           |     | 5.3 | 14  |                            |
|   |  | $V_{GS} = 10 \text{ V}, I_D = 44 \text{ A}, T_J = 125^\circ\text{C}$ |     | 5.7 | 9.0 |                            |
| $g_{\text{FS}}$                         | Forward Transconductance                                 | $V_{DS} = 10 \text{ V}, I_D = 44 \text{ A}$                          |     | 116 |     | S                          |

## Dynamic Characteristics

|                  |                              |  |     |      |      |          |
|------------------|------------------------------|--|-----|------|------|----------|
| $C_{\text{iss}}$ | Input Capacitance            | $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ |     | 2945 | 4500 | pF       |
| $C_{\text{oss}}$ | Output Capacitance           |  |     | 1730 | 2600 | pF       |
| $C_{\text{rss}}$ | Reverse Transfer Capacitance |  |     | 20   | 50   | pF       |
| $R_g$            | Gate Resistance              |  | 0.1 | 1.3  | 2.6  | $\Omega$ |

## Switching Characteristics

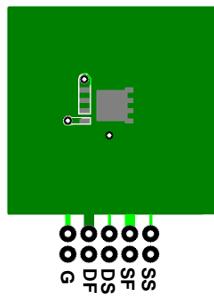
|                     |                               |   |  |    |     |    |
|---------------------|-------------------------------|---|--|----|-----|----|
| $t_{\text{d(on)}}$  | Turn-On Delay Time            | $V_{DD} = 50 \text{ V}, I_D = 44 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$ |  | 17 | 31  | ns |
| $t_r$               | Rise Time                     |   |  | 9  | 18  | ns |
| $t_{\text{d(off)}}$ | Turn-Off Delay Time           |   |  | 25 | 40  | ns |
| $t_f$               | Fall Time                     |   |  | 6  | 12  | ns |
| $Q_g$               | Total Gate Charge             | $V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}$   |  | 42 | 65  | nC |
| $Q_g$               | Total Gate Charge             |   | $V_{GS} = 0 \text{ V} \text{ to } 6 \text{ V}$ | 27 | 43  | nC |
| $Q_{gs}$            | Gate to Source Charge         |   | $I_D = 44 \text{ A}$                           |    | 13  | nC |
| $Q_{gd}$            | Gate to Drain "Miller" Charge |   |  |    | 9.3 | nC |

## Drain-Source Diode Characteristics

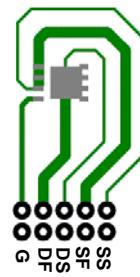
|          |                                       |   |  |     |     |    |
|----------|---------------------------------------|---|--|-----|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)            |  | 0.7 | 1.2 | V  |
|          |                                       | $V_{GS} = 0 \text{ V}, I_S = 44 \text{ A}$ (Note 2)             |  | 0.8 | 1.3 |    |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 20 \text{ A}, \text{di/dt} = 300 \text{ A}/\mu\text{s}$  |  | 32  | 52  | ns |
|          |                                       |   |  | 57  | 92  |    |
| $Q_{rr}$ | Reverse Recovery Charge               | $I_F = 20 \text{ A}, \text{di/dt} = 1000 \text{ A}/\mu\text{s}$ |  | 25  | 40  | ns |
|          |                                       |   |  | 158 | 253 |    |

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 337 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3 \text{ mH}$ ,  $I_{AS} = 15 \text{ A}$ ,  $V_{DD} = 100 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ . 100% test at  $L = 0.1 \text{ mH}$ ,  $I_{AS} = 49 \text{ A}$ .

4. Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

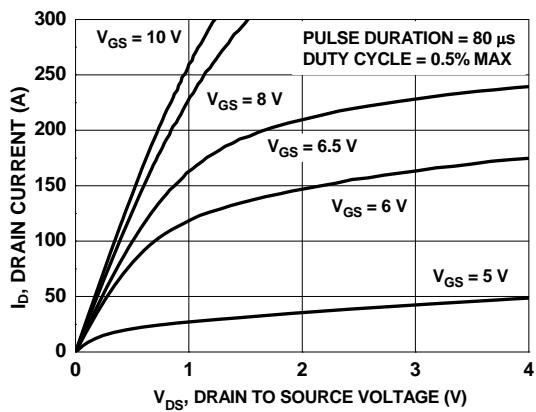


Figure 1. On-Region Characteristics

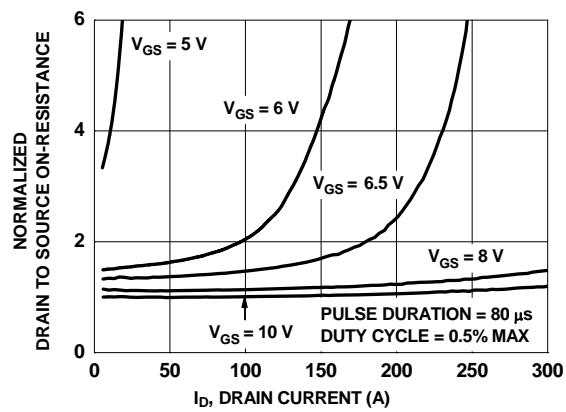


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

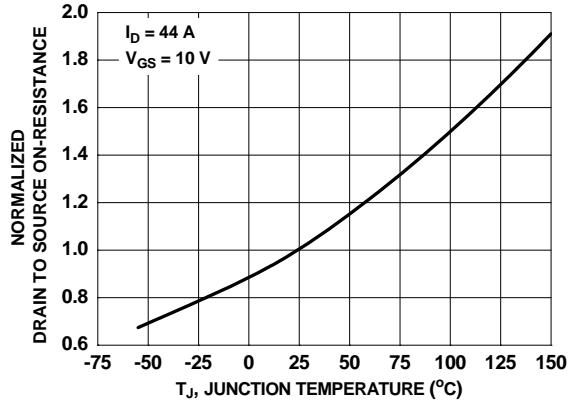


Figure 3. Normalized On-Resistance vs Junction Temperature

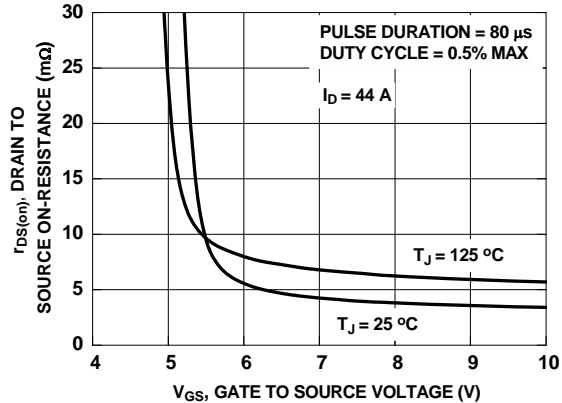


Figure 4. On-Resistance vs Gate to Source Voltage

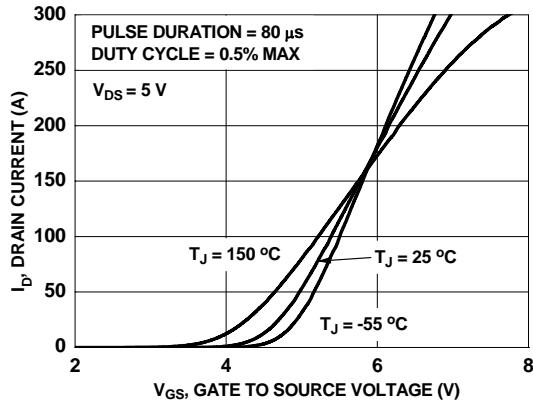


Figure 5. Transfer Characteristics

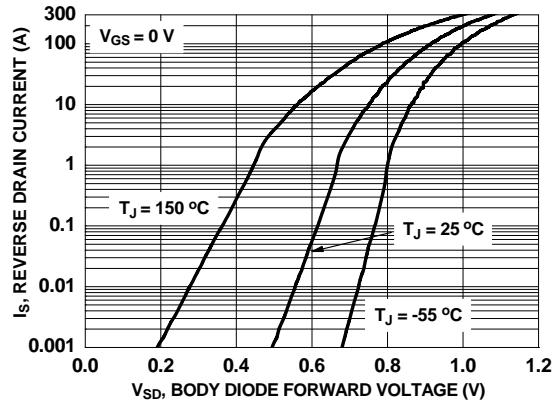


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

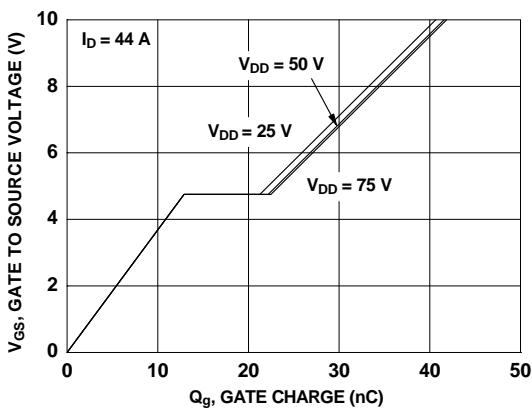


Figure 7. Gate Charge Characteristics

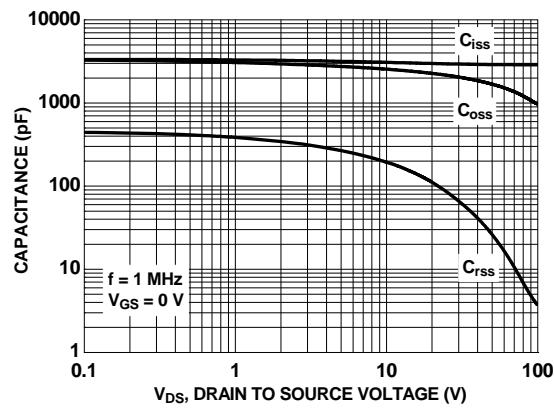


Figure 8. Capacitance vs Drain to Source Voltage

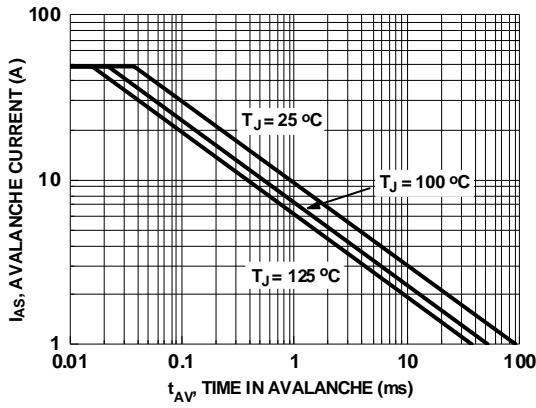


Figure 9. Unclamped Inductive Switching Capability

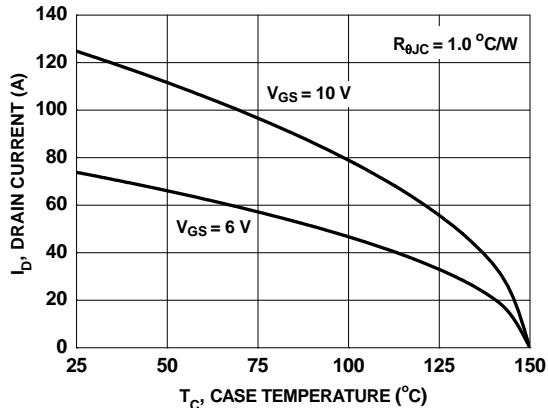


Figure 10. Maximum Continuous Drain Current vs Case Temperature

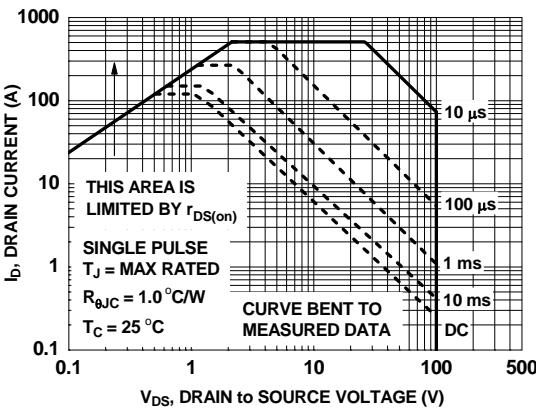


Figure 11. Forward Bias Safe Operating Area

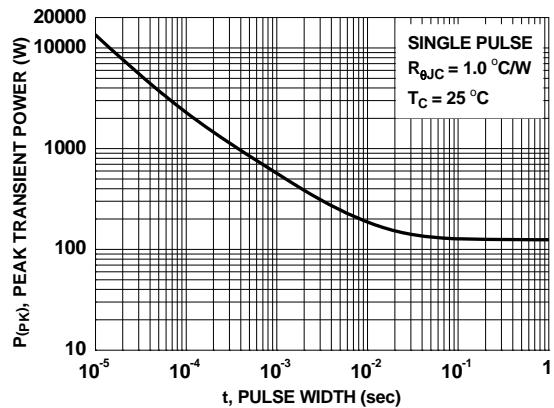


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

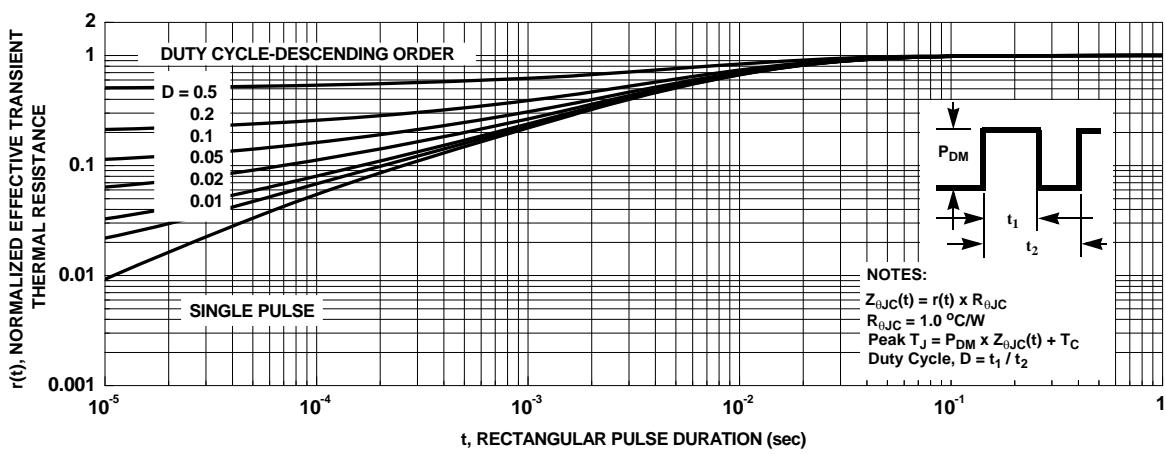
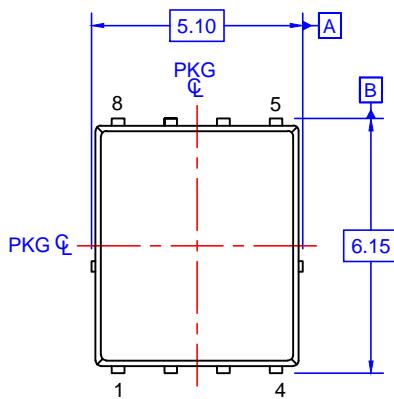
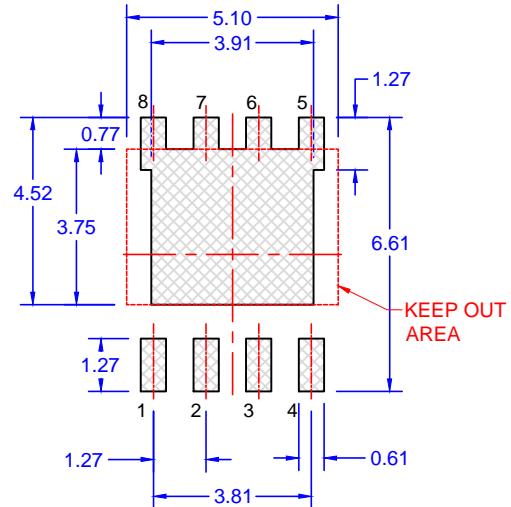


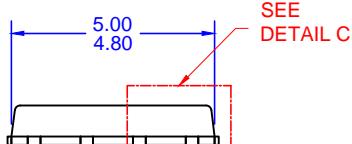
Figure 13. Junction-to-Case Transient Thermal Response Curve



TOP VIEW

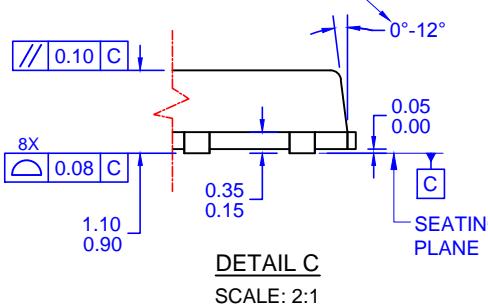


LAND PATTERN  
RECOMMENDATION

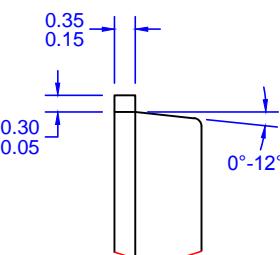


SIDE VIEW

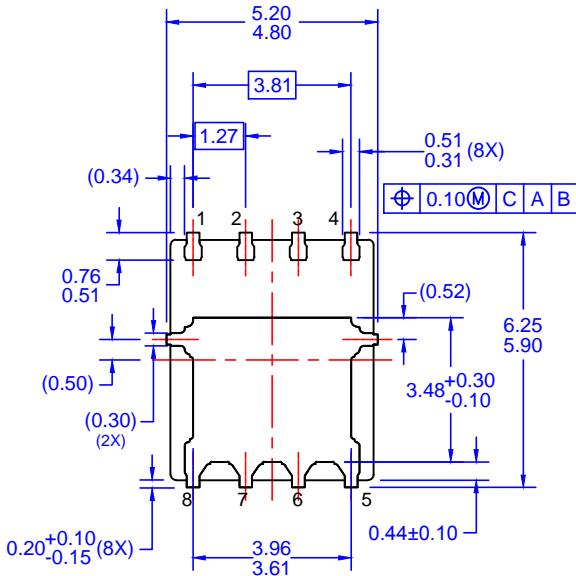
OPTIONAL DRAFT  
ANGLE MAY APPEAR  
ON FOUR SIDES  
OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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