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PRELIMINARY

CYW5459x

Single-Chip Wi-Fi 5 IEEE 802.11 ac 2×2 MAC/Baseband/Radio with RSDB and Bluetooth 5.1 for Commercial/Consumer Applications

CYW5459x is a complete dual-band (2.4 GHz and 5 GHz) Wi-Fi 5 2×2 MIMO MAC/PHY/Radio system-on-Chip. This Wi-Fi 5 single-chip device provides a high level of integration with a dual-stream IEEE 802.11ac MAC/baseband/radio and Bluetooth 5.1. In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates up to 867 Mbps. In addition, all the rates in IEEE 802.11a/b/g/n are supported. Included on-chip Wi-Fi 5 are the 2.4 GHz and 5 GHz transmit power amplifiers and receive low-noise amplifiers. The WLAN operation supports 2x2 MIMO operations as well as two fully simultaneous SISO channels; one in 2.4 GHz and the other in 5 GHz enabling dual-band real simultaneous dual-band (RSDB) operation.

For the WLAN section, the device interfaces to a host SoC processor through a PCIe v3.0-compliant interface running at Gen1 speed, and an SDIO v3.0 interface that can operate in 4b or 1b modes. For the Bluetooth section, Host interface is through a high-speed 4-wire UART interface and PCM interface for audio.

In addition, the CYW5459x implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms that ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. Coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a Commercial/Consumer systems is achieved.

CYW5459x enables fast data stream with minimized latency. It is ideal for high definition video streaming and good quality of audio streaming applications, such as smart speakers, gaming, VR, smart TV, multi-room speakers, and industrial applications like industrial gateways and edge computing.

Features

IEEE 802.11X Key Features

- IEEE 802.11ac Wave-2 compliant.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Supports IEEE 802.11ac/n beamforming.
- Supports RSDB.
- On-chip power amplifiers and low-noise amplifiers for both bands. Also supports external LNAs.
- Supports three antennas with one dedicated to Bluetooth and two to WLAN. Also, shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Supports multipoint external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE and GPS.
- PCIe mode complies with PCI Express base specification revision 3.0 for ×1 lane and power management running at Gen1 speed.
- Supports standard SDIO v3.0 host interface. Backward compatible with SDIO v2.0 host interface.
- Security:
  - WPA, WAPI STA, WPA2, and WPA3 (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Integrated Arm® Cortex® -R4 processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wakeup the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 896 KB SRAM and 896 KB ROM.

Bluetooth Key Features

- Supports Bluetooth 5.1 optional features:
  - Angel or Arrival (AoA)
  - Angel of Departure (AoD)
  - GATT Cache
  - LE power control
- Supports all Bluetooth 5.0 optional features including LE-2Mbps, LE-Long Range, LE-Advertising extensions.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM for audio data.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.
- Supports Serial flash interfaces.

General Features

- Supports battery range from 3.0 V to 4.8 V supplies with internal regulator.
- Programmable dynamic power management.
- Supports 1410 bytes of user-accessible OTP, of which 256 bytes are allocated for Bluetooth and 1150 bytes are allocated for WLAN for storing board parameters.
- GPIOs: 20
- 194-ball WLBGA package (5.16mm x 7.7mm, 0.4mm pitch):

Figure 1. CYW5459x Functional Block Diagram—Two Antenna System

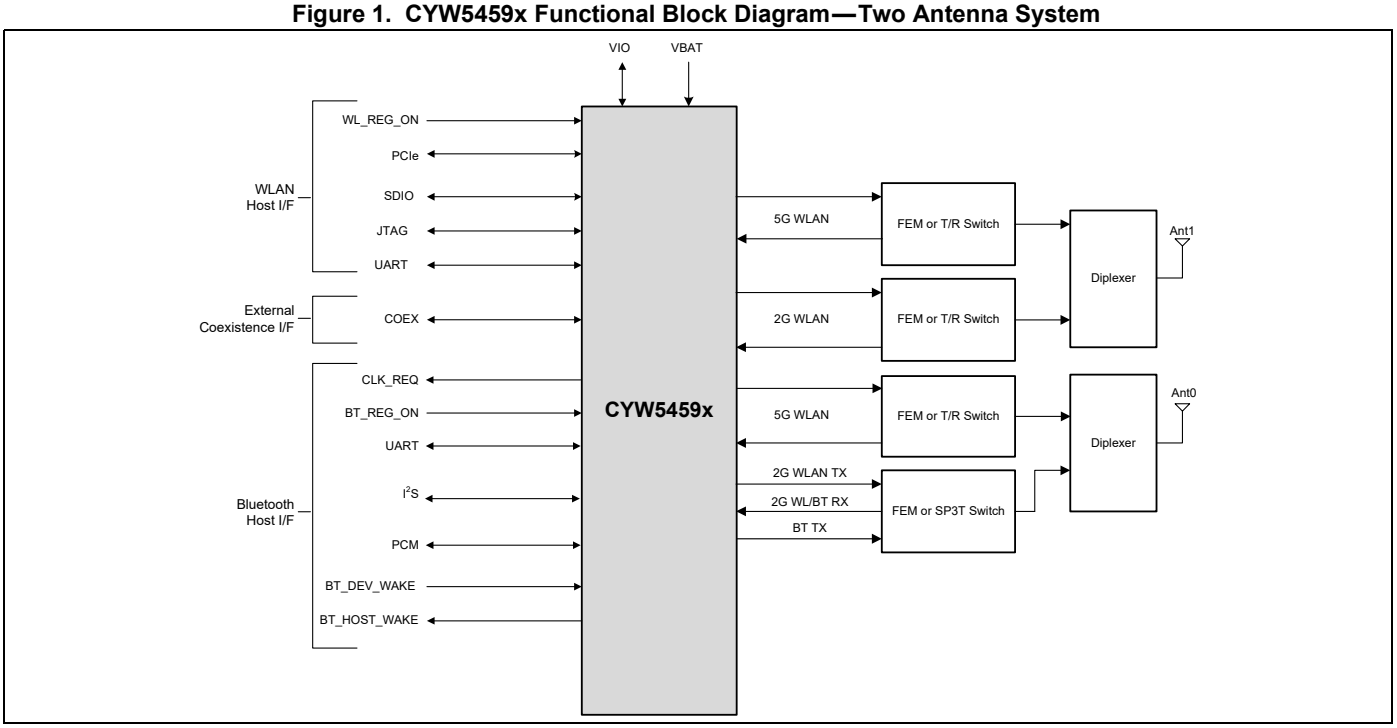
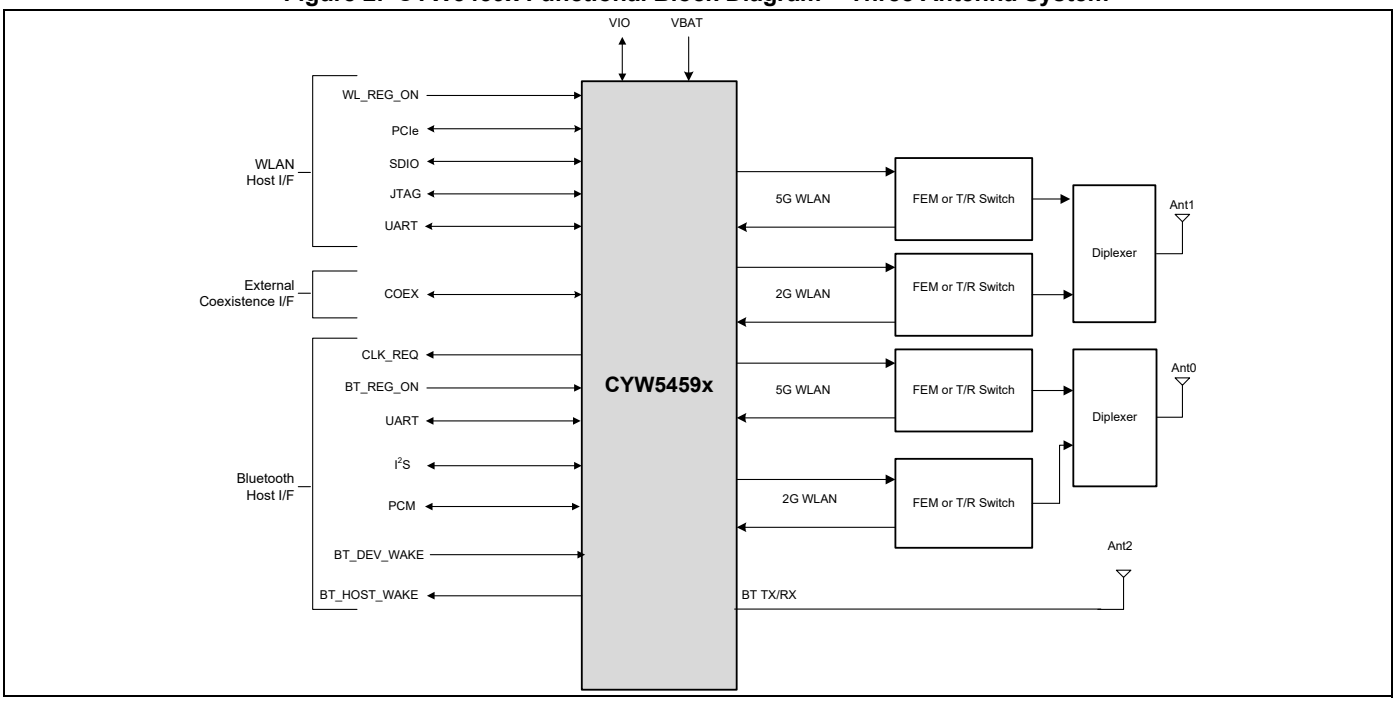


Figure 2. CYW5459x Functional Block Diagram—Three Antenna System



Contents

1. Overview

1.1 Overview

CYW5459x single-chip device provides the highest level of integration for Commercial/Consumer applications, with integrated IEEE 802.11 a/b/g/n/ac MAC/baseband/radio (dual-core 2×2 MIMO), Bluetooth 5.1+ Bluetooth LE with enhanced data rate (EDR). It provides a small form-factor solution with minimal external components to drive down cost and allows for platform design flexibility in size, form, and function.

Table 1. Device Options and Features

Feature	WLBGA
Package ball count	194 balls
PCIe	Yes
SDIO	Yes
UART	Yes
I^2S	Yes
GPIO	20

Figure 3 on page 7 and Figure 4 on page 8 show the interconnect of all the major physical blocks in the CYW5459x and their associated external interfaces for two-antenna and three-antenna systems, respectively.

The interfaces are described in greater detail in the sections following the interconnect diagrams.

Figure 3. CYW5459x Block Diagram for a Two-Antenna System

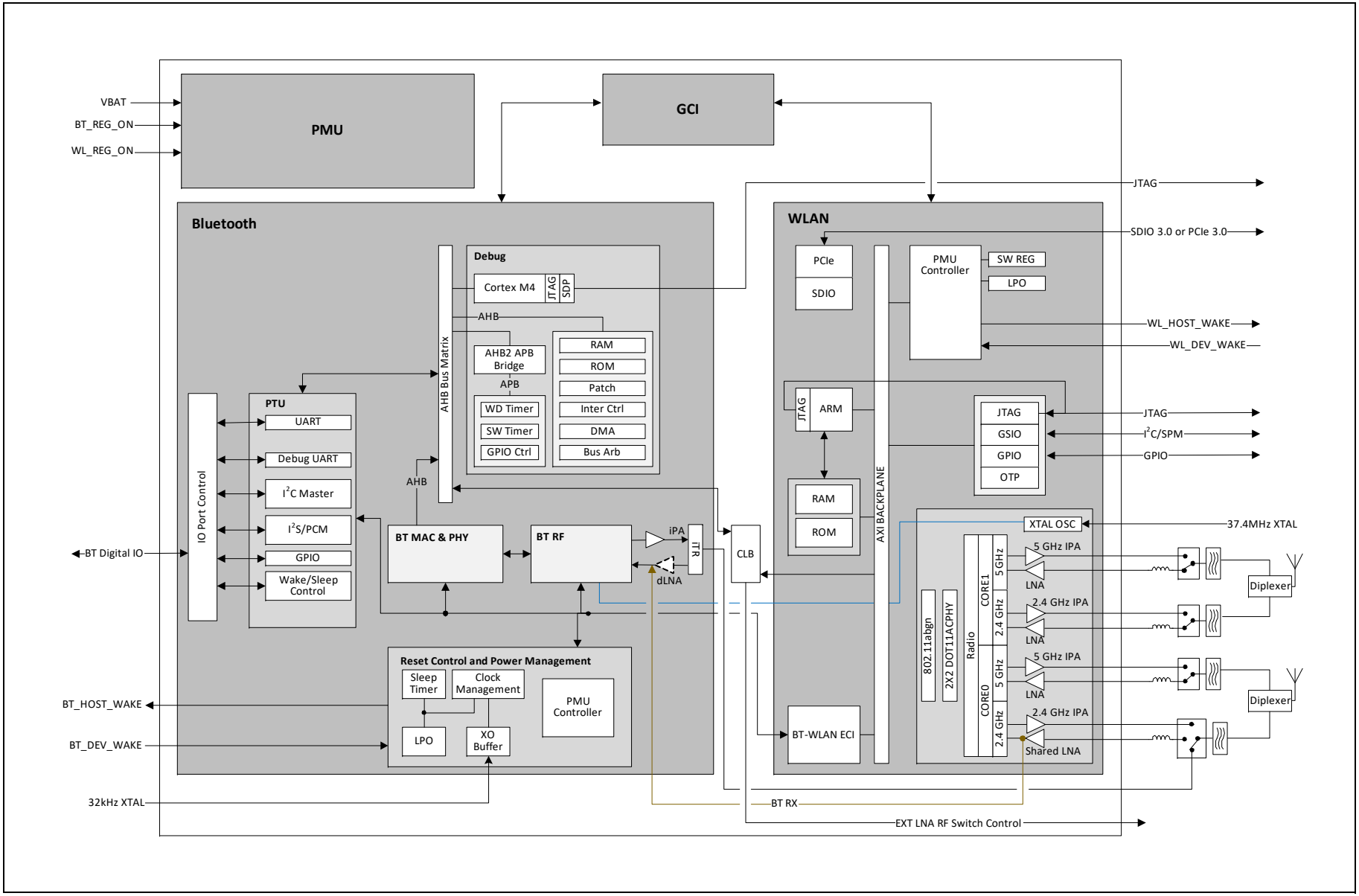
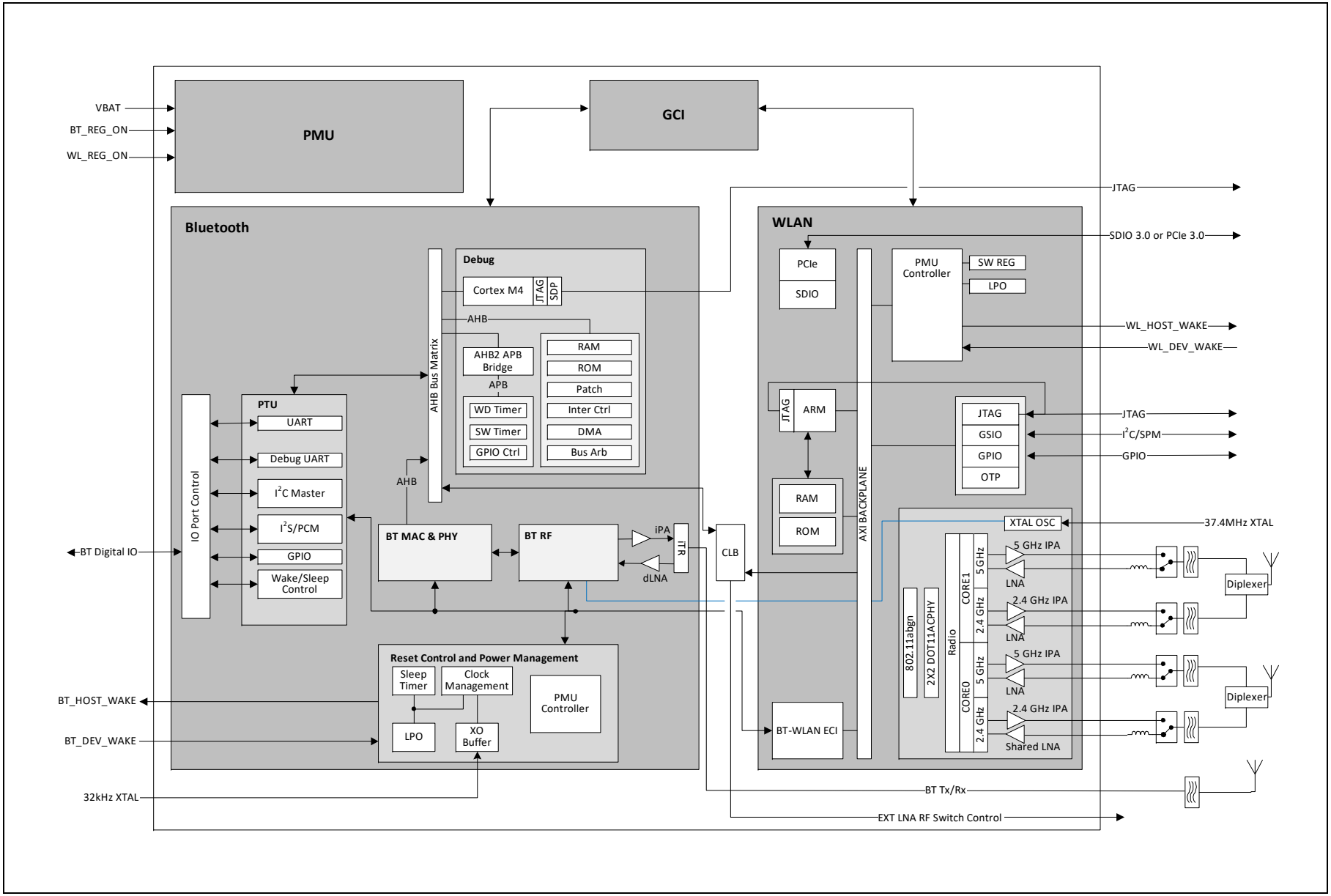


Figure 4. CYW5459x Block Diagram for a Three-Antenna System



1.2 Standards Compliance

The CYW5459x supports the following standards:

- Bluetooth 2.1 + EDR, 3.0, 4.2, 5.1
- IEEE 802.11ac mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11a/b/g/n/ac
- IEEE 802.11d/h
- IEEE 802.11i
- Security:
  - WEP, WPA/WPA2/WPA3 personal, WMM, WMM-PS (U-APSD), WMM-SA, AES (hardware accelerator), TKIP (hardware accelerator), and CKIP (software support)

The CYW5459x will support the following future drafts/standards:

- IEEE 802.11r (fast roaming between APs)
- IEEE 802.11w (secure management frames)
- IEEE 802.11 extensions:
  - IEEE 802.11e QoS enhancements (In accordance with the WMM specification, QoS is already supported.)
  - IEEE 802.11h 5 GHz extensions
  - IEEE 802.11i MAC enhancements

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW5459x. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT (3.0 V to 4.8 V DC max) and VIO supply (1.8 V to 3.3 V) can be used, with all additional voltages being provided by the regulators in the CYW5459x.

Three control signals, BT_REG_ON, WL_REG_ON, and WPT_REG_ON (that is, WPT_1P8), are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted and the wireless supplies (that is, WPT_1P8/WPT_3P3) are not available. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

The CYW5459x allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, MEMLPLDO and LPLDO (which is a low-power linear regulator supplied by the system VIO supply) provide the CYW5459x with all the voltages it requires, further reducing leakage currents.

2.2 CYW5459x PMU Features

- VBAT to 1.35 Vout (600 mA maximum) core-buck (CBUCK) switching regulator
- VBAT to 3.3 Vout (650 mA maximum) PALDO3P3
- VBAT to 3.3 Vout (200 mA maximum) LDO3P3
- VBAT to 2.5 V out (70 mA maximum) BTLDO2P5
- 1.35 V to 1.2 Vout (150 mA maximum) LNLDO
- 1.35 V to 1.2 Vout (420 mA maximum) CLDO with bypass mode for Deep Sleep
- 1.35 V to 1.2 Vout (100 mA maximum) HLDO
- VDDIO to 0.9 Vout (10 mA maximum) MEMLPLDO
- VDDIO to 1.1 Vout (3 mA maximum) LPLDO
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wakeup timing from extremely low-power consumption mode

Figure 5 and Figure 6 on page 12 illustrate the typical power topology for the CYW5459x. The shaded areas are external to the CYW5459x.

Figure 5. Typical Power Topology (1.2 V)

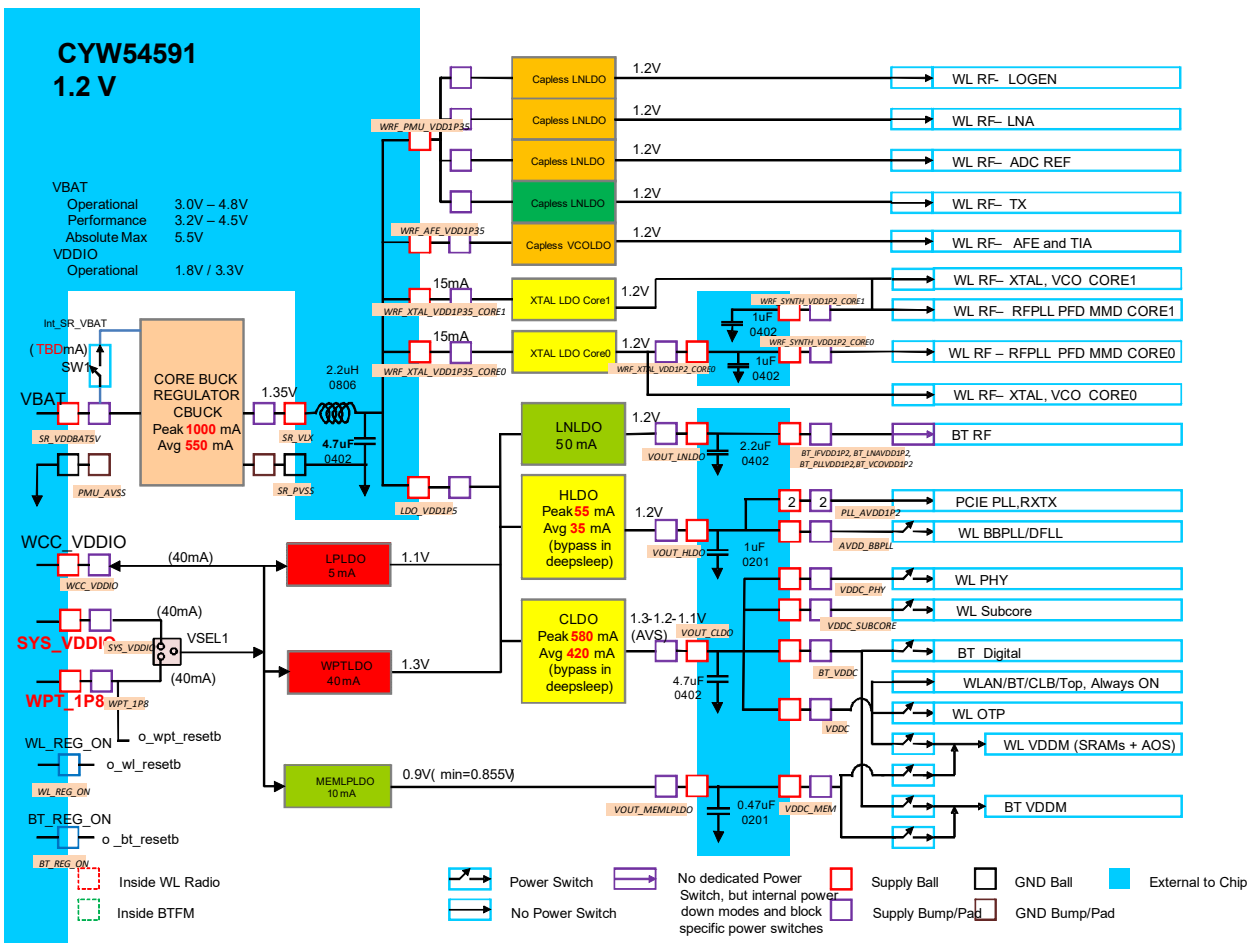
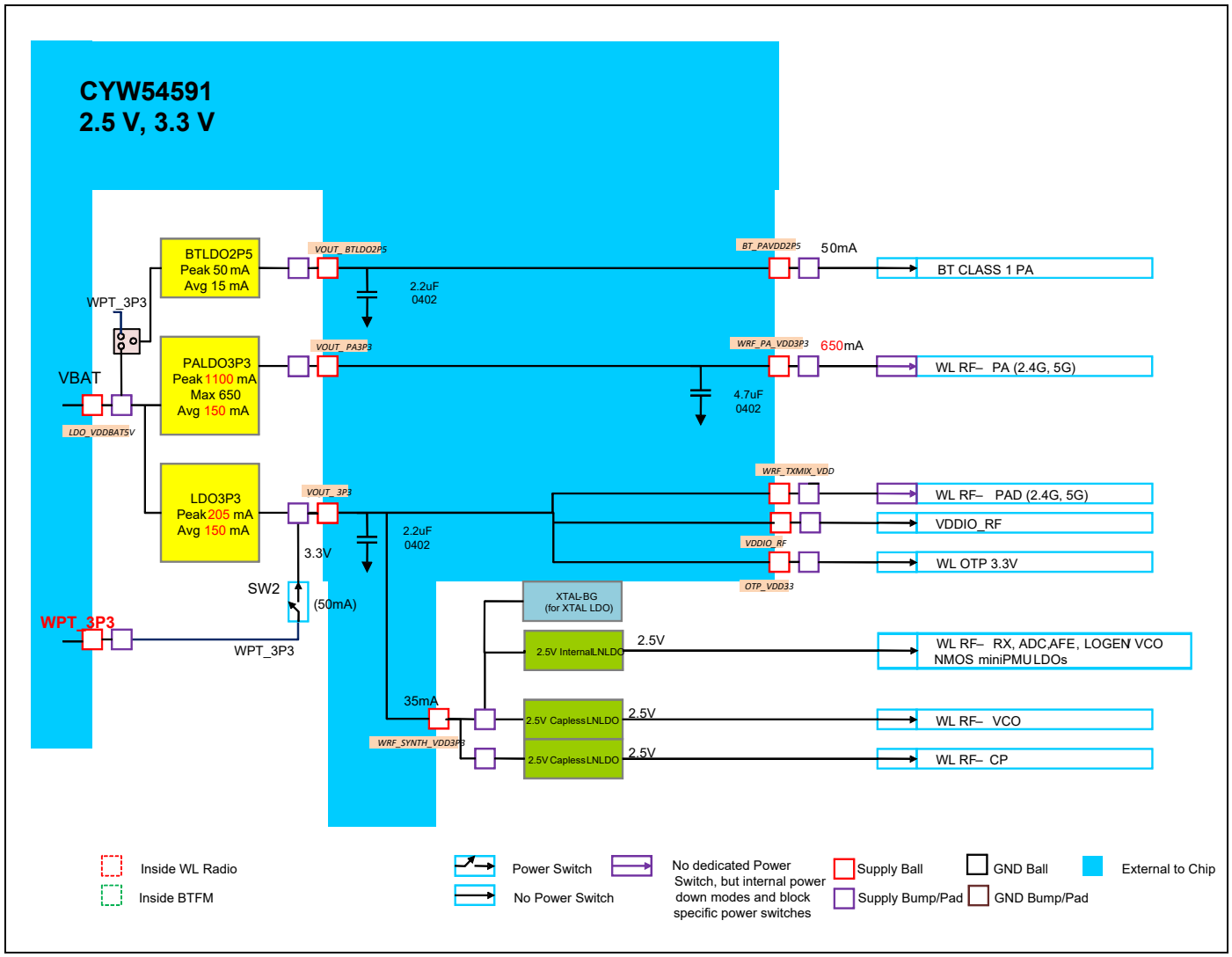


Figure 6. Typical Power Topology (2.5 V and 3.3 V)



2.3 WLAN Power Management

The CYW5459x has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW5459x integrated RAM is a high V_t memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW5459x includes an advanced WLAN PMU sequencer. The PMU sequencer provides significant power savings by putting the CYW5459x into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW5459x WLAN power states are described as follows:

- Active mode—All WLAN blocks in the CYW5459x are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Deep Sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wakeup the chip and transition to Active mode. Logic states in the digital core are saved and preserved into a retention memory in the always ON domain before the digital core is powered off. Upon a wakeup event triggered by the PMU timers, an external interrupt or a host resume, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization. In Deep Sleep mode, the primary source of power consumption is leakage current.
- Power-down mode—The CYW5459x is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW5459x provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW5459x is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW5459x to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the CYW5459x, all outputs are in tristate, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW5459x to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW5459x is powered on from this state, it is the same as a normal power up and the device does not retain any information about its state from before it was powered down.

2.6 Power-up/Power-down/Reset Circuits

The CYW5459x has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 19. “Power-Up Sequence and Timing,” on page 110.

Table 2. Power-up/Power-down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW5459x regulators. When this pin is HIGH, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both LOW, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW5459x regulators. If BT_REG_ON and WL_REG_ON are LOW, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

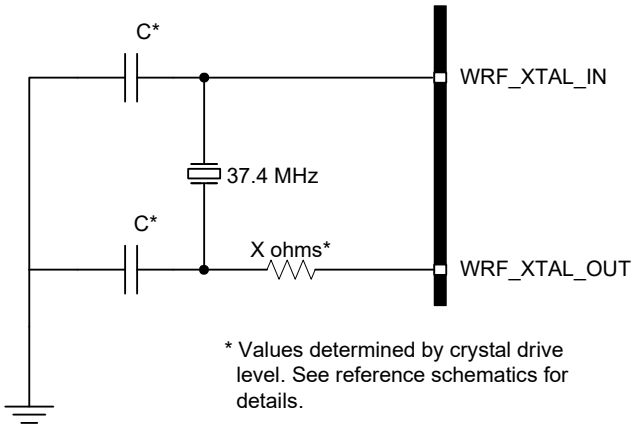
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. External frequency, an alternative reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW5459x can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 7. Refer to the reference schematics for the latest configuration.

Figure 7. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW5459x generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are also listed in Table 3.

Note Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

Table 3. Crystal Oscillator—Requirements and Performance

Parameter	Conditions/Notes	Crystal[1]			
		Min.	Typ.	Max.	Unit
Frequency	2.4G and 5G bands: IEEE 802.11ac operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[2]	Without trimming	–20.0	–	20.0	ppm
Crystal load capacitance	–	–	12.0	–	pF
Equivalent Series Resistance (ESR)	–	–	–	60.0	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	µW
Input impedance (WRF_XTAL_XOP_CORE0)	Resistive	–	–	–	kΩ
	Capacitive	–	–	7.5	pF

Notes
1. Use WRF_XTAL_XOP_CORE0 and WRF_XTAL_XON_CORE0.
2. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

3.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be provided. The recommended default frequency is 37.4 MHz, and it must meet the requirements listed in Table 4.

If used, the external clock should be connected to the WRF_XTAL_XOP_CORE0 pin through an external 1000 pF coupling capacitor, as shown in Figure 8. The internal clock buffer connected to this pin will be turned OFF when the CYW5459x goes into sleep mode.

When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P5 pin.

Figure 8. Recommended Circuit to Use with an External Reference Clock

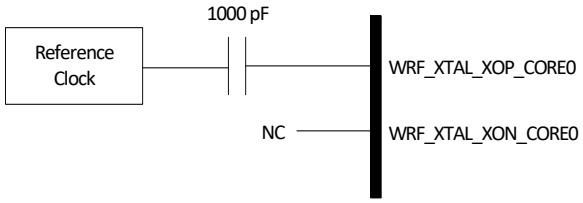


Table 4. External Clock—Requirements and Performance

Parameter	Conditions/Notes	External Frequency Reference			Unit
		Min	Typ	Max	
Frequency	2.4G and 5G bands: IEEE 802.11ac operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[3]	Without trimming	–20.0	–	20	ppm
Input impedance (WRF_XTAL_XOP_CORE0)	Resistive	30.0	100	–	kΩ
	Capacitive	–	–	7.5	pF
WRF_XTAL_XOP_CORE0 Input low level	DC-coupled digital signal	0	–	0.2	V
WRF_XTAL_XOP_CORE0 Input high level	DC-coupled digital signal	1.0	–	1.26	V
WRF_XTAL_XOP_CORE0 input voltage (see Figure 8)	AC-coupled analog signal	400	–	1200	m V_{p-p}
Duty cycle	37.4 MHz clock	40.0	50.0	60.0	%
Phase Noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–136	dBc/Hz
Phase Noise [4] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–144	dBc/Hz
Phase Noise [4] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–141	dBc/Hz
Phase Noise[4] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–149	dBc/Hz
Phase Noise[4] (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–148	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–157	dBc/Hz

Notes
3. It is the responsibility of the equipment designer to select oscillator components that comply with these Specifications.
4. Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 External 32.768 kHz Low-Power Oscillator

The CYW5459x requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in Table 5 must be used.

Table 5. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance [5]	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	ppm

Note
5. When power is applied or switched off.

4. Bluetooth Subsystem Overview

The Cypress CYW5459x is a Bluetooth 5.1 + EDR-compliant, baseband processor and 2.4 GHz transceiver with an integrated dual-band radio. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth solution.

The CYW5459x is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard HCI via a High-speed UART and PCM for audio. The CYW5459x incorporates all Bluetooth 5.1 features including Secure Simple Pairing (SSP), Sniff Subrating (SSR), and Encryption Pause and Resume.

The CYW5459x Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent temperature conditions and tightest integration requirements of embedded industrial and Commercial/Consumer applications. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

4.1 Bluetooth Features

- Bluetooth 5.1 features
  - GATT Caching
  - Angle of Arrival (AoA) and Angle of Departure (AoD)
  - Advertising Channel Index Randomization
  - Selective parts of Minor Feature Enhancements batch1
    - Sleep clock accuracy update mechanism
    - ADI field in scan response data
    - Interaction between QoS and Flow Specification
    - Host channel classification for secondary advertising
    - Allow the SID to appear in scan response reports
- Bluetooth 5.0 features
  - LE 2 Mbits/s
  - LE Long Range, S2/S8 coding
  - LE Higher Output Power (Class 1)
  - LE Advertising Extensions
  - LE Channel Selection Algorithm #2
  - LE High Duty Cycle Non-Connectable Advertising
  - Slot Availability Mask (SAM)
- Bluetooth 4.2 features
  - LE Data Packet Length Extension
  - LE Secure Connections
  - Link Layer privacy
  - Link Layer Extended Scanner Filter policies
- Bluetooth 4.1 features
  - BR/EDR secure connections
  - eSCO reserved slots clarification
  - Train nudging
  - Generalized interlaced scan
  - Connectionless Slave broadcast
  - Unencrypted unicast connectionless data support
  - Low duty cycle directed advertising
  - 32-bit UUID support in LE
  - LE dual mode topology
  - Piconet clock adjustment
  - LE L2CAP connection oriented channel support
  - LE privacy v1.1
  - LE Link Layer topology
  - LE ping
  - Fast advertising interval.
- HCI UART baud rates up to 4 Mbits/s supporting maximum Bluetooth data rates

- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Scatternet operation with up to four active piconets with background scan and support for scatter mode.
- Proprietary narrowband and wideband packet loss concealment
- Proprietary channel quality driven data rate and packet type selection for BR/EDR
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software controlled regulator shutdown
  - HCI UART supports out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management on page 23).
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

4.2 Bluetooth Radio

The CYW5459x has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

4.2.1 Transmit

The CYW5459x features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW5459x to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Receiver Signal Strength Indication (RSSI)

The radio portion of the CYW5459x provides a RSSI signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.7 Local Oscillator (LO) Generation

LO generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW5459x uses an internal RF and IF loop filter.

4.2.8 Calibration

The CYW5459x radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth baseband core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 5.1+ Features

The BBC supports all Bluetooth 5.x features, with the following benefits:

- Support for 5.1 features.
- Dual-mode Bluetooth low energy (BR/EDR and Bluetooth LE operation).
- LE 2M PHY: gives 2Mbits/s link gives higher throughput leading to shorter air time for the same data transfers.
- LE Long Range: coded LE1M PHY giving 125 or 500kb/s, useful for low data rate links needing longer ranges.
- LE Higher Output Power: Class 1 extends range of connectivity by factor of 4.
- LE Advertising Extensions: power and air time efficient mechanism to broadcast data using data channels.
- LE Channel Selection Algorithm #2: improved and adaptive channel hoping algorithm based on channel quality/success statistics.
- LE High Duty Cycle Non-Connectable Advertising: enables sensor applications to transmit data at increased frequency without establishing connections.
- Slot Availability Mask (SAM): enables peer devices to communicate their availability (governed by internal or external conditions) for Tx/Rx leading to improved CoEx and power consumption.
- LE Data Packet Length Extension: increases the Protocol Data Unit size from 27 to 251 bytes.
- Secure Connections: for both BR/EDR and LE physical transports using FIPS approved AES-CMAC and P-256 elliptic curve algorithms.
- Link Layer privacy: Key based Resolvable Private Address generation where the Identity Resolving Key is exchanged between Master and Slave during pairing.
- Link Layer Extended Scanner Filter policies: Saves power in background scan by having the ability filter out policy based private addresses at lower layers of processing.
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision timeout (LSTO): Additional commands added to HCI and link management protocol (LMP) for improved link timeout supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU).

This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth link controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Advertise
  - Scan
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

5.3 Test Mode Support

The CYW5459x fully supports Bluetooth Test mode as described in the Specification of the Bluetooth System v5.1. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test mode, the CYW5459x also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.4 Bluetooth Power Management Unit (PMU)

The Bluetooth PMU provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the CYW5459x are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

5.4.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.4.2 Host Controller Power Management

When running in UART mode, the CYW5459x may be configured so that dedicated signals are used for power management handshaking between the CYW5459x and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation. Table 6 describes the power-control handshake signals used with the UART interface.

Table 6. Power Control Pin Description

Signal	Type	Description
BT_DEV_WAKE	I	Bluetooth device wake up: Signal from the host to the CYW5459x indicating that the host requires attention. ■Asserted: The Bluetooth device must wakeup or remain awake. ■Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH/LOW.
BT_HOST_WAKE	O	Host wake up. Signal from the CYW5459x to the host indicating that the CYW5459x requires attention. ■Asserted: host device must wakeup or remain awake. ■Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH/LOW.
CLK_REQ	O	The CYW5459x asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The CLK_REQ polarity is active-high.

Note
6. Pad function Control Register is set to 0 for these pins. See DC Characteristics on page 68 for more details.

5.4.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW5459x runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW5459x is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW5459x to effectively be OFF while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

During the low-power shut-down state, provided VDDIO remains applied to the CYW5459x, all outputs are in tristate, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the CYW5459x to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW5459x input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW5459x is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.4.4 Wideband Speech (WBS)

The CYW5459x provides support for WBS using on-chip SmartAudio® technology. The CYW5459x can perform subband codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

5.4.5 Packet Loss Concealment (PLC)

PLC improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW5459x uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 9 and Figure 10 show audio waveforms with and without Packet Loss Concealment. Cypress PLC/BEC algorithms also support wideband speech.

Figure 9. CVSD Decoder Output Waveform Without PLC

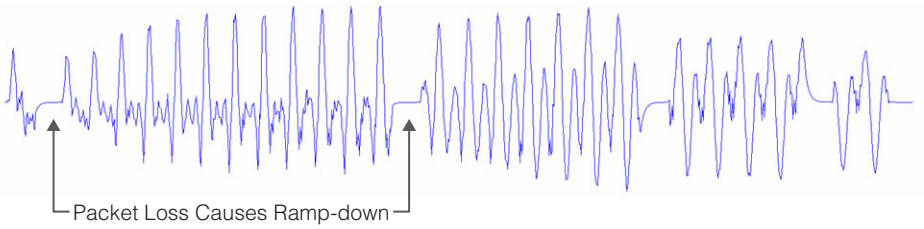
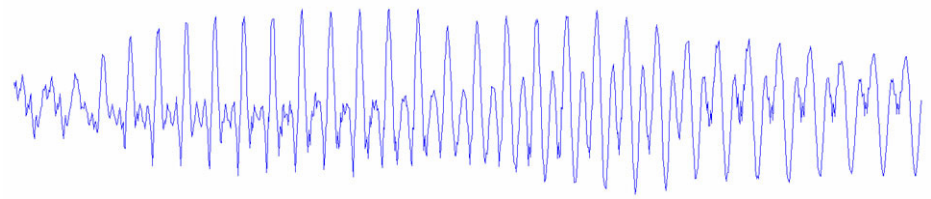


Figure 10. CVSD Decoder Output Waveform After Applying PLC



5.4.6 Audio Rate-Matching Algorithms

The CYW5459x has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth data rates.

5.4.7 Codec Encoding

The CYW5459x can support SBC and mSBC encoding and decoding for wideband speech.

5.4.8 Multiple Simultaneous A2DP Audio Stream

The CYW5459x has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.5 Adaptive Frequency Hopping

The CYW5459x gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.6 Advanced Bluetooth/WLAN Coexistence

The CYW5459x includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as Video-over-WLAN (VoWLAN) + SCO and VoWLAN + High Fidelity Bluetooth Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The CYW5459x radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The CYW5459x integrated solution enables MAC layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW5459x also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

Note For external FEM or SP3T switches, care should be taken to ensure that WLAN TX and Bluetooth RX have a minimum isolation of 20dB.

5.7 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW5459x supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth v2.1 page and inquiry procedures.

6. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the Arm® Cortex®-M4 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the HCI.

The Arm® Cortex®-M4 core is paired with a memory unit that contains 1600 KB of ROM memory for program storage and boot ROM, 320 KB of RAM for data scratch-pad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the CYW5459x through the UART transports.

6.1 RAM, ROM, and Patch Memory

The CYW5459x Bluetooth core has 320 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 1600 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

The CYW5459x has an integrated power-on reset (POR) circuit that resets all circuits to a known power-on state. The Bluetooth POR circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is LOW, then the POR circuit is held in reset.

7. Bluetooth Peripheral Transport Unit

The CYW5459x supports HFP and A2DP codec controllers with optimized I2S and PCM transports for Bluetooth audio.

HFP codec interface controller:

- Supported by PCM and I2S transports and bi-directional operations.
- PCM
  - Sample rates 8k for NBS and 16k for WBS supported.
  - Dual stream use cases can concurrently use NBS and WBS.
  - Sample width is limited to 16-bits.
  - Synchronization clock width of 1 or 3 (short or long).
  - Bit clocks of 128k, 256k, 512k, 1024k and 2024k, the only difference being the number of 16bit slots.
  - HFP samples can be taken from any available slot. Slot 0 is the default slot.
- I2S
  - Supports bit clocks of 256k (NBS) and 512K (WBS).
  - HFP samples can be taken from either left or right. Left is the default.

A2DP codec controller:

- Supported by I2S transport in a single direction, either in or out but not both.
- Two channels, left and right. Mono is not supported.
- Sample rates: 44.1k or 48k.
- Sample width is limited to 16-bits.
- Supports bit clocks of 32 times the sample rate, 1.411200 (44.1k) or 1536000 (48k) and not adjustable

7.1 PCM Interface

The CYW5459x supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on the CYW5459x can connect to linear PCM codec devices in Master/Slave mode. In Master mode, the CYW5459x generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in Slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW5459x.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.1.1 Slot Mapping

The CYW5459x supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from a SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.1.2 Frame Synchronization

The CYW5459x supports both short and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.1.3 Data Formatting

The CYW5459x may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW5459x uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked Most Significant Bit (MSb) first.

7.1.4 Wideband Speech Support

When the host encodes WBS packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in

a 64 Kbps bit rate. The CYW5459x also supports slave transparent mode using a proprietary rate-matching scheme. In SBCcode mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.1.5 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 11. PCM Timing Diagram (Short Frame Sync, Master Mode)

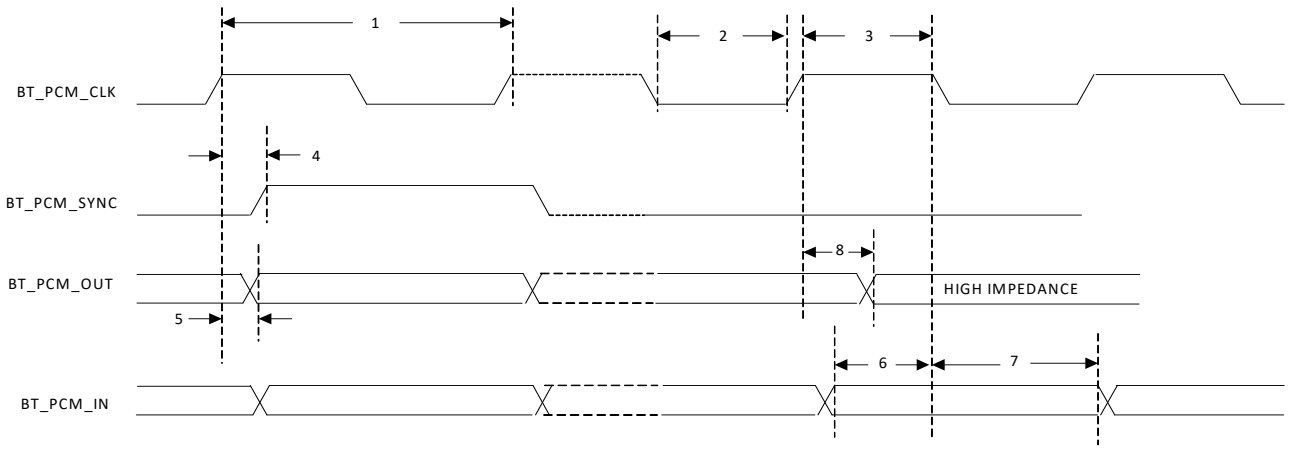


Table 7. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Short Frame Sync, Slave Mode

Figure 12. PCM Timing Diagram (Short Frame Sync, Slave Mode)

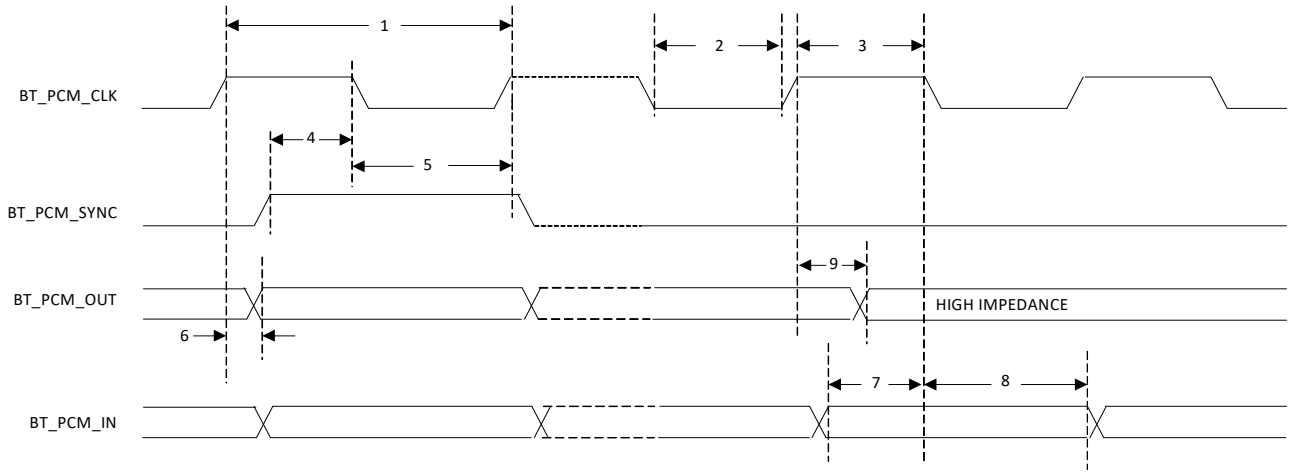


Table 8. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Long Frame Sync, Master Mode

Figure 13. PCM Timing Diagram (Long Frame Sync, Master Mode)

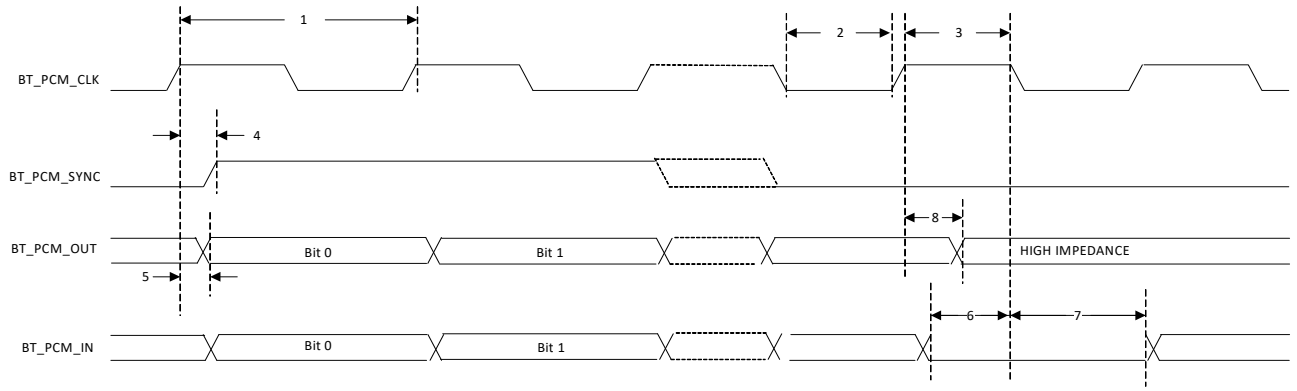


Table 9. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

Long Frame Sync, Slave Mode

Figure 14. PCM Timing Diagram (Long Frame Sync, Slave Mode)

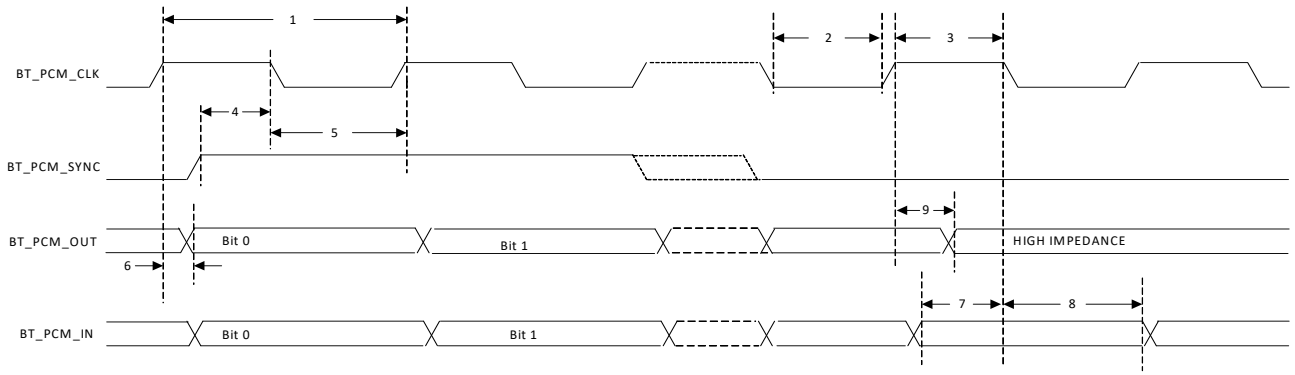


Table 10. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0.	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0.	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance.	0	–	25.0	ns

7.2 UART Interface

The CYW5459x UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“3-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW5459x UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW5459x UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 11. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 15. UART Timing

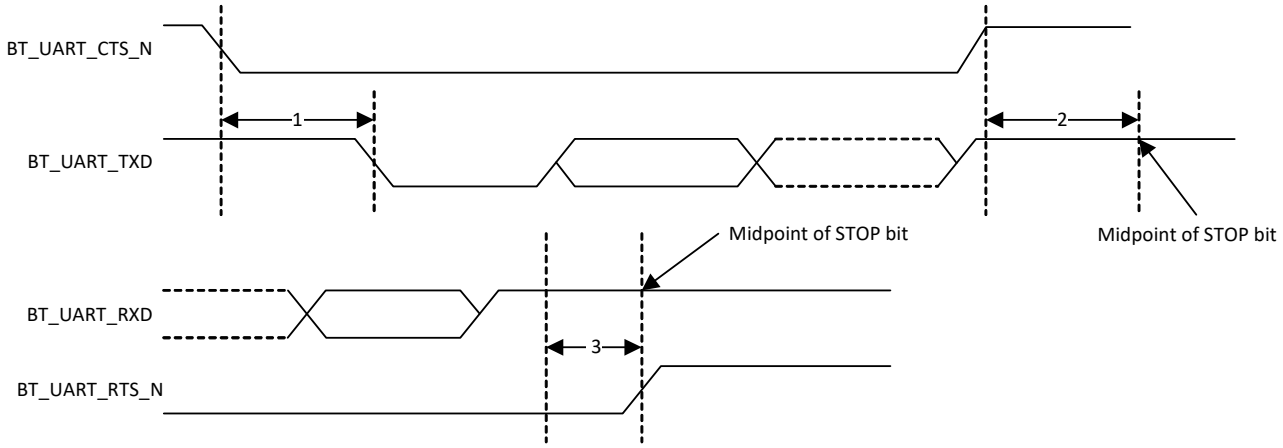


Table 12. UART Timing Specifications

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

7.3 I²S Interface

The CYW5459x supports I²S digital audio port for Bluetooth audio. The I²S signals are:

- I²S clock: BT_I2S_CLK
- I²S Word Select: BT_I2S_WS
- I²S Data Out: BT_I2S_DO
- I²S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in Master mode and inputs in Slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSb of the left-channel data is aligned with the MSb of the I²S bus, in accord with the I²S specification. The MSb of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is LOW, and right-channel data is transmitted when BT_I2S_WS is HIGH. Data bits sent by the CYW5459x are synchronized with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

The clock rate in master mode is either of the following:

48 kHz × 32 bits per frame = 1.536 MHz

48 kHz × 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

7.3.1 I^2S Timing

Note Timing values specified in Table 13 are relative to high and low threshold levels.

Table 13. Timing for I^2S Transmitters and Receivers

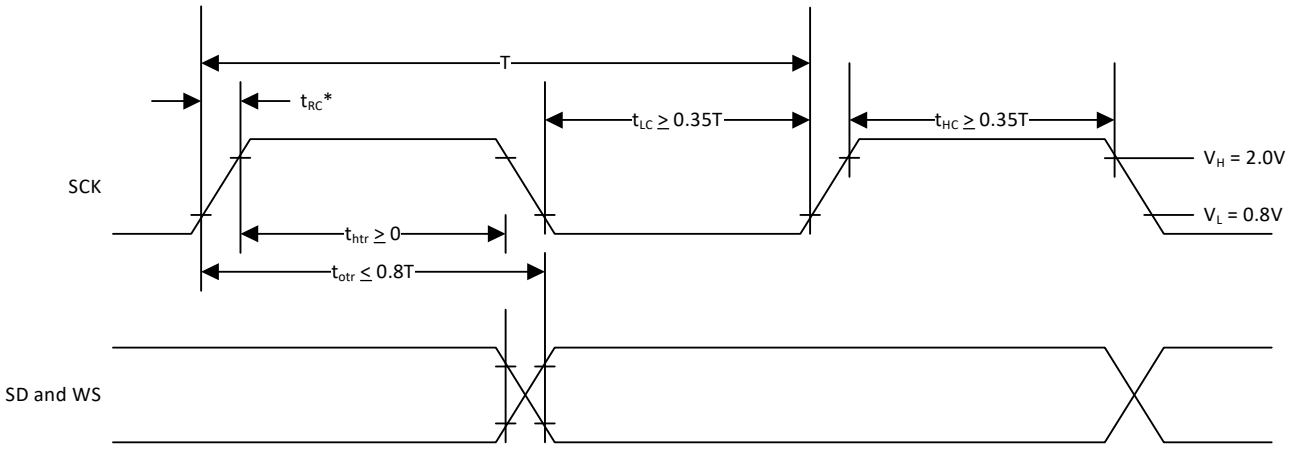
	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	7
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	8
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	8
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	9
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	9
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	10
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	11
Hold time t_{htr}	0	–	–	–	–	–	–	–	10
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	12
Hold time t_{hr}	–	–	–	–	–	0	–	–	12

Notes

7. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
8. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
9. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
10. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
11. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
12. The data setup and hold time must not be less than the specified receiver setup and hold time.

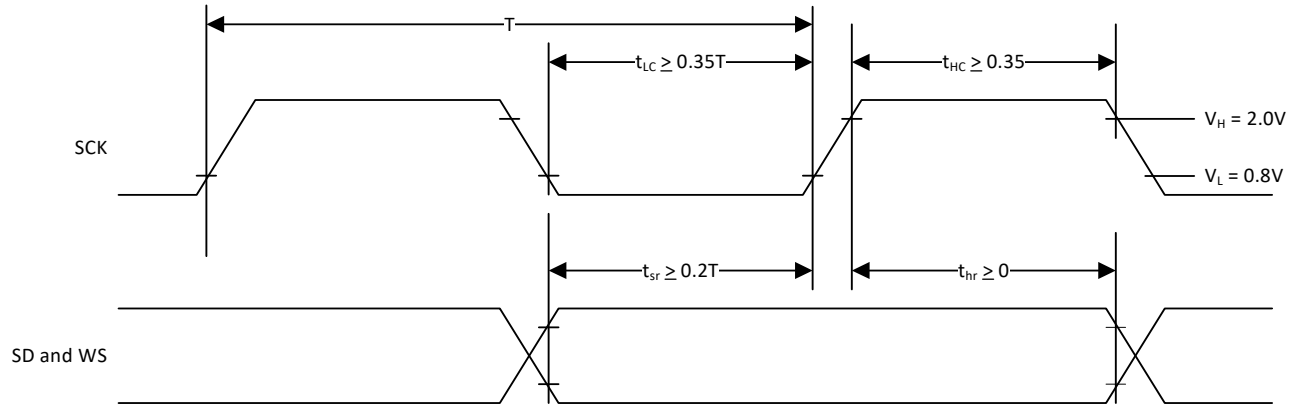
Note The time periods specified in Figure 16 and Figure 17 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 16. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 17. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

8. WLAN Global Functions

8.1 WLAN CPU and Memory Subsystem

The CYW5459x WLAN section includes an integrated Arm® Cortex®-R4 32-bit processor with internal RAM and ROM. The on-chip memory for the CPU includes 896KB SRAM and 896 KB ROM. The Arm® Cortex®-R4 processor implements the Arm v7-R architecture with support for the Thumb-2 instruction set.

Using multiple technologies to reduce cost, the Arm® Cortex® -R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and system buses), integrated sleep modes, and extensive debug features including real-time tracing of program execution.

8.2 OTP Memory

Various hardware configuration parameters may be stored in an internal OTP memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 1150 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

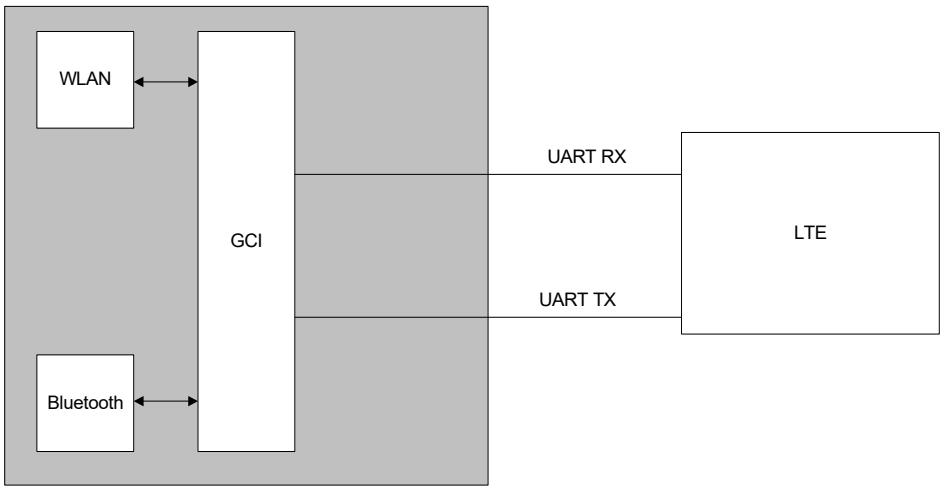
8.3 GPIO Interface

The CYW5459x has 20 GPIO pins in the WLAN section that can be used to connect to various external devices. Upon power-up and reset, these pins are in tristate. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions, see Table 22 on page 61.

8.4 External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as LTE to manage wireless medium sharing for optimal performance. Figure 18 shows the Long Term Evolution (LTE) coexistence interface (including UART). See Table 22 for further details on multiplexed signals, such as the GPIO pins.

Figure 18. Multipoint Global Coexistence Interface



Baud rates are derived from the crystal clock. For rates higher than a crystal_frequency/16, the baud rate is an integer divide of the crystal frequency. Table 14 shows the values for a 37.4 MHz crystal.

Table 14. Baud Rates for a 37.4 MHz Crystal

Division	XTAL	Baud Rate (Mbps)
12	37.4/12	3.116667
13	37.4/13	2.876923
14	37.4/14	2.671429
15	37.4/15	2.493333
16	37.4/16	2.3375

8.5 Debug UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 22 on page 61. Provided primarily for debugging during development, this UART enables the CYW5459x to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.6 FAST UART Interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Refer to Table 22. Provided primarily for control word exchange, this UART enables the chip to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.7 JTAG Interface

The CYW5459x supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs. Refer to Table 22 for JTAG pin assignments.

8.8 SPROM Interface

Various hardware configuration parameters may be stored in an external SPROM instead of the OTP. The SPROM is read by system software after device reset. In addition, depending on the board design, customer-specific parameters may be stored in SPROM.

The four SPROM control signals —SPROM_CS, SPROM_CLK, SPROM_MI, and SPROM_MO are multiplexed on the SDIO interface (see Table 22 for additional details). By default, the SPROM interface supports 4 kbit serial SPROMs.

8.9 Cypress Serial Control (CSC) Interface

A proprietary CSC, (an I^2C-compatible interface) slave interface is available as an alternate function on the GPIO lines. It supports data transfer rates up to 3.4 Mbps in high-speed mode. It can be primarily used to transfer data to a sensor hub in the host system. This interface supports device interrupts and 7-bit and 10-bit addressing to the processor. Based on the device-address matching, a device can be brought out of low-power state using this interface. This interface provides an internal FIFO depth of 32 bytes for both TX and RX with the ability to filter glitches on both clock and data lines.

9. WLAN Host Interfaces

9.1 SDIO v3.0

All three package options of the CYW5459x WLAN section provide support for SDIO v3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1 and 4-bit modes (3.3 V signaling).
- SDR12: SDR up to 25 MHz (1.8 V signaling).
- SDR25: SDR up to 50 MHz (1.8 V signaling).
- SDR50: SDR up to 100 MHz (1.8 V signaling).
- SDR104: SDR up to 208 MHz (1.8 V signaling)
- DDR50: DDR up to 50 MHz (1.8 V signaling).

Note: The CYW5459x is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options. Refer to Table 20 on page 60 WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max. BlockSize/ByteCount = 512B)

9.1.1 SDIO Pins

Table 15. SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 19. Signal Connections to SDIO Host (SD 4-Bit Mode)

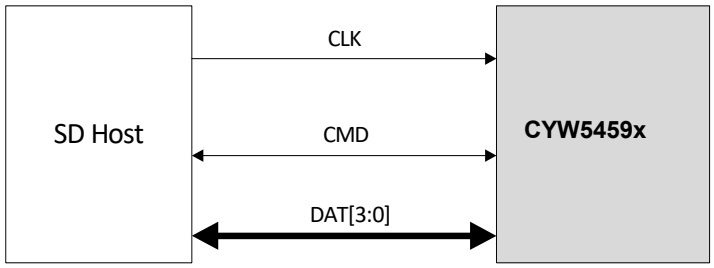
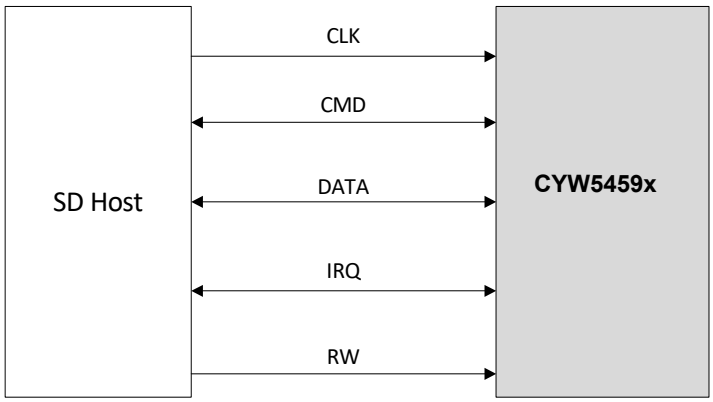


Figure 20. Signal Connections to SDIO Host (SD 1-Bit Mode)



Note: Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

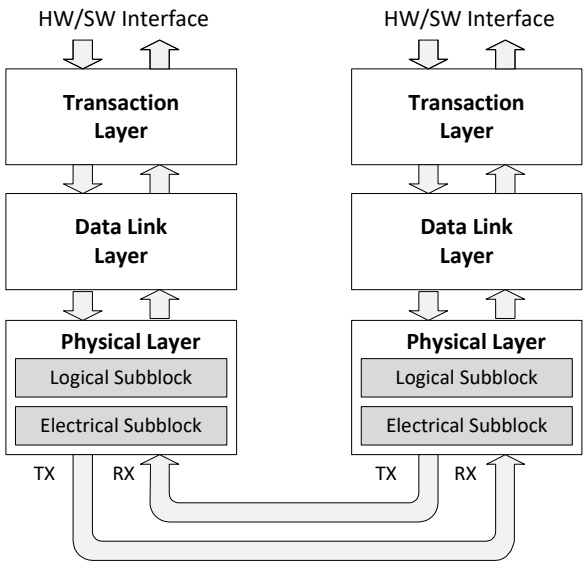
9.2 PCI Express (PCIe) Interface

The PCI Express core on the CYW5459x is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v3.0* running at Gen1 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 21. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW5459x device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 21. PCI Express Layer Model



9.2.1 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW5459x device, delivering new levels of performance and features. The upper layer of the PCIe is the transaction layer. The transaction layer is primarily responsible for assembly and disassembly of transaction layer packets (TLPs). TLP structure contains header, data payload, and end-to-end CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

9.2.2 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

The data link layer packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

9.2.3 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW5459x device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

9.2.4 Logical Subblock

The logical subblock primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

9.2.5 Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

9.2.6 8B/10B Encoder/Decoder

The PCIe core on the CYW5459x uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the 12 special symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. The special symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

9.2.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

9.2.8 Electrical Subblock

The high-speed signals utilize the common mode logic (CML) signaling interface with on-chip termination and deemphasis for best-in-class signal integrity. A deemphasis technique is employed to reduce the effects of intersymbol interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable bit-error rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are deemphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the deemphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

9.2.9 Configuration Space

The PCIe function in the CYW5459x implements the configuration space as defined in the *PCI Express Base Specification v3.0*.

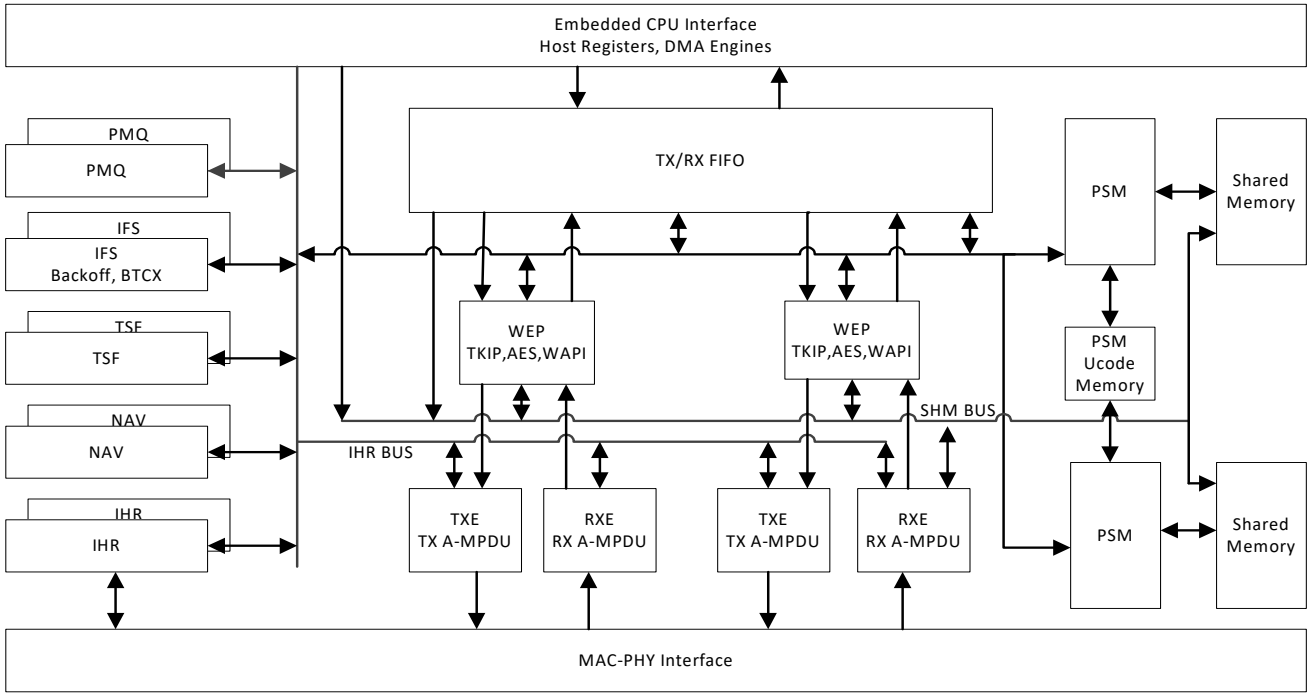
10. Wireless LAN MAC and PHY

10.1 IEEE 802.11ac MAC

The CYW5459x WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 22.

The following sections provide an overview of the important modules in the MAC.

Figure 22. WLAN MAC Architecture



The CYW5459x WLAN MAC supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ac features.
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT).
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Hardware offload engine for IEEE 802.11 to IEEE 802.3 header conversion for receive packets.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality.
- Statistics counters for MIB support.
- RSDB-capable PHY and MAC support for 2 × 2 operation or two independent 1 × 1 operations.

Programmable State Machine (PSM)

The PSM is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch-pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

Wired Equivalent Privacy (WEP)

The WEP engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, Wi-Fi Protected Access (WPA), Temporal Key Integrity Protocol (TKIP), WPA2, Advanced Encryption Standard - Counter Mode with Cipher Block Chaining Message Authentication Code Protocol (AES-CCMP).

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the Message Integrity Check (MIC) on receive frames.

Transmit Engine (TXE)

The TXE constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS Module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

Receive Engine (RXE)

The RXE constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

Inter-frame Spacing (IFS)

The IFS module contains the timers required to determine inter-frame space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The inter-frame spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

Timing Synchronization Function (TSF)

The TSF module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

Network Allocation Vector (NAV)

The NAV timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

10.2 IEEE 802.11ac PHY

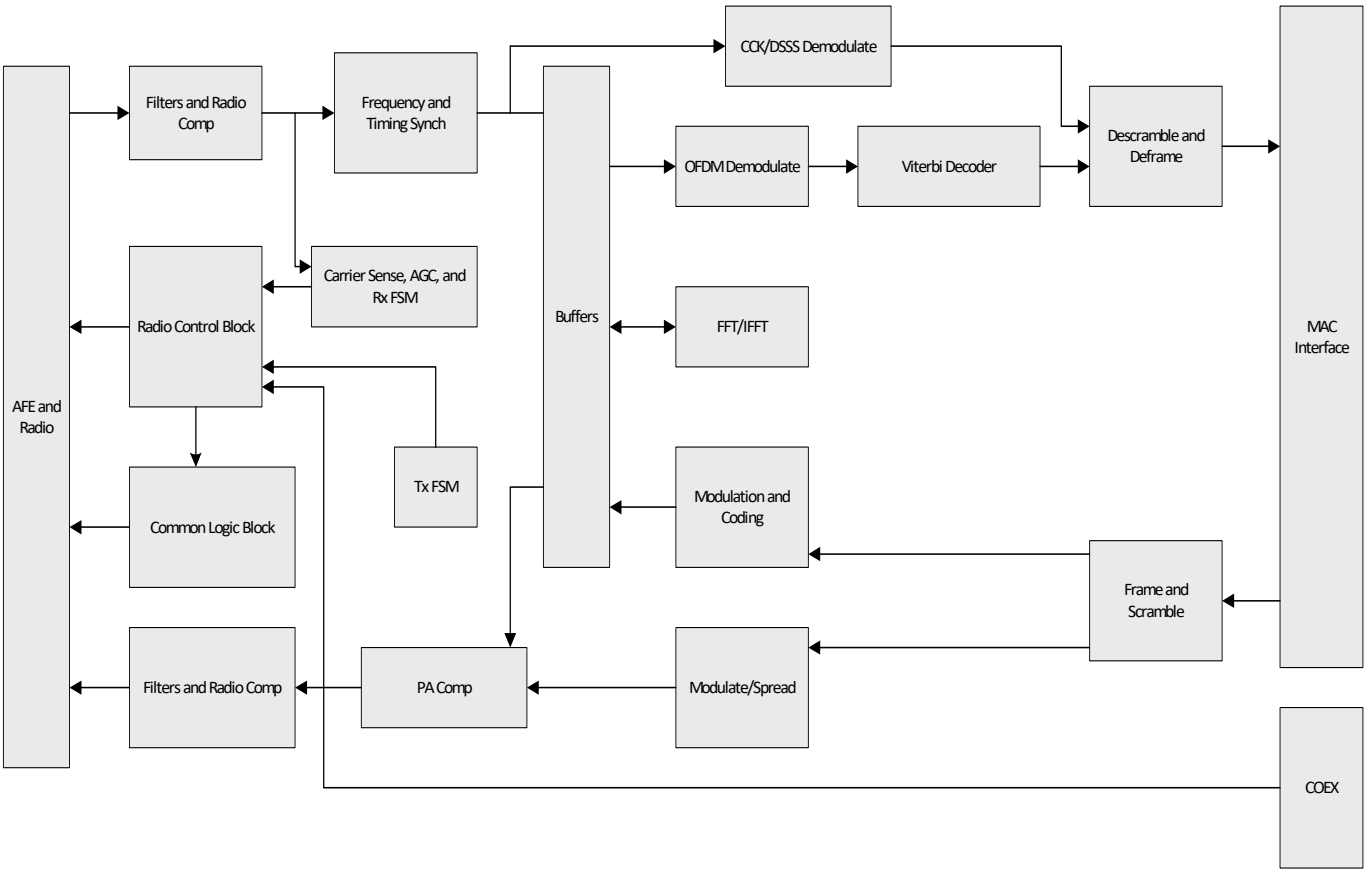
The CYW5459x WLAN PHY is designed to comply with IEEE 802.11ac and IEEE 802.11a/b/g/n specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 866.7 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for sharing an antenna between WL and Bluetooth to support simultaneous RX-RX.

The key PHY features include:

- Programmable data rates from MCS0–MCS9 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in IEEE 802.11ac
- Real simultaneous dual-band (RSDB), 2×2, and 80 + 80 MHz modes
- Improved performance with 2×2 channel smoothing support
- Short GI in TX and RX
- Beamforming
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction
- Supports IEEE 802.11d/h for worldwide operation, designed to meet FCC and other worldwide regulatory requirements
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Closed loop-transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Available per-packet channel quality and signal strength measurements

Figure 23. WLAN PHY Block Diagram



11. WLAN Radio Subsystem

The CYW5459x includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Twenty RF control signals are available (10 per core) to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

The CYW5459x includes an integrated dual-band WLAN RF radio that follows an RSDB architecture, using two RFPLLs, where each core can operate independently. The same radio can be configured in MIMO mode, whereas one RFPLL is used to drive both of the cores and MIMO operation is achieved.

11.1 Receiver Path

The CYW5459x has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low noise amplifier (LNA) in the 2.4 GHz path in CORE0 (can be optional) is shared between the Bluetooth and WLAN receivers, whereas the 5 GHz receive path and the CORE 1 2.4 GHz receive path have dedicated on-chip LNAs. Control signals are available that can support the use of external LNAs for each band, which can increase the receive sensitivity by several dB.

11.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output power while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications, and without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated.

11.3 Calibration

The CYW5459x features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

12. Pinout and Signal Descriptions

12.1 Ball Maps

Figure 24 and Figure 25 show the CYW5459x WLBGA ball map.

Figure 24. CYW5459x WLBGA Ball Map, A1–J12 (Package Bottom View — Balls Facing Up)

J	H	G	F	E	D	C	B	A	
	GPIO_6	GPIO_10	VDDC	PCIE_CLKREQ_L	PCIE_RDP0	PCIE_RDN0	PCIE_REFCLKP	PCIE_REFCLKN	12
GPIO_4	VDDC	GPIO_7	GPIO_9	PCIE_PERST_L	RXTX_AVDD1p2	PCIE_TESTN	PCIE_TESTP	PCIE_TDN0	11
GPIO_5	GPIO_8	GPIO_11	VDDIO	PCI_PME_L	PLL_AVSS	RXTX_AVSS	PLL_AVDD1p2	PCIE_TDP0	10
GPIO_3	VSSC		GPIO_13	JTAG_SEL	VSSC	VDDC			9
GPIO_14		AVSS_BBPLL	AVDD_BBPLL	GPIO_16	GPIO_12		SDIO_CMD	SDIO_CLK	8
VSSC	VDDC	VSSC	VSSC	VSSC	GPIO_15	GPIO_17	VDDIO_SD	SDIO__DATA_3	7
BT_UART_TXD	BT_PCM_SYNC	BT_PCM_CLK	RF_SW_CTRL_1	RF_SW_CTRL_0	VDDIO_RF		SDIO__DATA_0	SDIO__DATA_2	6
VSSC	RF_SW_CTRL_4	RF_SW_CTRL_3	RF_SW_CTRL_2	GPIO_18	GPIO_19		VDDC	SDIO__DATA_1	5
VSSC	RF_SW_CTRL_7	RF_SW_CTRL_6	RF_SW_CTRL_5	WL_REG_ON		VDDC_MEM			4
BT_VDDC	RF_SW_CTRL_8	WCC_VDDIO	BT_REG_ON	VOUT_MEMLPLDO	VSSC	VDDC	PMU_AVSS	VSSC	3
BT_PCM_IN	RF_SW_CTRL_9	WPT_1P8	SYS_VDDIO	VOUT_3P3	VOUT_LNLDO	VOUT_CLDO	VOUT_HLDO	SR_VLX	2
	VSSC	VOUT_PA3P3	LDO_VDDBAT5V	WPT_3P3	VOUT_BTLDO2P5	LDO_VDD1P5	SR_VDDBAT5V	SR_PVSS	1
J	H	G	F	E	D	C	B	A	

Figure 25. CYW5459x WLBGA Ball Map, K1–V12(Package Bottom View — Balls Facing Up)

	V	U	T	R	P	N	M	L	K
12	WRF_PA_VDD3P3_core1		WRF_PAOUT_2G_core1	WRF_RFIN_2G_core1	RF_SW_CTRL_12	RF_SW_CTRL_15		RF_SW_CTRL_19	GPIO_0
11	WRF_PAOUT_5G_core1	WRF_PA_GND3P3_core1	WRF_TXMIX_VDD_core1	WRF_RX2G_GND_core1		RF_SW_CTRL_11	RF_SW_CTRL_14	RF_SW_CTRL_18	GPIO_1
10	WRF_RFIN_5G_core1	WRF_GENERAL2_GND_core1	WRF_AFE_GND_core1	WRF_GPAIO_OUT_core1	VSSC	RF_SW_CTRL_10	RF_SW_CTRL_13	VDDC	GPIO_2
9	WRF_RX5G_GND_core1	WRF_AFE_VDD1P35_core1	WRF_GENERAL_GND_core1	WRF_EXT_TSSIA_core1		VDDC	VDDIO_RF	RF_SW_CTRL_17	RF_SW_CTRL_16
8	WRF_PMU_VDD1P35_core1	WRF_SYNTH_VDD1P2_core1	WRF_SYNTH_GND_core1	WRF_VCO_GND_core1		VSSC	BT_UART_RTS_N	BT_UART_CTS_N	VDDIO
7	WRF_XTAL_XOP_core0	WRF_XTAL_VDD1P2_core0	WRF_XTAL_VDD1P35_core1	WRF_SYNTH_VDD3P3_core1		VDDC		BT_I2S_WS	BT_I2S_CLK
6	WRF_XTAL_XON_core0	WRF_XTAL_GND1P2_core0	WRF_XTAL_VDD1P35_core0	WRF_SYNTH_VDD3P3_core0		LPO_IN	BT_I2S_DO	BT_GPIO_2	VDDC
5	WRF_PMU_VDD1P35_core0	WRF_SYNTH_VDD1P2_core0	WRF_SYNTH_GND_core0	WRF_VCO_GND_core0		CLK_REQ	BT_I2S_DI	BT_GPIO_3	BT_UART_RXD
4	WRF_RX5G_GND_core0	WRF_AFE_VDD1P35_core0	WRF_GENERAL_GND_core0	WRF_EXT_TSSIA_core0	BT_DEV_WAKE	BT_HOST_WAKE	VSSC	BT_VDDC	BT_VDDO
3	WRF_RFIN_5G_core0	WRF_GENERAL2_GND_core0	WRF_AFE_GND_core0	WRF_GPAIO_OUT_core0	BT_VCOVDD1p2	BT_VCOVSS	BT_IFVSS	BT_PCM_OUT	VSSC
2	WRF_PAOUT_5G_core0	WRF_PA_GND3P3_core0	WRF_TXMIX_VDD_core0	WRF_RX2G_GND_core0	BT_LNAVDD1p2	BT_LNAVSS	BT_PLLVSS	BT_GPIO_5	BT_VDDC
1	WRF_PA_VDD3P3_core0		WRF_PAOUT_2G_core0	WRF_RFIN_2G_core0	BT_RFOP	BT_PAVDD2p5	BT_PLLVDD1p2	BT_IFVDD1p2	BT_GPIO_4
	V	U	T	R	P	N	M	L	K

12.2 Pin List

12.2.1 Pin List by Number

This section provides the pin list by number. For pin list by name, see Pin List by Name on page 52.

Table 16. Pin List by Number

Ball No.	Name
A1	SR_PVSS
A2	SR_VLX
A3	VSSC
A5	SDIO_DATA_1
A6	SDIO_DATA_2
A7	SDIO_DATA_3
A8	SDIO_CLK
A10	PCIE_TDP0
A11	PCIE_TDN0
A12	PCIE_REFCLKN
B1	SR_VDDBAT5V
B2	VOUT_HLDO
B3	PMU_AVSS
B5	VDDC
B6	SDIO_DATA_0
B7	VDDIO_SD
B8	SDIO_CMD
B10	PLL_AVDD1P2
B11	PCIE_TESTP
B12	PCIE_REFCLKP
C1	LDO_VDD1P5
C2	VOUT_CLDO
C3	VDDC
C4	VDDC_MEM
C7	GPIO_17
C9	VDDC
C10	RXTX_AVSS
C11	PCIE_TESTN
C12	PCIE_RDN0
D1	VOUT_BTLDO2P5
D2	VOUT_LNLDO
D3	VSSC
D5	GPIO_19
D6	VDDIO_RF
D7	GPIO_15
D8	GPIO_12

Table 16. Pin List by Number (Cont.)

Ball No.	Name
D9	VSSC
D10	PLL_AVSS
D11	RXTX_AVDD1P2
D12	PCIE_RDP0
E1	WPT_3P3
E2	VOUT_3P3
E3	VOUT_MEMLPLDO
E4	WL_REG_ON
E5	GPIO_18
E6	RF_SW_CTRL_0
E7	VSSC
E8	GPIO_16
E9	JTAG_SEL
E10	PCI_PME_L
E11	PCIE_PERST_L
E12	PCIE_CLKREQ_L
F1	LDO_VDDBAT5V
F2	SYS_VDDIO
F3	BT_REG_ON
F4	RF_SW_CTRL_5
F5	RF_SW_CTRL_2
F6	RF_SW_CTRL_1
F7	VSSC
F8	AVDD_BBPLL
F9	GPIO_13
F10	VDDIO
F11	GPIO_9
F12	VDDC
G1	VOUT_PA3P3
G2	WPT_1P8
G3	WCC_VDDIO
G4	RF_SW_CTRL_6
G5	RF_SW_CTRL_3
G6	BT_PCM_CLK
G7	VSSC
G8	AVSS_BBPLL
G10	GPIO_11

Table 16. Pin List by Number (Cont.)

Ball No.	Name
G11	GPIO_7
G12	GPIO_10
H1	BT_VSSC
H2	RF_SW_CTRL_9
H3	RF_SW_CTRL_8
H4	RF_SW_CTRL_7
H5	RF_SW_CTRL_4
H6	BT_PCM_SYNC
H7	VDDC
H9	VSSC
H10	GPIO_8
H11	VDDC
H12	GPIO_6
J2	BT_PCM_IN
J3	BT_VDDC
J4	VSSC
J5	VSSC
J6	BT_UART_TXD
J7	VSSC
J8	GPIO_14
J9	GPIO_3
J10	GPIO_5
J11	GPIO_4
K1	BT_GPIO_4
K2	BT_VDDC
K3	BT_VSSC
K4	BT_VDDO
K5	BT_UART_RXD
K6	VDDC
K8	VDDIO
K9	RF_SW_CTRL_16
K10	GPIO_2
K11	GPIO_1
K12	GPIO_0
L1	BT_IFVDD1P2
L2	BT_GPIO_5
L3	BT_PCM_OUT
L4	BT_VDDC
L5	BT_GPIO_3
L6	BT_GPIO_2

Table 16. Pin List by Number (Cont.)

Ball No.	Name
L7	BT_I2S_WS
L8	BT_UART_CTS_N
L9	RF_SW_CTRL_17
L10	VDDC
L11	RF_SW_CTRL_18
L12	RF_SW_CTRL_19
M1	BT_PLLVDD1P2
M2	BT_PLLVSS
M3	BT_IFVSS
M4	BT_VSSC
M5	BT_I2S_DI
M6	BT_I2S_DO
M8	BT_UART_RTS_N
M9	VDDIO_RF
M10	RF_SW_CTRL_13
M11	RF_SW_CTRL_14
N1	BT_PAVDD2P5
N2	BT_LNAVSS
N3	BT_VCOVSS
N4	BT_HOST_WAKE
N5	CLK_REQ
N6	LPO_IN
N7	VDDC
N8	VSSC
N9	VDDC
N10	RF_SW_CTRL_10
N11	RF_SW_CTRL_11
N12	RF_SW_CTRL_15
P1	BT_RFOP
P2	BT_LNAVDD1P2
P3	BT_VCOVDD1P2
P4	BT_DEV_WAKE
P10	VSSC
P12	RF_SW_CTRL_12
R1	WRF_RFIN_2G_CORE0
R2	WRF_RX2G_GND_CORE0
R3	WRF_GPAIO_OUT_CORE0
R4	WRF_EXT_TSSIA_CORE0
R5	WRF_VCO_GND_CORE0
R6	WRF_SYNTH_VDD3P3_CORE0

Table 16. Pin List by Number (Cont.)

Ball No.	Name
R7	WRF_SYNTH_VDD3P3_CORE1
R8	WRF_VCO_GND_CORE1
R9	WRF_EXT_TSSIA_CORE1
R10	WRF_GPAIO_OUT_CORE1
R11	WRF_RX2G_GND_CORE1
R12	WRF_RFIN_2G_CORE1
T1	WRF_PAOUT_2G_CORE0
T2	WRF_TXMIX_VDD_CORE0
T3	WRF_AFE_GND_CORE0
T4	WRF_GENERAL_GND_CORE0
T5	WRF_SYNTH_GND_CORE0
T6	WRF_XTAL_VDD1P35_CORE0
T7	WRF_XTAL_VDD1P35_CORE1
T8	WRF_SYNTH_GND_CORE1
T9	WRF_GENERAL_GND_CORE1
T10	WRF_AFE_GND_CORE1
T11	WRF_TXMIX_VDD_CORE1
T12	WRF_PAOUT_2G_CORE1
U2	WRF_PA_GND3P3_CORE0
U3	WRF_GENERAL2_GND_CORE0
U4	WRF_AFE_VDD1P35_CORE0
U5	WRF_SYNTH_VDD1P2_CORE0
U6	WRF_XTAL_GND1P2_CORE0
U7	WRF_XTAL_VDD1P2_CORE0
U8	WRF_SYNTH_VDD1P2_CORE1
U9	WRF_AFE_VDD1P35_CORE1
U10	WRF_GENERAL2_GND_CORE1
U11	WRF_PA_GND3P3_CORE1
V1	WRF_PA_VDD3P3_CORE0
V2	WRF_PAOUT_5G_CORE0
V3	WRF_RFIN_5G_CORE0
V4	WRF_RX5G_GND_CORE0
V5	WRF_PMU_VDD1P35_CORE0
V6	WRF_XTAL_XON_CORE0
V7	WRF_XTAL_XOP_CORE0
V8	WRF_PMU_VDD1P35_CORE1
V9	WRF_RX5G_GND_CORE1
V10	WRF_RFIN_5G_CORE1
V11	WRF_PAOUT_5G_CORE1
V12	WRF_PA_VDD3P3_CORE1

12.2.2 Pin List by Name

This sections provides the pin list by name. For pin list by number, see Pin List by Number on page 49.

Table 17. CYW5459x Pin List by Name

Name	Ball No.
AVDD_BBPLL	F8
AVSS_BBPLL	G8
BT_DEV_WAKE	P4
BT_GPIO_2	L6
BT_GPIO_3	L5
BT_GPIO_4	K1
BT_GPIO_5	L2
BT_HOST_WAKE	N4
BT_I2S_CLK	K7
BT_I2S_DI	M5
BT_I2S_DO	M6
BT_I2S_WS	L7
BT_IFVDD1P2	L1
BT_IFVSS	M3
BT_LNAVDD1P2	P2
BT_LNAVSS	N2
BT_PAVDD2P5	N1
BT_PCM_CLK	G6
BT_PCM_IN	J2
BT_PCM_OUT	L3
BT_PCM_SYNC	H6
BT_PLLVDD1P2	M1
BT_PLLVSS	M2
BT_REG_ON	F3
BT_RFOP	P1
BT_UART_CTS_N	L8
BT_UART_RTS_N	M8
BT_UART_RXD	K5
BT_UART_TXD	J6
BT_VCOVDD1P2	P3
BT_VCOVSS	N3
BT_VDDC	J3
BT_VDDC	K2
BT_VDDC	L4
BT_VDDO	K4
BT_VSSC	H1
BT_VSSC	K3
BT_VSSC	M4
CLK_REQ	N5
PMU_AVSS	B3

Name	Ball No.
GPIO_0	K12
GPIO_1	K11
GPIO_10	G12
GPIO_11	G10
GPIO_12	D8
GPIO_13	F9
GPIO_14	J8
GPIO_15	D7
GPIO_16	E8
GPIO_17	C7
GPIO_18	E5
GPIO_19	D5
GPIO_2	K10
GPIO_3	J9
GPIO_4	J11
GPIO_5	J10
GPIO_6	H12
GPIO_7	G11
GPIO_8	H10
GPIO_9	F11
VSSC	F7
VSSC	G7
JTAG_SEL	E9
LDO_VDD1P5	C1
LDO_VDDBAT5V	F1
LPO_IN	N6
PCI_PME_L	E10
PCIE_CLKREQ_L	E12
PCIE_PERST_L	E11
PCIE_RDN0	C12
PCIE_RDP0	D12
PCIE_REFCLKN	A12
PCIE_REFCLKP	B12
PCIE_TDN0	A11
PCIE_TDP0	A10
PCIE_TESTN	C11
PCIE_TESTP	B11
PLL_AVDD1P2	B10
PLL_AVSS	D10
VDDIO_RF	M9

Table 17. CYW5459x Pin List by Name (Cont.)

Name	Ball No.
RF_SW_CTRL_0	E6
RF_SW_CTRL_1	F6
RF_SW_CTRL_10	N10
RF_SW_CTRL_11	N11
RF_SW_CTRL_12	P12
RF_SW_CTRL_13	M10
RF_SW_CTRL_14	M11
RF_SW_CTRL_15	N12
RF_SW_CTRL_16	K9
RF_SW_CTRL_17	L9
RF_SW_CTRL_18	L11
RF_SW_CTRL_19	L12
RF_SW_CTRL_2	F5
RF_SW_CTRL_3	G5
RF_SW_CTRL_4	H5
RF_SW_CTRL_5	F4
RF_SW_CTRL_6	G4
RF_SW_CTRL_7	H4
RF_SW_CTRL_8	H3
RF_SW_CTRL_9	H2
RXTX_AVDD1P2	D11
RXTX_AVSS	C10
SR_PVSS	A1
SR_VDDBAT5V	B1
SR_VLX	A2
SYS_VDDIO	F2
VDDC	B5
VDDC	C3
VDDC	C9
VDDC	F12
VDDC	H7
VDDC	H11
VDDC	K6
VDDC	L10
VDDC	N7
VDDC	N9
VDDC_MEM	C4
VDDIO	F10
VDDIO	K8
VDDIO_RF	D6
WRF_PAOUT_5G_CORE0	V2

Name	Ball No.
VDDIO	B7
VOUT_3P3	E2
VOUT_BTLDO2P5	D1
VOUT_CLDO	C2
VOUT_HLDO	B2
VOUT_LNLDO	D2
VOUT_MEMLPLDO	E3
VOUT_PA3P3	G1
VSSC	A3
VSSC	D3
VSSC	D9
VSSC	E7
VSSC	H9
VSSC	J4
VSSC	J5
VSSC	J7
VSSC	N8
VSSC	P10
WCC_VDDIO	G3
WL_REG_ON	E4
WPT_1P8	G2
WPT_3P3	E1
WRF_AFE_GND_CORE0	T3
WRF_AFE_GND_CORE1	T10
WRF_AFE_VDD1P35_CORE0	U4
WRF_AFE_VDD1P35_CORE1	U9
WRF_EXT_TSSIA_CORE0	R4
WRF_EXT_TSSIA_CORE1	R9
WRF_GENERAL_GND_CORE0	T4
WRF_GENERAL_GND_CORE1	T9
WRF_GENERAL2_GND_CORE0	U3
WRF_GENERAL2_GND_CORE1	U10
WRF_GPAIO_OUT_CORE0	R3
WRF_GPAIO_OUT_CORE1	R10
WRF_PA_GND3P3_CORE0	U2
WRF_PA_GND3P3_CORE1	U11
WRF_PA_VDD3P3_CORE0	V1
WRF_PA_VDD3P3_CORE1	V12
WRF_PAOUT_2G_CORE0	T1
WRF_PAOUT_2G_CORE1	T12
WRF_SYNTH_VDD1P2_CORE0	U5

Table 17. CYW5459x Pin List by Name (Cont.)

Name	Ball No.
WRF_PAOUT_5G_CORE1	V11
WRF_PMU_VDD1P35_CORE0	V5
WRF_PMU_VDD1P35_CORE1	V8
WRF_RFIN_2G_CORE0	R1
WRF_RFIN_2G_CORE1	R12
WRF_RFIN_5G_CORE0	V3
WRF_RFIN_5G_CORE1	V10
WRF_RX2G_GND_CORE0	R2
WRF_RX2G_GND_CORE1	R11
WRF_RX5G_GND_CORE0	V4
WRF_RX5G_GND_CORE1	V9
WRF_SYNTH_GND_CORE0	T5
WRF_SYNTH_GND_CORE1	T8

Name	Ball No.
WRF_SYNTH_VDD1P2_CORE1	U8
WRF_SYNTH_VDD3P3_CORE0	R6
WRF_SYNTH_VDD3P3_CORE1	R7
WRF_TXMIX_VDD_CORE0	T2
WRF_TXMIX_VDD_CORE1	T11
WRF_VCO_GND_CORE0	R5
WRF_VCO_GND_CORE1	R8
WRF_XTAL_GND1P2_CORE0	U6
WRF_XTAL_VDD1P2_CORE0	U7
WRF_XTAL_VDD1P35_CORE0	T6
WRF_XTAL_VDD1P35_CORE1	T7
WRF_XTAL_XON_CORE0	V6
WRF_XTAL_XOP_CORE0	V7

12.3 Signal Descriptions

The signal name, type, and description of each pin in the CYW5459x is listed in Table 18. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 18. CYW5459x WLBGA Signal Descriptions

Ball	Signal Name	Type	Description
WLAN and Bluetooth Receive RF Signal Interface			
R1	WRF_RFIN_2G_CORE0	I	2.4 GHz Bluetooth and WLAN CORE0 receiver shared input.
R12	WRF_RFIN_2G_CORE1	I	2.4 GHz Bluetooth and WLAN CORE1 receiver shared input.
V3	WRF_RFIN_5G_CORE0	I	5 GHz WLAN CORE0 receiver input.
V10	WRF_RFIN_5G_CORE1	I	5 GHz WLAN CORE1 receiver input.
T1	WRF_PAOUT_2G_CORE0	O	2.4 GHz WLAN CORE0 PA output.
T12	WRF_PAOUT_2G_CORE1	O	2.4 GHz WLAN CORE1 PA output.
V2	WRF_PAOUT_5G_CORE0	O	5 GHz WLAN CORE0 PA output.
V11	WRF_PAOUT_5G_CORE1	O	5 GHz WLAN CORE1 PA output.
R4	WRF_EXT_TSSIA_CORE0	I	5 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
R9	WRF_EXT_TSSIA_CORE1	I	5 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
R3	WRF_GPAIO_OUT_CORE0	I	GPIO or 2.4 GHz TSSI CORE0 input from an optional external power amplifier/power detector.
R10	WRF_GPAIO_OUT_CORE1	I	GPIO or 2.4 GHz TSSI CORE1 input from an optional external power amplifier/power detector.
RF Switch Control Lines			
E6	RF_SW_CTRL_0	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
F6	RF_SW_CTRL_1	O	
F5	RF_SW_CTRL_2	O	
G5	RF_SW_CTRL_3	O	
H5	RF_SW_CTRL_4	O	
F4	RF_SW_CTRL_5	O	
G4	RF_SW_CTRL_6	O	
H4	RF_SW_CTRL_7	O	
H3	RF_SW_CTRL_8	O	
H2	RF_SW_CTRL_9	O	
N10	RF_SW_CTRL_10	O	
N11	RF_SW_CTRL_11	O	
P12	RF_SW_CTRL_12	O	
M10	RF_SW_CTRL_13	O	
M11	RF_SW_CTRL_14	O	
N12	RF_SW_CTRL_15	O	
K9	RF_SW_CTRL_16	O	
L9	RF_SW_CTRL_17	O	
L11	RF_SW_CTRL_18	O	
L12	RF_SW_CTRL_19	O	
WLAN PCI Express Interface			
E12	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.

Table 18. CYW5459x WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
E11	PCIE_PERST_L	I	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1. PCIE_PERST_L pad excludes internal pull-up.
C12	PCIE_RDN0	I	Receiver differential pair (×1 lane).
D12	PCIE_RDP0	I	
A12	PCIE_REFCLKN	I	PCIE Differential Clock inputs (negative and positive). 100 MHz differential.
B12	PCIE_REFCLKP	I	
A11	PCIE_TDN0	O	Transmitter differential pair (×1 lane).
A10	PCIE_TDP0	O	
E10	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
B11	PCIE_TESTP	–	PCIe test pins.
C11	PCIE_TESTN	–	
WLAN SDIO Bus Interface **Note:** These signals can support alternate functionality depending on package and host interface mode. See Table 22 on page 61 for additional details.			
A8	SDIO_CLK	I	SDIO clock input.
B8	SDIO_CMD	I/O	SDIO command line.
B6	SDIO_DATA_0	I/O	SDIO data line 0.
A5	SDIO_DATA_1	I/O	SDIO data line 1.
A6	SDIO_DATA_2	I/O	SDIO data line 2.
A7	SDIO_DATA_3	I/O	SDIO data line 3.
WLAN GPIO Interface **Note** The GPIO signals can be multiplexed via software and the JTAG_SEL pin to support other functions. See Table 20 on page 60 and Table 22 for additional details.			
K12	GPIO_0	I/O	Programmable GPIO pins.
K11	GPIO_1	I/O	
K10	GPIO_2	I/O	
J9	GPIO_3	I/O	
J11	GPIO_4	I/O	
J10	GPIO_5	I/O	
H12	GPIO_6	I/O	
G11	GPIO_7	I/O	
H10	GPIO_8	I/O	
F11	GPIO_9	I/O	
G12	GPIO_10	I/O	
G10	GPIO_11	I/O	
D8	GPIO_12	I/O	Programmable GPIO pins.
F9	GPIO_13	I/O	
J8	GPIO_14	I/O	
D7	GPIO_15	I/O	
E8	GPIO_16	I/O	
C7	GPIO_17	I/O	
E5	GPIO_18	I/O	
D5	GPIO_19	I/O	

Table 18. CYW5459x WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
JTAG Interface			
E9	JTAG_SEL	I/O	JTAG select: pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground. See Table 22 on page 61 for the JTAG signal pins.
Clocks			
V6	WRF_XTAL_XON_CORE0	O	XTAL oscillator output.
V7	WRF_XTAL_XOP_CORE0	I	XTAL oscillator input.
N6	LPO_IN	I	External sleep clock input (32.768 kHz).
N5	CLK_REQ	I/O	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.
Bluetooth Transceiver			
P1	BT_RFOP	O	Bluetooth PA output.
Bluetooth PCM			
G6	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input).
J2	BT_PCM_IN	I	PCM data input.
L3	BT_PCM_OUT	O	PCM data output.
H6	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input).
Bluetooth UART			
L8	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
M8	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. Bluetooth LED control pin.
K5	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
J6	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
Bluetooth I^2S			
K7	BT_I2S_CLK	I/O	I^2S clock, can be master (output) or slave (input).
M6	BT_I2S_DO	I/O	I^2S data output.
M5	BT_I2S_DI	I/O	I^2S data input.
L7	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input).
Bluetooth GPIO			
L6	BT_GPIO_2	I/O	Bluetooth general-purpose I/O.
L5	BT_GPIO_3	I/O	
K1	BT_GPIO_4	I/O	
L2	BT_GPIO_5	I/O	
Miscellaneous			
E4	WL_REG_ON	I	Used by PMU to power up or power down the internal CYW5459x regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
F3	BT_REG_ON	I	Used by PMU to power up or power down the internal CYW5459x regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
P4	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE.
N4	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE.
Integrated Voltage Regulators			
B1	SR_VDDBAT5V	I	Power VBAT.
A2	SR_VLX	O	CBUCK switching regulator output. Refer to Table 41 on page 90 for details of the inductor and capacitor required on this output.
C1	LDO_VDD1P5	I	LNLDO input.

Table 18. CYW5459x WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
F1	LDO_VDDBAT5V	I	LDO VBAT.
U7	WRF_XTAL_VDD1P2_CORE0	O	XTAL LDO CORE0 output (1.2V).
T6	WRF_XTAL_VDD1P35_CORE0	I	XTAL LDO CORE0 input (1.35V).
T7	WRF_XTAL_VDD1P35_CORE1	I	XTAL LDO CORE1 input (1.35V).
D2	VOUT_LNLDO	O	Output of LNLDO.
C2	VOUT_CLDO	O	Output of core LDO.
D1	VOUT_BTLDO2P5	O	Output of Bluetooth LDO.
E2	VOUT_3P3	O	LDO 3.3V output.
G1	VOUT_PA3P3	O	Voltage sense pin for PA LDO 3.3V output.
Bluetooth Supplies			
N1	BT_PAVDD2P5	PWR	Bluetooth PA power supply.
P2	BT_LNAVDD1P2	PWR	Bluetooth LNA power supply.
L1	BT_IFVDD1P2	PWR	Bluetooth IF block power supply.
M1	BT_PLLVDD1P2	PWR	Bluetooth RF PLL power supply.
P3	BT_VCOVDD1P2	PWR	Bluetooth RF power supply.
K4	BT_VDDO	PWR	1.8V or 3.3V VIO supply.
WLAN Supplies			
V5	WRF_PMU_VDD1P35_CORE0	PWR	PMU core0 1.35V supply.
V8	WRF_PMU_VDD1P35_CORE1	PWR	PMU core1 1.35V supply.
R7	WRF_SYNTH_VDD3P3_CORE1	PWR	SYNTH core1 VDD3.3V supply.
R6	WRF_SYNTH_VDD3P3_CORE0	PWR	SYNTH core0 VDD3.3V supply.
U4	WRF_AFE_VDD1P35_CORE0	PWR	AFE core0 1.35V supply.
U9	WRF_AFE_VDD1P35_CORE1	PWR	AFE core1 1.35V supply.
V1	WRF_PA_VDD3P3_CORE0	PWR	Core0 PA 3.3V VBAT supply.
V12	WRF_PA_VDD3P3_CORE1	PWR	Core1 PA 3.3V VBAT supply.
U5	WRF_SYNTH_VDD1P2_CORE0	PWR	SYNTH CORE0 VDD 1.2V supply.
U8	WRF_SYNTH_VDD1P2_CORE1	PWR	SYNTH CORE1 VDD 1.2V supply.
T2	WRF_TXMIX_VDD_CORE0	PWR	TX Mixer core0 VDD 3.3V supply.
T11	WRF_TXMIX_VDD_CORE1	PWR	TX Mixer core1 VDD 3.3V supply.
Miscellaneous Supplies			
B5, C3, C9, F12, H7, H11, K6, L10, N7, N9	VDDC	PWR	1.2V core supply for WLAN.
B7, F10, K8	VDDIO	PWR	1.8 V/3.3 V supply for WLAN. Must be directly connected to PMU_VDDIO and BT_VDDO on the PCB.
J3, K2, L4	BT_VDDC	PWR	1.2 V core supply for Bluetooth.
D6, M9	VDDIO_RF	PWR	IO supply for RF switch control pads (3.3 V).
F8	AVDD_BBPLL	PWR	Baseband PLL supply.
B10	PLL_AVDD1P2	PWR	1.2 V supply for PCIe PLL.
D11	RXTX_AVDD1P2	PWR	1.2 V supply for PCIE TX and RX.
B2	VOUT_HLDO	PWR	Output of host system interface core LDO 1.2 V supply.
C4	VDDC_MEM	PWR	Input power supply for the memory.
E3	VOUT_MEMLPLDO	PWR	Memory LDO output.
E1	WPT_3P3	PWR	Wireless charging 3.3 V supply for BTLDO2P5 and VBAT_SEL with internal switches.
G2	WPT_1P8	PWR	Wireless charging 1.8 V supply with internal switches.
F2	SYS_VDDIO	PWR	1.8 V or 3.3 V input of VDDIO_SEL.

Table 18. CYW5459x WLBGA Signal Descriptions (Cont.)

Ball	Signal Name	Type	Description
G3	WCC_VDDIO	PWR	1.8 V or 3.3 V input for LPLDO, WPTLDO, and chip VDDOP. Output of VDDIO_SEL.
Ground			
U6	WRF_XTAL_GND1P2_CORE0	GND	XTAL CORE0 ground.
R5	WRF_VCO_GND_CORE0	GND	CORE0 VCO ground.
R8	WRF_VCO_GND_CORE1	GND	CORE1 VCO ground.
T3	WRF_AFE_GND_CORE0	GND	CORE0 AFE ground.
T10	WRF_AFE_GND_CORE1	GND	CORE1 AFE ground.
T5	WRF_SYNTH_GND_CORE0	GND	SYNTH CORE0 ground.
T8	WRF_SYNTH_GND_CORE1	GND	SYNTH CORE1 ground.
T4	WRF_GENERAL_GND_CORE0	GND	General ground.
T9	WRF_GENERAL_GND_CORE1	GND	General ground.
U3	WRF_GENERAL2_GND_CORE0	GND	General ground.
U10	WRF_GENERAL2_GND_CORE1	GND	General ground.
R2	WRF_RX2G_GND_CORE0	GND	RX 2GHz CORE0 ground.
R11	WRF_RX2G_GND_CORE1	GND	RX 2GHz CORE1 ground.
V4	WRF_RX5G_GND_CORE0	GND	RX 5GHz CORE0 ground.
V9	WRF_RX5G_GND_CORE1	GND	RX 5GHz CORE1 ground.
U2	WRF_PA_GND3P3_CORE0	GND	PA CORE0 ground.
U11	WRF_PA_GND3P3_CORE1	GND	PA CORE1 ground.
A3, D3, D9, E7, F7, G7, H9, J7, N8, P10	VSSC	GND	Core ground for WLAN and Bluetooth.
A1	SR_PVSS	GND	Power ground.
B3	PMU_AVSS	GND	Quiet ground.
H1, K3, M4	BT_VSSC	GND	Bluetooth core ground.
M3	BT_IFVSS	GND	Bluetooth IF block ground.
M2	BT_PLLVSS	GND	Bluetooth PLL ground.
N3	BT_VCOVSS	GND	Bluetooth VCO ground.
G8	AVSS_BBPLL	GND	Baseband PLL ground.
N2	BT_LNAVSS	GND	Bluetooth LNA ground.
C10	RXTX_AVSS	GND	PCIe ground.
D10	PLL_AVSS	GND	PCIe ground.

12.4 WLAN/Bluetooth GPIO Signals and Strapping Options

The pins listed in Table 19 and Table 20 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note Refer to the reference board schematics for more information.

Table 19. Bluetooth GPIO Functions and Strapping Options

Pin Name	Default Function	Description
BT_GPIO2	0	1: Bluetooth Serial Flash is present. 0: Bluetooth Serial Flash is absent (default).

Note Not valid on wireless charging platform.

12.4.1 Strapping Options

Table 20. GPIO Strap Pins

Pin Name	Default Pull During Strapping	All Packages
GPIO_7	0	JTAG_ENABLE
GPIO_14	0	RSRC_INIT_0
GPIO_15	1	RSRC_INIT_1
GPIO_16	1	VTRIM_EN
GPIO_17	1	SDIO_PADVDDIO: 0 = 3.3 V, 1 = 1.8 V; when SDIO is enabled (strap from GPIO_18 is 0). SPROM_ABSENT: 0 = SPROM present, 1 = SPROM absent; when SDIO is disabled (strap from GPIO_18 is 1).
GPIO_18	1	SDIO_DISABLE: 0 = SDIO enabled, 1 = SDIO disabled; either PCIe or SDIO or both have to be present.
GPIO_19	1	PCIE_ENABLE: 0 = PCIe disabled, 1 = PCIe enabled; either PCIe or SDIO or both have to be present.

12.4.2 Host Interface Selection

Note The strapping options are defined in such a way that defaults have internal PU, so that it is easy to configure the strap value in opposite manner on a board (put a PD on the board).

Table 21. Host Interface Selection

PCIe Enable	GPIO_18	GPIO_17	Mode
1	1	1	PCIe; VDDIO_SD can be 3.3/1.8 V
1	1	0	PCIe + SPROM; VDDIO_SD can be 3.3/1.8 V
0	0	1	1.8 V SDIO; Connect VDDIO_SD to 1.8 V
0	0	0	3.3 V SDIO; Connect VDDIO_SD to 3.3 V
1	0	1	PCIe + SDIO(1.8V); VDDIO_SD should be 1.8 V
1	0	0	PCIe + SDIO (3.3V); VDDIO_SD should be 3.3 V
1	1	1	PCIe; VDDIO_SD can be 3.3/1.8 V

12.5 GPIO Alternative Signal Functions

Table 22. GPIO Alternative Signal Functions

Pin Names	HW Decided/Power ON Default[13]	GPIO_0	FAST_UART/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I²C	SPROM	MISC-0	MISC-1	MISC-2	Additional Functionality
	Function Select											
	0	2	3	4	5	6	7	8	9	10	11	
GPIO_0	TRISTATE_PDN	GPIO_8	–	GCI_GPIO_0	GCI_GPIO_11	–	–	–	–	–	–	WL_HOST_WAKE
GPIO_1	TRISTATE_IND	GPIO_9	–	GCI_GPIO_1	GCI_GPIO_12	–	–	–	RF_DISABLE_L	–	–	WL_DEV_WAKE
GPIO_2	JTAG_SEL? TCK: TRISTATE_IND	GPIO_10	FAST_UART_RX	GCI_GPIO_2	GCI_GPIO_13	–	–	–	TCK	–	–	–
GPIO_3	JTAG_SEL? TMS: TRISTATE_IIND	GPIO_11	FAST_UART_TX	GCI_GPIO_3	GCI_GPIO_14	–	–	–	TMS	–	–	–
GPIO_4	JTAG_SEL? TDI: TRISTATE_IND	GPIO_12	FAST_UART_CTS_IN	GCI_GPIO_4	GCI_GPIO_15	DBG_UART_RX	–	–	TDI	–	–	–
GPIO_5	JTAG_SEL? TDO: TRISTATE_IND	GPIO_13	FAST_UART_RTS_OUT	GCI_GPIO_0	GCI_GPIO_5	DBG_UART_TX	–	–	TDO	–	–	–
GPIO_6	JTAG_SEL? TRST_L: TRISTATE_IND	GPIO_14	–	GCI_GPIO_1	GCI_GPIO_6	DBG_UART_RX	–	–	TRST_L	–	–	–
GPIO_7	TRISTATE_IND	GPIO_15	–	GCI_GPIO_2	GCI_GPIO_7	DBG_UART_TX	–	–	PMU_TEST_O	–	–	–
GPIO_8	TRISTATE_IND	GPIO_0	FAST_UART_RX	GCI_GPIO_3	GCI_GPIO_8	–	GSIO_SDI	–	–	–	–	–
GPIO_9	TRISTATE_PUP	GPIO_1	FAST_UART_TX	GCI_GPIO_4	GCI_GPIO_9	–	GSIO_SDO	–	–	–	–	–
GPIO_10	TRISTATE_IND	GPIO_2	FAST_UART_CTS_IN	GCI_GPIO_0	GCI_GPIO_10	DBG_UART_RX	GSIO_CSN	–	–	–	–	–
GPIO_11	TRISTATE_PUP	GPIO_3	FAST_UART_RTS_OUT	GCI_GPIO_1	GCI_GPIO_11	DBG_UART_TX	GSIO_CLK	–	–	–	–	–
GPIO_12	TRISTATE_IND	GPIO_4	–	GCI_GPIO_2	GCI_GPIO_12	DBG_UART_RX	–	–	–	SDIO_SE	P_INT_OD	WL_LED1
GPIO_13	TRISTATE_IND	GPIO_5	–	GCI_GPIO_3	GCI_GPIO_13	DBG_UART_TX	–	–	–	–	–	WL_LED0
GPIO_14	TRISTATE_IND	GPIO_6	–	GCI_GPIO_4	GCI_GPIO_14	–	–	–	–	–	–	–
GPIO_15	TRISTATE_IND	GPIO_7	–	–	GCI_GPIO_15	–	–	–	–	–	–	–
GPIO_16	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
GPIO_17	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
GPIO_18	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
GPIO_19	TRISTATE_IND	–	–	–	–	–	–	–	–	–	–	–
SDIO_CLK	SDIO_EN ? SDIO_CLK: TRISTATE_IND	–	–	–	–	–	–	–	SDIO_AOS_CLK	TEST_SDIO_CLK	–	–

Note
13. In some rows, a ternary operator (condition **?** value if condition is true **:** value if condition is false) is used to represent a conditional assignment.

Table 22. GPIO Alternative Signal Functions (Cont.)

Pin Names	HW Decided/Power ON Default[13]	GPIO_0	FAST_UART/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I²C	SPROM	MISC-0	MISC-1	MISC-2	Additional Functionality
	Function Select											
	0	2	3	4	5	6	7	8	9	10	11	
SDIO_CMD	SDIO_EN ? SDIO_CMD: (SPROM_EN ? SPROM_CS: TRISTATE_IND)	GPIO_11	–	GCI_GPIO_0	–	–	–	SPROM_CS	SDIO_AOS_CMD	TEST_SDIO_CMD	–	–
SDIO_DATA_0	SDIO_EN ? SDIO_DATA_0: (SPROM_EN ? SPROM_CLK: TRISTATE_IND)	GPIO_12	–	GCI_GPIO_1	–	–	–	SPROM_CLK	SDIO_AOS_D0	TEST_SDIO_DATA_0	–	–
SDIO_DATA_1	SDIO_EN ? SDIO_DATA_1: (SPROM_EN ? SPROM_MISO: TRISTATE_IND)	GPIO_13	–	GCI_GPIO_2	–	–	–	SPROM_MISO	SDIO_AOS_D1	TEST_SDIO_DATA_1	–	–
SDIO_DATA_2	SDIO_EN ? SDIO_DATA_2: TRISTATE_IND	GPIO_14	–	GCI_GPIO_3	–	–	–	–	SDIO_AOS_D2	TEST_SDIO_DATA_2	–	–
SDIO_DATA_3	SDIO_EN ? SDIO_DATA_3: (SPROM_EN ? SPROM_MOSI: TRISTATE_IND)	GPIO_15	–	GCI_GPIO_4	–	–	–	SPROM_MOSI	SDIO_AOS_D3	TEST_SDIO_DATA_3	–	–
RF_SW_CTRL_0	RF_SW_CTRL_0	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_1	RF_SW_CTRL_1	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_2	RF_SW_CTRL_2	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_3	RF_SW_CTRL_3	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_4	RF_SW_CTRL_4	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_5	RF_SW_CTRL_5	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_6	RF_SW_CTRL_6	GPIO_8	GPIO_0	–	GCI_GPIO_8	–	GSIO_SDI	–	–	–	–	–
RF_SW_CTRL_7	RF_SW_CTRL_7	GPIO_9	GPIO_1	–	GCI_GPIO_9	–	GSIO_SDO	–	–	–	–	–
RF_SW_CTRL_8	RF_SW_CTRL_8	GPIO_10	GPIO_2	–	GCI_GPIO_10	DBG_UART_RX	GSIO_CSN	–	–	–	–	–
RF_SW_CTRL_9	RF_SW_CTRL_9	GPIO_11	GPIO_3	–	GCI_GPIO_11	DBG_UART_TX	GSIO_CLK	–	PALDO_PU	–	–	–
RF_SW_CTRL_10	RF_SW_CTRL_10	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_11	RF_SW_CTRL_11	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_12	RF_SW_CTRL_12	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_13	RF_SW_CTRL_13	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_14	RF_SW_CTRL_14	–	–	–	–	–	–	–	–	–	–	–

Note
13. In some rows, a ternary operator (condition **?** value if condition is true **:** value if condition is false) is used to represent a conditional assignment.

Table 22. GPIO Alternative Signal Functions (Cont.)

Pin Names	HW Decided/Power ON Default[13]	GPIO_0	FAST_UART/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I²C	SPROM	MISC-0	MISC-1	MISC-2	Additional Functionality
	Function Select											
	0	2	3	4	5	6	7	8	9	10	11	
RF_SW_CTRL_15	RF_SW_CTRL_15	–	–	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_16	RF_SW_CTRL_16	GPIO_12	GPIO_4	–	GCI_GPIO_12	–	GSIO_CLK	–	–	–	–	–
RF_SW_CTRL_17	RF_SW_CTRL_17	GPIO_13	GPIO_5	–	GCI_GPIO_13	–	GSIO_CSN	–	–	–	–	–
RF_SW_CTRL_18	RF_SW_CTRL_18	GPIO_14	GPIO_6	–	GCI_GPIO_14	DBG_UART_TX	GSIO_SDO	–	–	–	–	–
RF_SW_CTRL_19	RF_SW_CTRL_19	GPIO_15	GPIO_7	–	GCI_GPIO_15	DBG_UART_RX	GSIO_SDI	–	PALDO_PD	–	–	–

Note
13. In some rows, a ternary operator (condition **?** value if condition is true **:** value if condition is false) is used to represent a conditional assignment.

Table 23 defines status for all CYW5459x GPIOs based on the tristate test mode.

Table 23. GPIO Status Versus Test Modes

Test Mode	Function Select	Status of All GPIOs
TRISTATE_IND	12	Input disable
TRISTATE_PDN	13	PD
TRISTATE_PUP	14	PU
TRISTATE	15	Tristate

12.6 I/O States

The following notations are used in Table 24 on page 65:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- NoPull = Neither pulled up nor pulled down
- Where applicable, the default value is shown in bold brackets (for example, [default value])

Table 24. I/O States

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down can be disabled	I: PD Pull-down can be disabled	I: PD (of 200K)	I: PD (of 200K)	I: PD (of 200K)	–
SDIO DATA[14]	I/O	N	I/O: PU	I/O: PU	High-Z, NoPull	I/O: PU	I/O: PU	VDDIO_SD
SDIO CMD[14]	I/O	N	I/O: PU	I/O: PU	High-Z, NoPull	I/O: PU	I/O: PU	VDDIO_SD
SDIO_CLK[14]	I	N	I: NoPull	I: NoPull	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO_SD
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	I: PD	I: PD	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[15]	I: NoPull	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[15]	I: NoPull	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[15]	I: NoPull	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[15]	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[15]	I: NoPull	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO

Note
14. .n SDIO mode.
15. When JTAG is not enabled on the GPIO

Table 24. I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	I: PU	I: PU	I:PU	VDDIO
GPIO_10	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_16	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_18	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_19	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RF
CLK_REQ	O	Y	Open drain or push-pull (programmable).Active high.	Open drain or push-pull (programmable).Active high.	High-Z, NoPull	Open drain. Active high	Open drain. Active high	BT_VDDO
BT_HOST_WAKE	O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PD	BT_VDDO
BT_DEV_WAKE	I	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_GPIO_2, BT_GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_GPIO_4, BT_GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_CTS_N	I	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_RTS_N	O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_RXD	I	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_TXD	O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_PCM_CLK	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_IN	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_OUT	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_SYNC	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I^2S_CLK	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	BT_VDDO

Note
14. .n SDIO mode.
15. When JTAG is not enabled on the GPIO

Table 24. I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low-Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_REG_ON High and BT_REG_ON = 0) and VDDIOs are Present	Power Rail
BT_I^{2}S_DO	I/O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I^{2}S_DI	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I^{2}S_WS	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	BT_VDDO

Note
14. .n SDIO mode.
15. When JTAG is not enabled on the GPIO

13. DC Characteristics

13.1 Absolute Maximum Ratings

Table 25. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O[16]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[16]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C
Maximum input power for RX input ports[17]	–	13	dBm
DC supply voltage for wireless charging	WPT_3p3	–0.5 to 3.9	V
DC supply voltage for wireless charging	WPT_1p8 V	–0.5 to 3.9	V
DC supply voltage for WCC I/O	WCC_VDDIO V	–0.5 to 3.9	V

Note
16. Duration not to exceed 25% of the duty cycle.
17. Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 13 dBm at a 1.5% duty-cycle derated from a seven year lifetime.

13.2 Environmental Ratings

The environmental ratings are shown in Table 26.

Table 26. Environmental Ratings

Characteristic	Value	Unit	Conditions/Comments
Ambient Temperature (T_A)	–40 to +85	°C	Functional operation[18]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Note
18. The device is functional across this range of temperature.The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability. Transmit throughput throttling can lower throughput up to 25% of maximum throughput at 25°C depending on the thermal environment of operation.

13.3 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 27, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 27. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
DC supply voltage for VBAT	VBAT	3.0[19]	–	4.8[20]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO	1.62	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
DC supply voltage for wireless charging	WPT_1p8, WPT_3p3	1.62	–	3.63	V
DC supply voltage for WCC I/O	WCC_VDDIO	1.62	–	3.63	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	3.63[22]	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	3.63	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
PCIe Out-of-Band Signals (PCIE_PME_L and PCIE_CLKREQ_L)					
For VDDIO = 1.8V:					
Input high voltage	VIH	1.27	–	3.63[22]	V
Input low voltage	VIL	–	–	0.58	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO	–	3.63	V
Input low voltage	VIL	–	–	0.25 × VDDIO	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	3.63[22]	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V

Notes

19. The CYW5459x is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 4.5V.
20. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
21. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.
22. IO is failsafe to 3.63V.

Table 27. Recommended Operating Conditions and DC Characteristics (Cont.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:		–	–	–	
Input high voltage	VIH	2.00	–	3.63	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage@ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[21]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

Notes
19. The CYW5459x is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 4.5V.
20. The maximum continuous voltage is 5.25V. Voltage transients up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
21. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.
22. IO is failsafe to 3.63V.

13.4 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 28. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	2	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	300	V

14. Bluetooth RF Specifications

Unless otherwise stated, limit values apply for the conditions specified in Table 26 on page 68 and Table 27 on page 69. Typical values apply for an ambient temperature of +25°C.

Figure 26 shows the RF port locations for testing Bluetooth in a system configuration with two antennas. Only one of the two system antennas is available to Bluetooth in this configuration and, thus, only one antenna is shown.

Figure 26. RF Port Locations for Bluetooth Testing in Two-Antenna System

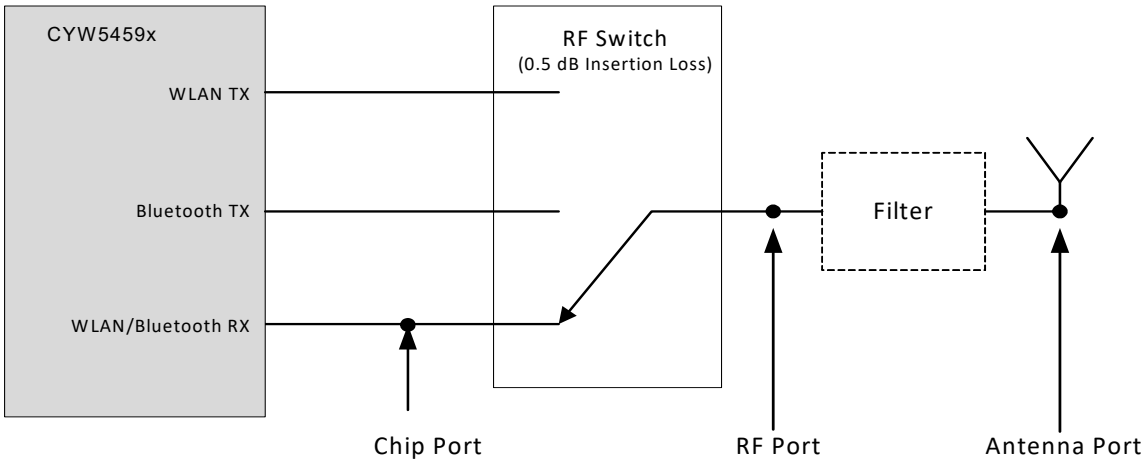
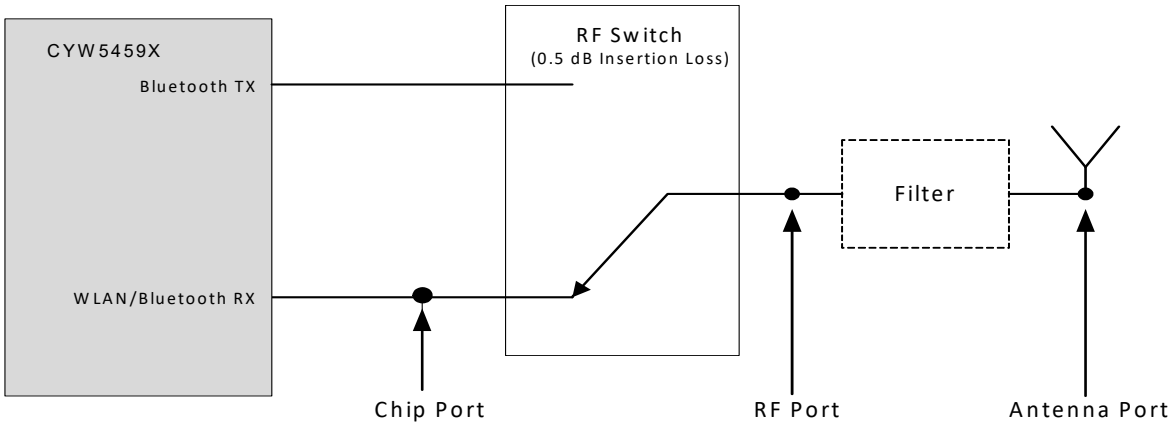


Figure 27 shows the RF port locations for testing Bluetooth in a system configuration with three antennas. In this system configuration, any one of the three system antennas can be used for Bluetooth.

Figure 27. RF Port Locations for Bluetooth Testing in Three-Antenna System



Note All Bluetooth specifications are measured at the chip port unless otherwise specified.

Table 29 provides the Bluetooth receiver RF specifications.

Table 29. Bluetooth Receiver RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Note The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity (dLNA)	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
RX sensitivity (sLNA)	GFSK, 0.1% BER, 1 Mbps	–	–95.3	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–97.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–91.5	–	dBm
Input IP3	–	–16.0	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
Interference Performance[23]					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	–	13.0	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20.0	dB
C/I co-channel	8-DPSK, 0.1% BER	–	–	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13.0	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27.0	–	dBm
2498–3000 MHz	0.1% BER	–	–27.0	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Notes
23. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
24. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = -90.5dBm for 1Mbps, -92.5dBm for 2Mbps.
25. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
26. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
27. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
28. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
29. Bluetooth reference level for the wanted signal at the Bluetooth chip port = -86.5dBm for 3Mbps.

Table 29. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Min	Typ	Max	Unit
Out-of-Band Blocking Performance, Modulated Interferer					
GFSK (1 Mbps)[24]					
698–716 MHz	WCDMA	–	–13.0	–	dBm
776–849 MHz	WCDMA	–	–14.0	–	dBm
824–849 MHz	GSM850	–	–13.0	–	dBm
824–849 MHz	WCDMA	–	–14.0	–	dBm
880–915 MHz	E-GSM	–	–13.0	–	dBm
880–915 MHz	WCDMA	–	–13.0	–	dBm
1710–1785 MHz	GSM1800	–	–18.0	–	dBm
1710–1785 MHz	WCDMA	–	–17.0	–	dBm
1850–1910 MHz	GSM1900	–	–19.0	–	dBm
1850–1910 MHz	WCDMA	–	–19.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20.0	–	dBm
1920–1980 MHz	WCDMA	–	–20.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–26.0	–	dBm
2530 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–23.0	–	dBm
2550 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2570 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2310 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–22.0	–	dBm
2330 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–21.0	–	dBm
2350 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–22.0	–	dBm
2370 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–26.0	–	dBm
2570–2620 MHz[27]	Band 38	–	–22.0	–	dBm
2545–2575 MHz[28]	XGP Band	–	–23.0	–	dBm
π/4-DPSK (2 Mbps)[24]					
698–716 MHz	WCDMA	–	–10.0	–	dBm
776–794 MHz	WCDMA	–	–10.0	–	dBm
824–849 MHz	GSM850	–	–11.0	–	dBm
824–849 MHz	WCDMA	–	–11.0	–	dBm
880–915 MHz	E-GSM	–	–10.0	–	dBm
880–915 MHz	WCDMA	–	–10.0	–	dBm

Notes
23. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
24. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = -90.5dBm for 1Mbps, -92.5dBm for 2Mbps.
25. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
26. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
27. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
28. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
29. Bluetooth reference level for the wanted signal at the Bluetooth chip port = -86.5dBm for 3Mbps.

Table 29. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Min	Typ	Max	Unit
1710–1785 MHz	GSM1800	–	–16.0	–	dBm
1710–1785 MHz	WCDMA	–	–15.0	–	dBm
1850–1910 MHz	GSM1900	–	–17.0	–	dBm
1850–1910 MHz	WCDMA	–	–16.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18.0	–	dBm
1920–1980 MHz	WCDMA	–	–17.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–19.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–26.0	–	dBm
2530 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2550 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2570 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2310 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–22.0	–	dBm
2330 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–21.0	–	dBm
2350 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–22.0	–	dBm
2370 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–26.0	–	dBm
2570–2620 MHz[27]	Band 38	–	–22.0	–	dBm
2545–2575 MHz[28]	XGP Band	–	–25.0	–	dBm
8-DPSK (3 Mbps)[29]					
698–716 MHz	WCDMA	–	–13.0	–	dBm
776–794 MHz	WCDMA	–	–13.0	–	dBm
824–849 MHz	GSM850	–	–13.0	–	dBm
824–849 MHz	WCDMA	–	–14.0	–	dBm
880–915 MHz	E-GSM	–	–13.0	–	dBm
880–915 MHz	WCDMA	–	–13.0	–	dBm
1710–1785 MHz	GSM1800	–	–18.0	–	dBm
1710–1785 MHz	WCDMA	–	–17.0	–	dBm
1850–1910 MHz	GSM1900	–	–19.0	–	dBm
1850–1910 MHz	WCDMA	–	–19.0	–	dBm
1880–1920 MHz	TD-SCDMA	–	–19.0	–	dBm
1920–1980 MHz	WCDMA	–	–19.0	–	dBm
2010–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500–2570 MHz	WCDMA	–	–23.0	–	dBm

Notes
23. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
24. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = -90.5dBm for 1Mbps, -92.5dBm for 2Mbps.
25. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
26. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
27. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
28. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
29. Bluetooth reference level for the wanted signal at the Bluetooth chip port = -86.5dBm for 3Mbps.

Table 29. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Min	Typ	Max	Unit
2510 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–26.0	–	dBm
2530 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–23.0	–	dBm
2550 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2570 MHz[25]	LTE band 7 FDD 20 MHz BW	–	–22.0	–	dBm
2310 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–23.0	–	dBm
2330 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–21.0	–	dBm
2350 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–22.0	–	dBm
2370 MHz[26]	LTE band 40 TDD 20 MHz BW	–	–26.0	–	dBm
2570–2620 MHz[27]	Band 38	–	–22.0	–	dBm
2545–2575 MHz[28]	XGP Band	–	–24.0	–	dBm
Spurious Emissions					
30 MHz–1 GHz		–	–95.0	–62.0	dBm
1–12.75 GHz		–	–70.0	–47.0	dBm
851–894 MHz		–	–147.0	–	dBm/Hz
925–960 MHz		–	–147.0	–	dBm/Hz
1805–1880 MHz		–	–147.0	–	dBm/Hz
1930–1990 MHz		–	–147.0	–	dBm/Hz
2110–2170 MHz		–	–147.0	–	dBm/Hz

Notes
23. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
24. Bluetooth reference level for the wanted signal at the Bluetooth Chip port = -90.5dBm for 1Mbps, -92.5dBm for 2Mbps.
25. Interferer: 2560 MHz, BW=10 MHz; measured at 2480 MHz.
26. Interferer: 2360 MHz, BW=10 MHz; measured at 2402 MHz.
27. Interferer: 2380 MHz, BW=10 MHz; measured at 2480 MHz.
28. Interferer: 2355 MHz, BW=10 MHz; measured at 2480 MHz.
29. Bluetooth reference level for the wanted signal at the Bluetooth chip port = -86.5dBm for 3Mbps.

Table 30 provides the Bluetooth transmitter RF specifications.

Table 30. Bluetooth Transmitter RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Note The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	13.0	–	dBm
QPSK TX power at Bluetooth		–	9.5	–	dBm
8PSK TX power at Bluetooth		–	9.5	–	dBm
Power control step		–	4.5	–	dB
Note Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38.0	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31.0	–20.0	dBm
|M – N| ≥ 2.5 MHz[30]		–	–43.0	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[31, 32]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[31, 33, 34]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor[35]					
65–108 MHz	FM RX	–	–177	–	dBm/Hz
776–794 MHz	CDMA2000	–	–177	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–177	–	dBm/Hz
925–960 MHz	E-GSM	–	–174	–	dBm/Hz
1570–1580 MHz	GPS	–	–164	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–160	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–152	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–145	–	dBm/Hz
2500–2570 MHz	Band 7	–	–135	–	dBm
2300–2400 MHz	Band 40	–	–135	–	dBm
2570–2620 MHz	Band 38	–	–135	–	dBm
2545–2575 MHz	XGP Band	–	–135	–	dBm

Notes
30. The typical number is measured at ± 3 MHz offset.
31. The maximum value represents the value required for Bluetooth qualification as defined in the v4.0 specification.
32. The spurious emissions during Idle mode are the same as specified in Table 30 on page 76.
33. Specified at the Bluetooth Antenna port.
34. Meets this specification using a front–end band–pass filter.
35. Transmitted power in cellular and FM bands at the Bluetooth Antenna port. See Figure 26 on page 71 for location of the port.

Table 31. Local Oscillator Performance

Parameter	Min	Typ	Max	Unit
LO Performance				
Lock time	–	72.0	–	µs
Initial carrier frequency tolerance	–	±25.0	±75.0	kHz
Frequency Drift				
DH1 packet	–	±15.0	±25.0	kHz
DH3 packet	–	±15.0	±40.0	kHz
DH5 packet	–	±15.0	±40.0	kHz
Drift rate	–	±10.0	20.0	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[36]	150	155	165	kHz
10101010 sequence in payload[37]	115	135	–	kHz
Channel spacing	–	1	–	MHz

Notes
36. This pattern represents an average deviation in payload.
37. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 32. Bluetooth LE RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402		2480	MHz
RX sense (dLNA)[38]	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
RX sense (sLNA)[38]	GFSK, 0.1% BER, 1 Mbps	–	–101.5	–	dBm
TX power[39]	–	–	13.0	–	dBm
Mod Char: delta F1 average	–	247.5	250	272.5	kHz
Mod Char: delta F2 Max	–	185	230	–	kHz
Mod Char: ratio	–	0.8	1.00	–	%

Notes
38. Dirty TX is off.
39. The Bluetooth LE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

Table 33. LE2M RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402		2480	MHz
RX sense (dLNA)[40]	GFSK, 0.1% BER, 2 Mbps	–	–94.0	–	dBm
RX sense (sLNA)[40]	GFSK, 0.1% BER, 2 Mbps	–	–98.5	–	dBm
TX power[41]	–	–	13.0	–	dBm
Mod Char: delta F1 average	–	495	500	505	kHz
Mod Char: delta F2 Max	–	370	490	–	kHz
Mod Char: ratio	–	0.8	1.00	–	%

Notes
40. Dirty TX is off.
41. The LE2M TX power is set to the maximum. All LE2M TX specs are characterized at this level..

Table 34. LELR RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
RX sense (dLNA)[42]	GFSK, 0.1% BER, 500 kbps, S2, standard demodulation index, 37 byte payload length	–	–103.5	–	dBm
RX sense (dLNA)[42]	GFSK, 0.1% BER, 500 kbps, S2, stable demodulation index, 37 byte payload length	–	–106.0	–	dBm
RX sense (dLNA)[42]	GFSK, 0.1% BER, 125 kbps, S8, standard demodulation index, 37 byte payload length	–	–108.0	–	dBm
RX sense (dLNA)[42]	GFSK, 0.1% BER,125 kbps, S2, stable demodulation index, 37 byte payload length	–	–108.0	–	dBm
RX sense (sLNA)[42]	GFSK, 0.1% BER, 500 kbps, S2, standard demodulation index, 37 byte payload length	–	–105.5	–	dBm
RX sense (sLNA)[42]	GFSK, 0.1% BER, 500 kbps, S2, stable demodulation index, 37 byte payload length	–	–108	–	dBm
RX sense (sLNA)[42]	GFSK, 0.1% BER, 125 kbps, S8, standard demodulation index, 37 byte payload length	–	–111	–	dBm
RX sense (sLNA)[42]	GFSK, 0.1% BER,125 kbps, S8, stable demodulation index, 37 byte payload length	–	–111	–	dBm
TX power[43]	–	–	13.0	–	dBm
Mod Char: delta F1 average	–	247.5	250.0	252.5	kHz
Mod Char: delta F2 Max	–	185	234	–	kHz

Notes
42. Dirty TX is off.
43. The LELR TX power is set to the maximum. All LELR TX specs are characterized at this level..

15. WLAN RF Specifications

15.1 Introduction

The CYW5459x includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radios.

Unless otherwise stated, limit values apply for the conditions specified in Table 26 on page 68 and Table 27 on page 69. Typical values apply for an ambient temperature +25°C.

Figure 28. 2.4 GHz WLAN Port Locations

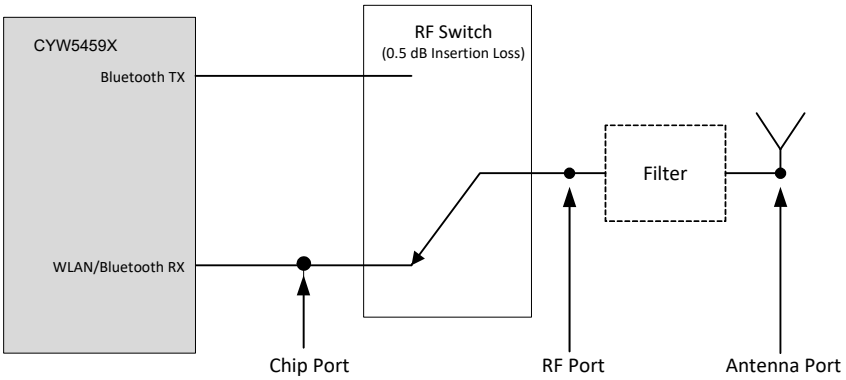
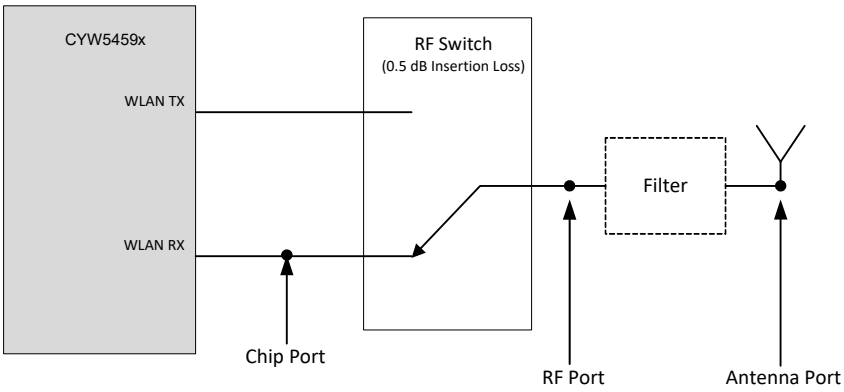


Figure 29. 5 GHz WLAN Port Locations



15.2 2.4 GHz Band General RF Specifications

Table 35. 2.4 GHz Band General RF Specifications

Item	Condition	Min	Typ	Max	Unit
TX/RX switch time	Including TX ramp down	–	–	5.0	µs
RX/TX switch time	Including TX ramp up	–	–	2.0	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

15.3 WLAN 2.4 GHz Receiver Performance Specifications

Note The values in Table 36 are specified at the RF port unless otherwise noted.

Table 36. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min	Typ	Max	Unit
Frequency range	–	2400	–	2500	MHz
Rx sensitivity IEEE 802.11b	1 Mbps DSSS	–96.5	–100.0	–	dBm
	2 Mbps DSSS	–	–97.0	–	dBm
	5.5 Mbps DSSS	–	–95.0	–	dBm
	11 Mbps DSSS	–	–91.5	–	dBm
SISO RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–91.0	–95.5	–	dBm
	9 Mbps OFDM	–	–94.0	–	dBm
	12 Mbps OFDM	–	–93.0	–	dBm
	18 Mbps OFDM	–	–90.5	–	dBm
	24 Mbps OFDM	–	–87.5	–	dBm
	36 Mbps OFDM	–	–84.5	–	dBm
	48 Mbps OFDM	–	–80.0	–	dBm
	54 Mbps OFDM	–75.0	–78.5	–	dBm
SISO RX sensitivity IEEE 802.11n 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: 800ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0	–	–95.5	–	dBm
	MCS1	–	–94.0	–	dBm
	MCS2	–	–91.5	–	dBm
	MCS3	–	–89.0	–	dBm
	MCS4	–	–85.5	–	dBm
	MCS5	–	–81.0	–	dBm
	MCS6	–	–79.5	–	dBm
	MCS7	–74.5	–78.0	–	dBm
MIMO RX sensitivity IEEE 802.11n 2-stream rates 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: 800ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS8	–	–92.5	–	dBm
	MCS9	–	–91.0	–	dBm
	MCS10	–	–88.5	–	dBm
	MCS11	–	–86.0	–	dBm
	MCS12	–	–82.5	–	dBm
	MCS13	–	–78.5	–	dBm
	MCS14	–	–77.0	–	dBm
	MCS15	–72.0	–75.0	–	dBm

Note
44. With external RF matching network.

Table 36. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min	Typ	Max	Unit
SISO RX sensitivity IEEE 802.11ac 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: 800ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–91.0	–95.5	–	dBm
	MCS1, Nss 1	–	–94.0	–	dBm
	MCS2, Nss 1	–	–91.5	–	dBm
	MCS3, Nss 1	–	–89.0	–	dBm
	MCS4, Nss 1	–	–85.5	–	dBm
	MCS5, Nss 1	–	–81.0	–	dBm
	MCS6, Nss 1	–	–79.5	–	dBm
	MCS7, Nss 1	–	–78.0	–	dBm
	MCS8, Nss 1	–69.5	–74.0	–	dBm
MIMO RX sensitivity IEEE 802.11ac 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: 800ns GI, and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 2	–	–92.5	–	dBm
	MCS1, Nss 2	–	–91.0	–	dBm
	MCS2, Nss 2	–	–88.5	–	dBm
	MCS3, Nss 2	–	–86.0	–	dBm
	MCS4, Nss 2	–	–82.5	–	dBm
	MCS5, Nss 2	–	–78.5	–	dBm
	MCS6, Nss 2	–	–76.5	–	dBm
	MCS7, Nss 2	–	–75.5	–	dBm
	MCS8, Nss 2	–68.0	–71.5	–	dBm
Blocking level for 1 dB Rx sensitivity degradation (without external filtering)	776-794 MHz CDMA2000	–	–17.0	–	dBm
	824-849 MHz GSM850	–	–16.9	–	dBm
	880-915 MHz E-GSM	–	–15.6	–	dBm
	1710-1785 MHz GSM1800	–	–18.2	–	dBm
	1850-1910 MHz GSM1900	–	–17.0	–	dBm
	1850-1910 MHz WCDMA	–	–17.0	–	dBm
	1920-1980 MHz WCDMA	–	–17.0	–	dBm
	2500-2570 MHz Band 7	–	–23.2	–	dBm
	2300-2400 MHz Band 40	–	–23.4	–	dBm
	2570-2620 MHz Band 38	–	–22.6	–	dBm
	2545-2575 MHz XGP band	–	–22.4	–	dBm
In-band static CW jammer immunity (fc -8 MHz<fcw<+8 MHz)	RxPER<1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSense + 23 dB<Rxlevel<max input level)	–80.0	–	–	dBm
Input In-Band IP3	Maximum LNA gain	–	–9	–	dBm
	Minimum LNA gain	–	3	–	dBm
Maximum Receive Level @2.4 GHz	1, 2 Mbps (8% PER, 1024 octets)	–	–5.0	–	dBm
	5.5, 11 Mbps (8% PER, 1024 octets)	–	–5.0	–	dBm
	6-54 Mbps (10% PER, 1024 octets)	–	–5.0	–	dBm
	MCS0-7 rates (10% PER, 4095 octets)	–	–5.0	–	dBm
	MCS8, Nss 1 rate (10% PER, 4095 octets)	–	–10.0	–	dBm

Note
44. With external RF matching network.

Table 36. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min	Typ	Max	Unit
LPF 3 dB Bandwidth	–		9.0	–	36.0	MHz
Adjacent channel rejection- DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	Desired and interfering signal 30 MHz apart					
	11 Mbps DSSS	-70 dBm	–	43.4	–	dB
Adjacent channel rejection- OFDM (Difference between interfering and desired signal at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	-79 dBm	–	40.1	–	dB
	54 Mbps OFDM	-62 dBm	–	23.3	–	dB
Adjacent channel rejection MCS0-9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	-79 dBm	–	32.7	–	dB
	MCS7	-61 dBm	–	15.9	–	dB
IEEE 802.11ac Adjacent channel rejection MCS0-8 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	-79 dBm	–	34.3	–	dB
	MCS8	-56 dBm	–	15.3	–	dB
Maximum receiver gain	–		–	66.0	–	dB
Gain control step	–		–	3.0	–	dB
RSSI Accuracy	Range -85 dBm to -26 dBm		–5.0	–	5.0	dB
	Range above -26 dBm		–8.0	–	8.0	dB
Return loss[44]	Zo = 50Ω, across the dynamic range		–	15	–	dB
Receiver cascaded noise figure	At maximum gain		–	3.5	–	dB

Note
44. With external RF matching network.

15.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note The values in Table 37 are specified at the RF port unless otherwise noted.

Table 37. WLAN 2.4 GHz Transmitter Performance Specifications (with Internal Power Amplifier)

Parameter	Condition/Notes		Min	Typ	Max	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (at 18 dBm, 100% duty cycle, 1 Mbps CCK)[45]	76–108 MHz	FM RX	–	–166	–	dBm/Hz
	776–794 MHz	–	–	–160	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–158	–	dBm/Hz
	925–960 MHz	E-GSM	–	–158	–	dBm/Hz
	1570–1580 MHz	GPS	–	–149	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–138	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–133	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–125	–	dBm/Hz
	2500–2570 MHz	Band 7	–	–109	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–88	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–114	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–114	–	dBm/Hz
Harmonic level (at 21 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–25			dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–7			dBm/1 MHz

Notes
45. The cellular standards listed only indicate the typical usages of that band in some countries: other standards may also be used within those bands.
46. Typical numbers indicate average results of 1.5 sigma parts with VBAT = 3.3V at 25 °C. Min numbers indicate worst results of 1.5 sigma parts with VBAT = 3.3V at 25 °C.

Table 37. WLAN 2.4 GHz Transmitter Performance Specifications (with Internal Power Amplifier) (Cont.)

Parameter	Condition/Notes		Min	Typ	Max	Unit
EVM Does Not Exceed						
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance	802.11b (DSSS/CCK)	–9 dB	19.5	22.5	–	dBm
	OFDM, BPSK	–8 dB	18.5	21.5	–	dBm
	OFDM, QPSK	–13 dB	18.5	21.5	–	dBm
	OFDM, 16-QAM	–19 dB	18.5	21.5	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	18.5	21.5	–	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	18	21	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	17	20	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees
TX power control dynamic range	–		10.0	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies across 10 dBm to 20 dBm output power range		–	±1.5	–	dB
Carrier suppression	–		15.0	–	–	dBc
Gain control step	–		–	0.25	–	dB

Notes
45. The cellular standards listed only indicate the typical usages of that band in some countries: other standards may also be used within those bands.
46. Typical numbers indicate average results of 1.5 sigma parts with VBAT = 3.3V at 25 °C. Min numbers indicate worst results of 1.5 sigma parts with VBAT = 3.3V at 25 °C.

15.5 WLAN 5 GHz Receiver Performance Specifications

Note The values in Table 38 are specified at the RF port unless otherwise noted.

Table 38. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Min	Typ	Max	Unit
Frequency range	–	4900	–	5845	MHz
SISO RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–91.5	–94.5	–	dBm
	9 Mbps OFDM	–	–93.5	–	dBm
	12 Mbps OFDM	–	–92.5	–	dBm
	18 Mbps OFDM	–	–90.0	–	dBm
	24 Mbps OFDM	–	–87.0	–	dBm
	36 Mbps OFDM	–	–83.5	–	dBm
	48 Mbps OFDM	–	–79.5	–	dBm
	54 Mbps OFDM	–75.0	–78.0	–	dBm

Notes
47. The minimum and maximum values shown have a 95% confidence level.
48. Measured with some external matching components.

Table 38. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min	Typ	Max	Unit
SISO RX sensitivity IEEE 802.11n 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94.5	–	dBm
	MCS1	–	–93.5	–	dBm
	MCS2	–	–91.0	–	dBm
	MCS3	–	–88.5	–	dBm
	MCS4	–	–85.0	–	dBm
	MCS5	–	–80.5	–	dBm
	MCS6	–	–79.0	–	dBm
	MCS7	–74.5	–77.5	–	dBm
MIMO RX sensitivity IEEE 802.11n 2-stream rates 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port.	20 MHz channel spacing for all MCS rates				
	MCS8	–	–92.5	–	dBm
	MCS9	–	–90.5	–	dBm
	MCS10	–	–88.0	–	dBm
	MCS11	–	–85.5	–	dBm
	MCS12	–	–82.0	–	dBm
	MCS13	–	–78.5	–	dBm
	MCS14	–	–76.5	–	dBm
	MCS15	–71.5	–74.5	–	dBm
SISO RX sensitivity IEEE 802.11n 40 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	40 MHz channel spacing for all MCS rates				
	MCS0	–89.0	–92.0	–	dBm
	MCS1	–	–91.0	–	dBm
	MCS2	–	–88.5	–	dBm
	MCS3	–	–86.0	–	dBm
	MCS4	–	–82.5	–	dBm
	MCS5	–	–78.0	–	dBm
	MCS6	–	–77.0	–	dBm
	MCS7	–72.0	–75.0	–	dBm
MIMO RX sensitivity IEEE 802.11n 2-stream rates 40 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	40 MHz channel spacing for all MCS rates				
	MCS8	–	–90.0	–	dBm
	MCS9	–	–88.0	–	dBm
	MCS10	–	–85.5	–	dBm
	MCS11	–	–83.0	–	dBm
	MCS12	–	–79.5	–	dBm
	MCS13	–	–75.5	–	dBm
	MCS14	–	–74.0	–	dBm
	MCS15	–68.5	–71.5	–	dBm

Notes
47. The minimum and maximum values shown have a 95% confidence level.
48. Measured with some external matching components.

Table 38. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min	Typ	Max	Unit
SISO RX sensitivity IEEE 802.11ac 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–95.0	–	dBm
	MCS1, Nss 1	–	–93.5	–	dBm
	MCS2, Nss 1	–	–91.0	–	dBm
	MCS3, Nss 1	–	–88.5	–	dBm
	MCS4, Nss 1	–	–85.0	–	dBm
	MCS5, Nss 1	–	–80.5	–	dBm
	MCS6, Nss 1	–	–79.0	–	dBm
	MCS7, Nss 1	–	–77.5	–	dBm
	MCS8, Nss 1	–70.5	–73.5	–	dBm
MIMO RX sensitivity IEEE 802.11ac 20 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	20 MHz channel spacing for all MCS rates				
	MCS0, Nss 2	–	–92.5	–	dBm
	MCS1, Nss 2	–	–90.5	–	dBm
	MCS2, Nss 2	–	–88.0	–	dBm
	MCS3, Nss 2	–	–85.5	–	dBm
	MCS4, Nss 2	–	–82.0	–	dBm
	MCS5, Nss 2	–	–78.0	–	dBm
	MCS6, Nss 2	–	–76.5	–	dBm
	MCS7, Nss 2	–	–75.0	–	dBm
	MCS8, Nss 2	–67.5	–70.5	–	dBm
SISO RX sensitivity IEEE 802.11ac 40 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	40 MHz channel spacing for all MCS rates				
	MCS0, Nss 1	–	–92.5	–	dBm
	MCS1, Nss 1	–	–91.0	–	dBm
	MCS2, Nss 1	–	–88.5	–	dBm
	MCS3, Nss 1	–	–85.5	–	dBm
	MCS4, Nss 1	–	–82.0	–	dBm
	MCS5, Nss 1	–	–78.0	–	dBm
	MCS6, Nss 1	–	–76.5	–	dBm
	MCS7, Nss 1	–	–74.5	–	dBm
	MCS8, Nss 1	–	–71.0	–	dBm
	MCS9, Nss 1	–66.0	–69.0	–	dBm

Notes
47. The minimum and maximum values shown have a 95% confidence level.
48. Measured with some external matching components.

Table 38. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min	Typ	Max	Unit
MIMO RX sensitivity IEEE 802.11ac 40 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	40 MHz channel spacing for all MCS rates					
	MCS0, Nss 2		–	–90.0	–	dBm
	MCS1, Nss 2		–	–88.0	–	dBm
	MCS2, Nss 2		–	–85.5	–	dBm
	MCS3, Nss 2		–	–83.0	–	dBm
	MCS4, Nss 2		–	–79.0	–	dBm
	MCS5, Nss 2		–	–75.0	–	dBm
	MCS6, Nss 2		–	–73.5	–	dBm
	MCS7, Nss 2		–	–72.0	–	dBm
	MCS8, Nss 2		–	–68.5	–	dBm
	MCS9, Nss 2		–63.0	–66.0	–	dBm
SISO RX sensitivity IEEE 802.11ac 80 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	80 MHz channel spacing for all MCS rates					
	MCS0, Nss 1		–	–90.0	–	dBm
	MCS1, Nss 1		–	–88.0	–	dBm
	MCS2, Nss 1		–	–85.0	–	dBm
	MCS3, Nss 1		–	–82.5	–	dBm
	MCS4, Nss 1		–	–79.0	–	dBm
	MCS5, Nss 1		–	–75.0	–	dBm
	MCS6, Nss 1		–	–73.5	–	dBm
	MCS7, Nss 1		–	–71.5	–	dBm
	MCS8, Nss 1		–65.0	–68.0	–	dBm
	MCS9, Nss 1		–63.0	–66.0	–	dBm
MIMO RX sensitivity IEEE 802.11ac 80 MHz channel spacing (10% PER for 4096 octet PSDU) at WLAN RF port	80 MHz channel spacing for all MCS rates					
	MCS0, Nss 2		–	–87.0	–	dBm
	MCS1, Nss 2		–	–85.0	–	dBm
	MCS2, Nss 2		–	–82.0	–	dBm
	MCS3, Nss 2		–	–79.5	–	dBm
	MCS4, Nss 2		–	–76.0	–	dBm
	MCS5, Nss 2		–	–71.5	–	dBm
	MCS6, Nss 2		–	–70.0	–	dBm
	MCS7, Nss 2		–	–68.5	–	dBm
	MCS8, Nss 2		–	–64.5	–	dBm
	MCS9, Nss 2		–59.5	–62.5	–	dBm
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	-79 dBm	–	24.8	–	dB
	54 Mbps OFDM	-62 dBm		12.1	–	dB
Adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0 OFDM	-76 dBm	–	23.7	–	dB
	MCS7 OFDM	-58 dBm	–	10	–	dB

Notes
47. The minimum and maximum values shown have a 95% confidence level.
48. Measured with some external matching components.

Table 38. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min	Typ	Max	Unit
Adjacent channel rejection (Difference between interfering and desired signal (80 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0 OFDM	-73 dBm	–	31.7	–	dB
	MCS9 OFDM	-48 dBm	–	4.8	–	dB
Maximum receiver gain	–		–	66.0	–	dB
Gain control step	–		–	3.0	–	dB
RSSI accuracy[47]	Range –85 dBm to –26 dBm		–5.0	–	5.0	dB
	Range above –26 dBm		–8.0	–	8.0	dB
Return loss[48]	Zo = 50Ω, across the dynamic range		–	13	–	dB
Receiver cascaded noise figure	At maximum gain		–	4.2	–	dB
Input In-Band IP3	Maximum LNA gain		–	–8.0	–	dBm
	Minimum LNA gain		–	6.0	–	dBm
Maximum receive level @ 5.24 GHz	6, 9, 12 Mbps		–9.5	–5.0	–	dBm
	18, 24, 36, 48, 54 Mbps		–14.5	–5.0	–	dBm
LPF 3 dB bandwidth			–5.0	–	–	MHz

Notes
47. The minimum and maximum values shown have a 95% confidence level.
48. Measured with some external matching components.

15.6 WLAN 5 GHz Transmitter Performance Specifications

Note The values in Table 39 are specified at the RF port unless otherwise noted.

Table 39. WLAN 5 GHz Transmitter Performance Specifications (With Internal Power Amplifier)

Parameter	Condition/Notes		Min	Typ	Max	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (at 18 dBm)[49]	76–108 MHz	FM RX	–	–168	–	dBm/Hz
	776–794 MHz	–	–	–168	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–168	–	dBm/Hz
	925–960 MHz	E-GSM	–	–168	–	dBm/Hz
	1570–1580 MHz	GPS	–	–168	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–167	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–164	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–164	–	dBm/Hz
	2400–2483 MHz	Bluetooth/WLAN	–	–161	–	dBm/Hz
	2500–2570 MHz	Band 7	–	–161	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–162	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–157	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–161	–	dBm/Hz
Harmonic level (at 19 dBm)	9.8–11.570 GHz	2nd harmonic	–	–9	–	dBm/MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance	OFDM, QPSK	–13 dB	16	19	–	dBm
	OFDM, 16-QAM	–19 dB	16	19	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	16	19	–	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	16	19	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT80)	–30 dB	14	17	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT80)	–32 dB	13	16	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
TX power control dynamic range	–		10.0	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.		–	±1.5		dB
Carrier suppression	–		15.0	–	–	dBc
Gain control step	–		–	0.25	–	dB

Notes
49. The cellular standards listed only indicate the typical usages of that band in some countries: other standards may also be used within those bands.
50. Typical numbers indicate average results of 1.5 sigma parts with VBAT = 3.3V at 25 °C. Min numbers indicate worst results of 1.5 sigma parts with VBAT = 3.3V at 25 °C.

15.7 General Spurious Emissions Specifications

Table 40. General Spurious Emissions Specifications

Parameter	Condition/Notes		Min	Typ	Max	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–85.0	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–31.0	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–81.0	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–86.0	–	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–100.0	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–60.0	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–87.0	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–87.0	–	dBm

16. Internal Regulator Electrical Specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

16.1 Core Buck Switching Regulator

Table 41. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Unit
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	4.8[51]	V
PWM mode switching frequency	CCM, Load > 100 mA VBAT = 3.6 V	2.8	4.0	5.2	MHz
PWM output current	–	–	–	600	mA
Output current limit	–	–	1400		mA
Output voltage range	Programmable, 30 mV steps, Default = 1.35 V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4.0	% ±2 with trim
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max Ripple based on VBAT = 3.6 V, V_{out} = 1.35 V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL< 200 pH	–	7.0	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load	78.0	86.0	–	%
PFM mode efficiency	10 mA load current	–	80.0	–	%
Start-up time from power down	V_{IO} already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2 V	–	–	500	µs
External inductor	0806 size, ± 30%, 0.11 ± 25% Ω	0.67[52]	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V	2.0[53]	4.7	10.0[54]	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 10V, 4.7 µF	0.67[53]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3 V	40.0	–	–	µs

Notes

51. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
52. Effective inductance under current-bias and part-to-part tolerance.
53. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
54. Total capacitance includes those connected at the far end of the active load.

16.2 3.3V LDO (PALDO3P3)

Table 42. PALDO3P3 Specifications

Specification	Notes	Min	Typ	Max	Unit
Input supply voltage, V_{in}	Min = V_o + 0.2 V = 3.1 V (for V_o = 2.9 V) dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[55]	V
Output current	–	0.2	–	650	mA
Nominal output voltage, V_o	Default = 3.3 V	–	3.3	–	V
Dropout voltage	At max load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5.0	–	+5.0	%
Quiescent current	No load	–	100	120	µA
	Maximum load (600 mA)	–	5.8	6.0	mA
Leakage current	Power-Down mode, junction temperature = 85°C	–	1.5	5.0	µA
Line regulation	V_{in} from (V_o + 0.2 V) to 4.8 V, max load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2 V, V_o = 3.3V, C_o = 4.7 µF, Max load, 100 Hz to 100 kHz	20.0	–	–	dB
LDO turn-on time	C_o = 4.7 µF (plus other board capacitor max 4.7 µF)	–	160	210	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[56]	4.7	–	µF
External input capacitor	For SR_VDDBATA5V pin (shared with band gap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10 V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

Notes
55. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
56. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.3 3.3V LDO (LDO3P3)

Table 43. LDO3P3 Specifications

Specification	Notes	Min	Typ	Max	Unit
Input supply voltage, V_{in}	Min = V_o + 0.2 V = 3.1 V (for V_o = 2.9 V) Dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[57]	V
Output current	–	0.1	–	200	mA
Nominal output voltage, V_o	Default = 3.3 V	–	3.3	–	V
Dropout voltage	At max load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5.0	–	+5.0	%
Quiescent current	No load	–	35.0	40	µA
	Maximum load	–	1.94	1.97	mA
Leakage current	Power-Down mode, junction temperature = 85°C	–	1.5	5.0	µA
Line regulation	V_{in} from (V_o + 0.2 V) to 4.8 V, max load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2 V, V_o = 3.3V, C_o = 4.7 µF, Max load, 100 Hz to 100 kHz	20.0	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10 V	0.7[58]	2.2	–	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402	–	4.7	–	µF

Notes

57. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
58. Minimum capacitor value refers to the residual capacitor value after taking into account the part–to–part tolerance, DC–bias, temperature, and aging.

16.4 2.5V LDO (BTLDO2P5)

Table 44. BTLDO2P5 Specifications

Specification	Notes	Min	Typ	Max	Unit
Input supply voltage	Min = 2.8 V + 0.3 V = 3.1 V (for V_o = 2.8 V) Dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8[59]	V
Nominal output voltage	Default = 2.5 V.	–	2.5	–	V
Output voltage programmability	Range	2.2	2.5	2.8	V
	Accuracy at any step (including line/load regulation), load > 0.1 mA.	–5	–	5.0	%
Dropout voltage	At maximum load.	–	–	300	mV
Output current	–	0.1	–	70.0	mA
Quiescent current	No load.	–	8	16.0	µA
	Maximum load at 70 mA.	–	660	700	µA
Leakage current	Power-down mode.	–	1.5	5.0	µA
Line regulation	V_{in} from (V_o + 0.3 V) to 4.8 V, maximum load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, V_{in} = 3.6 V.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.3 V, V_o = 2.5 V, C_o = 2.2 µF, maximum load, 100 Hz to 100 kHz.	20.0	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	150	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5–240 mΩ), ±10%, 10V	0.7[60]	2.2	2.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with band gap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10 V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	–	4.7	–	µF

Notes
59. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
60. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

16.5 CLDO

Table 45. CLDO Specifications

Specification	Notes	Min	Typ	Max	Unit
Input supply voltage, V_{in}	Min = 1.2 + 0.15 V = 1.35 V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.3	–	420	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2 V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4.0	–	+4.0	% ±2 with trim
Quiescent current	No load	–	36.0	51.0	µA
	420 mA load	–	2.65	2.71	mA
Line Regulation	V_{in} from (V_o + 0.15 V) to 1.5 V, maximum load	–	–	5.0	mV/V
Load Regulation	Load from 1 mA to 420 mA	–	0.025	0.045	mV/mA
Leakage Current	Power down	–	–	20	µA
	Bypass mode	–	1.0	3	µA
PSRR	@1 kHz, V_{in} ≥ 1.35 V, C_o = 4.7 µF	20.0	–		dB
Start-up Time of PMU	V_{IO} up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2 V.	–	–	700	µs
LDO Turn-on Time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	2.2[61]	4.7	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1.0	2.2	µF

Note
61. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC–bias, temperature, and aging.

16.6 LNLDO

Table 46. LNLDO Specifications

Specification	Notes	Min	Typ	Max	Unit
Input supply voltage, Vin	Min = 1.2 V_o + 0.15 V = 1.35 V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2 V.	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4.0	–	+4.0	% ±2 with trim
Quiescent current	No load	–	44.0	–	µA
	Max load	–	970	990	µA
Line regulation	V_{in} from (V_o + 0.1 V) to 1.5 V, max load	–	–	5.5	mV/V
Load regulation	Load from 1 mA to 150 mA	–	0.025	0.045	mV/mA
Leakage current	Power-down	–	–	10.0	µA
Output noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60.0 35.0	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35 V, C_o= 2.2 µF, V_o = 1.2 V	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	140	180	µs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[62]	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1.0	2.2	µF

Note
62. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC–bias, temperature, and aging.

16.7 HLDO

Table 47. HLDO Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, V_{in}	Min V_{in} = V_o + 0.15 V = 1.35 V (for V_o = 1.2 V) dropout voltage requirement must be met under max load.	1.3	1.35	1.5	V
Output current	Peak load = 80 mA, average = 35 mA	0.1		100	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2 V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4.0	–	+4.0	% ±2 with trim
Quiescent current	No load. 100 mA load	–	11.0 633	13.0 650	µA µA
Line regulation	V_{in} from (V_o + 0.15 V) to 1.5 V; 100 mA load	–	–	5.0	mV/V
Load regulation	load from 1 mA to 100 mA; V_{in} ≥ (V_o + 0.15 V)	–	0.025	0.045	mV/mA
Leakage current	Power-down mode Bypass mode	–	5.0 0.2	20.0 1.5	µA µA
PSRR	At 1 kHz, V_{in} ≥ 1.35V, C_o= 1 µF	20.0	–	–	dB
Start-up time of PMU	V_{IO} up and steady. Time from REG_ON rise edge to CLDO reaching 99% of V_o.	–	530	700	µs
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	0201 size capacitor 6.3 V.	0.5[63]	1.0	–	µF
External input capacitor	Only use an external input capacitor at VDD_LDO pin if it is not supplied from CBUCK output.	–	1.0	–	µF

Note
63. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.8 MEMLPLDO

Table 48. MEMLPLDO Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, V_{in}	Taken from VDDIO input	1.6	1.8	1.98	V
Nominal output voltage, V_o	Default = 0.9 V	0.825	0.9	1.237	V
Output voltage DC accuracy	Including line/load regulation.	–5.0	–	+5.0	%
Output current	–	0	–	10.0	mA
Quiescent current	No load includes LP-B Gap. Excludes other PMU peripherals.	–	3.0	–	µA
Leakage current	Power-down mode. At junction temperature 85°C.	–	–	1	µA
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	18.0	40.0	µs
External output capacitor, C_o	–	–	0.47	–	µF
External input capacitor	VDDIO input pin capacitor	0.06	0.22	0.47	µF

17. System Power Consumption

17.1 WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 49.

All values in Table 49 are with the Bluetooth core in reset (that is Bluetooth is OFF).

Table 49. Typical WLAN Power Consumption

Mode	Bandwidth (MHz)	Band (GHz)	V_{bat} = 3.3V mA	V_{io} = 1.8V µA[64]
Sleep Modes				
OFF[65]	–	–	–	243
Sleep[66]	–	–	–	–
IEEE power save, DTIM 1 1 RX core[67]	20.0	2.4	2.7	208
IEEE power save, DTIM 3 1 RX core[67]	20.0	2.4	0.9	239
IEEE power save, DTIM 1 1 RX core[67]	20.0	5.0	2.2	214
IEEE power save, DTIM 3 1 RX core[67]	20.0	5.0	0.8	224
IEEE power save, DTIM 1 1 RX core[67]	40.0	5.0	2.6	214
IEEE power save, DTIM 3 1 RX core[67]	40.0	5.0	1.0	252
IEEE power save, DTIM 1 1 RX core[67]	80.0	5.0	3.2	216
IEEE power save, DTIM 3 1 RX core[67]	80.0	5.0	1.2	236
Active Modes				
Transmit				
CCK 1 chain[68]	20.0	2.4	370	23
MCS7, SGI[69, 70, 71]	20.0	2.4	311	23
MCS15, SGI[69, 70, 71]	20.0	5.0	564	23
6 Mbps	20.0	5.0	360	23
MCS8, Nss 1, HT20	20.0	5.0	333	23
MCS7[69, 70, 72]	40.0	5.0	364	23
MCS9, Nss 1, SGI[69, 70, 73]	40.0	5.0	351	23
MCS9, Nss 2, SGI[69, 70, 73]	40.0	5.0	673	23
MCS9, Nss 1, SGI[69, 70, 73]	80.0	5.0	391	23
MCS9, Nss 2, SGI[69, 70, 73]	80.0	5.0	755	23
Receive				
1 Mbps, 1 RX core	20.0	2.4	86	23
MCS7, HT20 1 RX core[74]	20.0	2.4	91	23
MCS15, HT20[74]	20.0	2.4	125	23
CRS 1 RX core[72]	20.0	2.4	85	23
6 Mbps	20.0	5.0	85	23

Notes

64. Specified with all pins idle (not switching) and not driving any loads.
65. Both WL_REG and BT_REG_ON are low.
66. Idle, not associated, or inter-beacon.
67. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over three DTIM intervals.
68. Output power per core at RF port = 21 dBm.
69. Duty cycle is 100%.
70. Measured using Packet engine test mode.
71. Output power per core at RF port = 17 dBm.
72. Output power per core at RF port = 17.5 dBm.
73. Output power per core at RF port = 14 dBm.
74. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
75. Carrier sense (CCA) when no carrier is present.

Table 49. Typical WLAN Power Consumption (Cont.)

Mode	Bandwidth (MHz)	Band (GHz)	V_{bat} = 3.3V mA	V_{io} = 1.8V µA[64]
Receive MCS7, SGI 1 RX core[74]	20.0	5.0	87	23
Receiver MCS15, SGI[74]	20.0	5.0	148	23
CRS 1 RX core[72]	20.0	5.0	80	23
Receive MCS 7, SGI 1 RX core[74]	40.0	5.0	110	23
Receive MCS 15, SGI[74]	40.0	5.0	202	23
CRS 1 RX core[72]	40.0	5.0	98	23
Receive MCS9, Nss 1, SGI[74]	80.0	5.0	161	23
Receive MCS9, Nss 2, SGI[74]	80.0	5.0	286	23
CRS 1 RX core	80.0	5.0	137	23

Notes
64. Specified with all pins idle (not switching) and not driving any loads.
65. Both WL_REG and BT_REG_ON are low.
66. Idle, not associated, or inter-beacon.
67. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over three DTIM intervals.
68. Output power per core at RF port = 21 dBm.
69. Duty cycle is 100%.
70. Measured using Packet engine test mode.
71. Output power per core at RF port = 17 dBm.
72. Output power per core at RF port = 17.5 dBm.
73. Output power per core at RF port = 14 dBm.
74. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
75. Carrier sense (CCA) when no carrier is present.

17.2 Bluetooth Current Consumption

The Bluetooth and Bluetooth LE current consumption measurements are shown in Table 50.

Notes

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in Table 50.
- The Bluetooth current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 50. Bluetooth and Bluetooth LE Current Consumption

Operating Mode	VBAT (3.3V) Typical	VDDIO (1.8V) Typical	Unit
Sleep	5.0	158	µA
Standard 1.28s inquiry scan	137.0	164	µA
500 ms sniff master	86	181	µA
3-DH5 TXRX master	17	0.119	mA
3-DH5 TXRX slave	16.5	0.119	mA
SCO HV3 master	8.7	0.024	mA
Bluetooth LE scan	151.0	182.0	µA
Bluetooth LE adv. unconnectable 1 sec	48	183	µA
Bluetooth LE connected 1 sec	50	165.0	µA

18. Interface Timing and AC Characteristics

18.1 SDIO Timing

18.1.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 30 and Table 51.

Figure 30. SDIO Bus Timing (Default Mode)

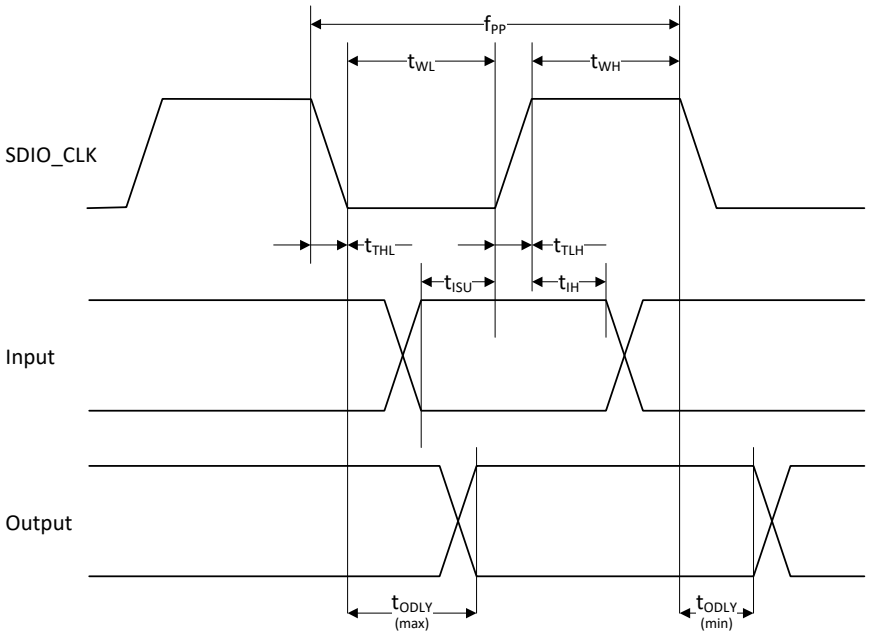


Table 51. SDIO Bus Timing[76] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[77])					
Frequency – Data Transfer mode	f_{PP}	0	–	25.0	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10.0	–	–	ns
Clock high time	t_{WH}	10.0	–	–	ns
Clock rise time	t_{TLH}	–	–	10.0	ns
Clock low time	t_{THL}	–	–	10.0	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5.0	–	–	ns
Input hold time	t_{IH}	5.0	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14.0	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50.0	ns

Note
76. Timing is based on CL ≤ 40 pF load on CMD and Data.
77. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

18.1.2 SDIO High-Speed (HS) Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 31 and Table 52.

Figure 31. SDIO Bus Timing (HS Mode)

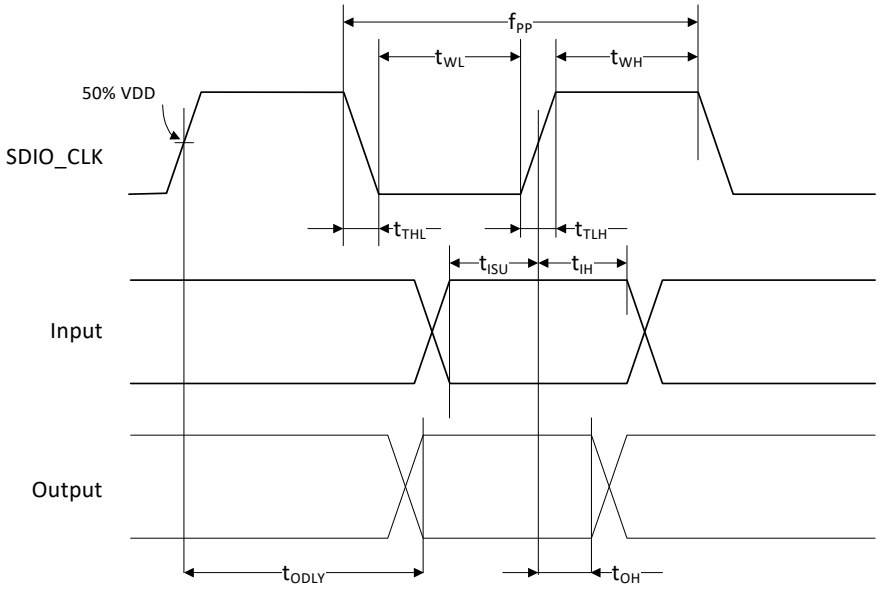


Table 52. SDIO Bus Timing[78] Parameters (HS Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[79])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7.0	–	–	ns
Clock high time	t_{WH}	7.0	–	–	ns
Clock rise time	t_{TLH}	–	–	3.0	ns
Clock low time	t_{THL}	–	–	3.0	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6.0	–	–	ns
Input hold Time	t_{IH}	2.0	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14.0	ns
Output hold time	t_{OH}	2.5.0	–	–	ns
Total system capacitance (each line)	CL	–	–	40.0	pF

Note
78. Timing is based on CL ≤ 40 pF load on CMD and Data.
79. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

18.1.3 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 32. SDIO Clock Timing (SDR Modes)

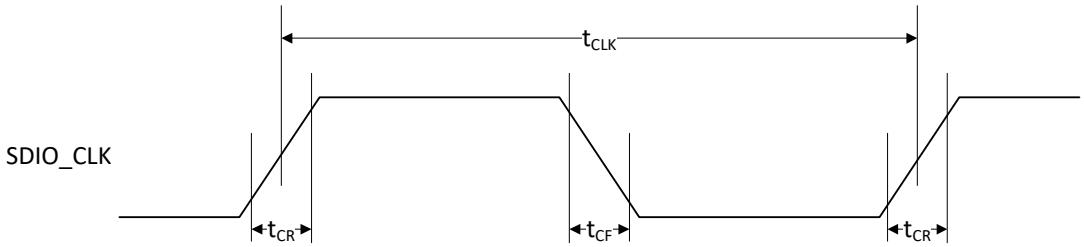


Table 53. SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40.0	–	ns	SDR12 mode
		20.0	–	ns	SDR25 mode
		10.0	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30.0	70.0	%	–

Device Input Timing

Figure 33. SDIO Bus Input Timing (SDR Modes)

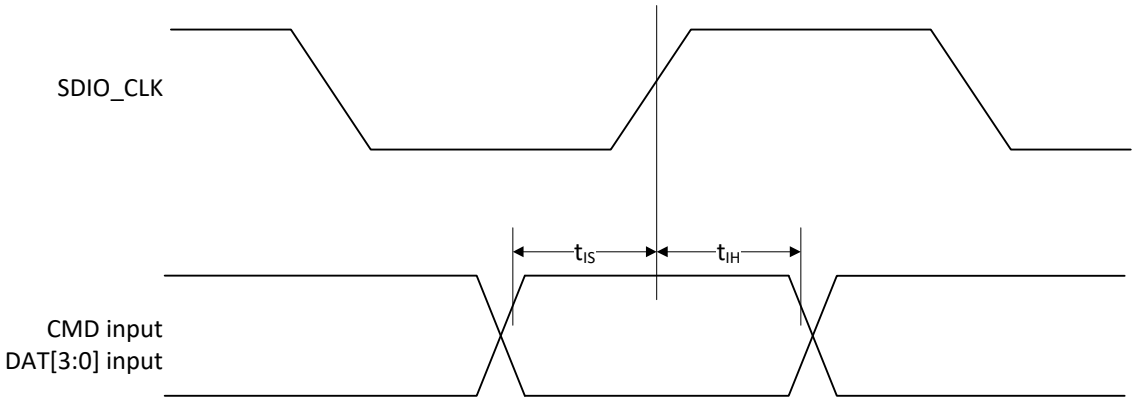


Table 54. SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975 V

Device Output Timing

Figure 34. SDIO Bus Output Timing (SDR Modes up to 100 MHz)

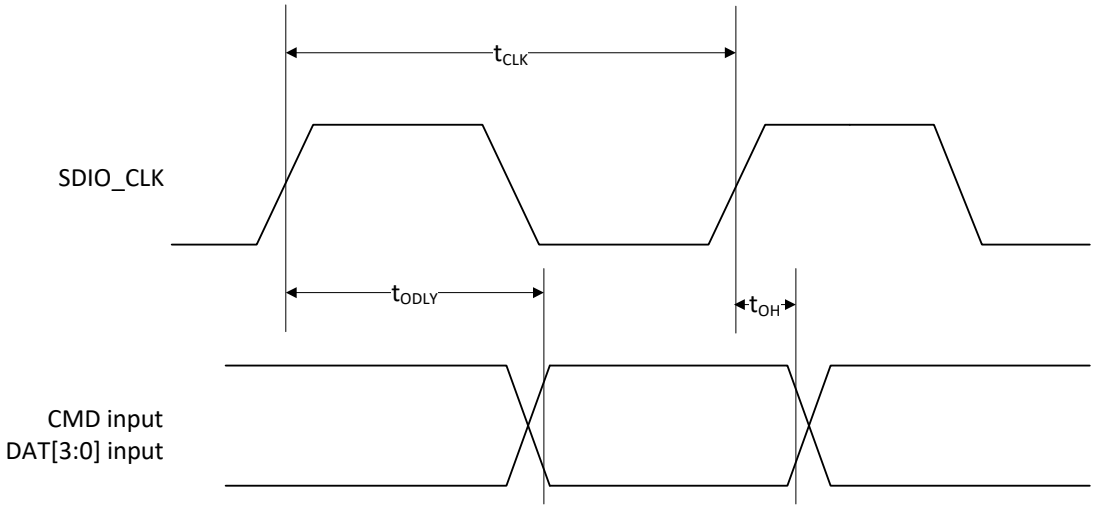


Table 55. SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L = 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L = 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L = 15 pF

Figure 35. SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

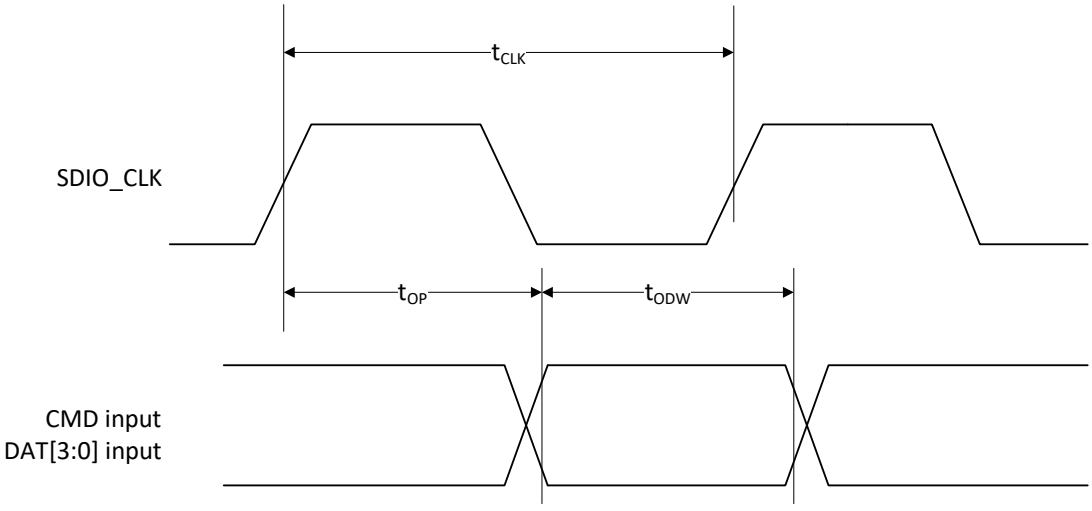
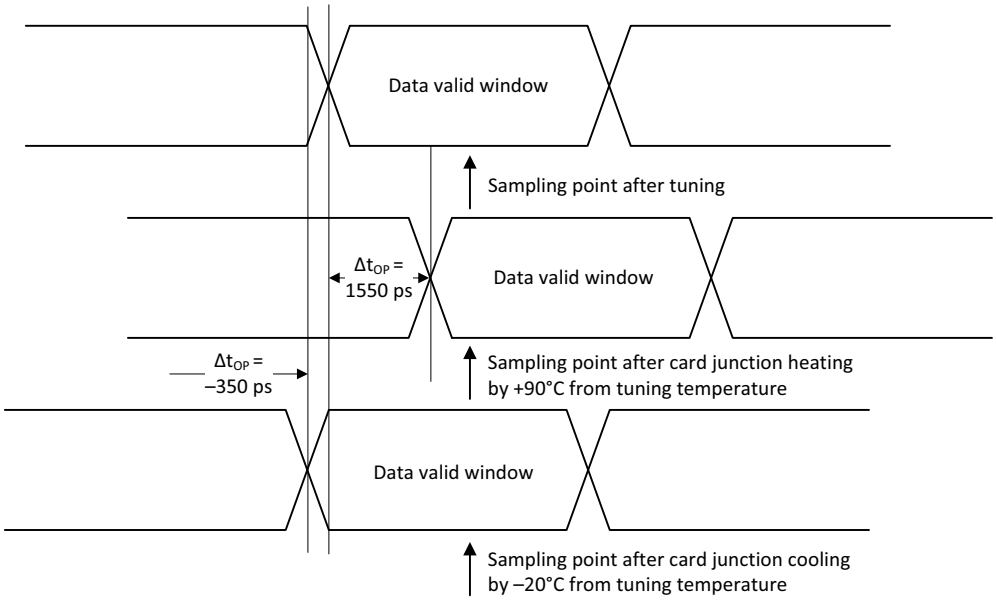


Table 56. SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2.0	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

Figure 36. Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



18.1.4 SDIO Bus Timing Specifications in DDR50 Mode

Figure 37. SDIO Clock Timing (DDR50 Mode)

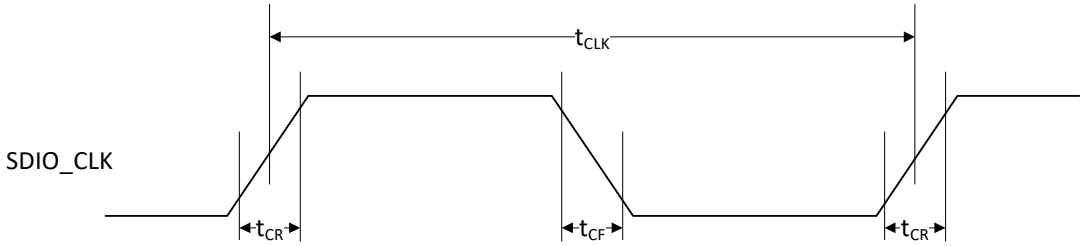


Table 57. SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20.0	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45.0	55.0	%	–

Data Timing, DDR50 Mode

Figure 38. SDIO Data Timing (DDR50 Mode)

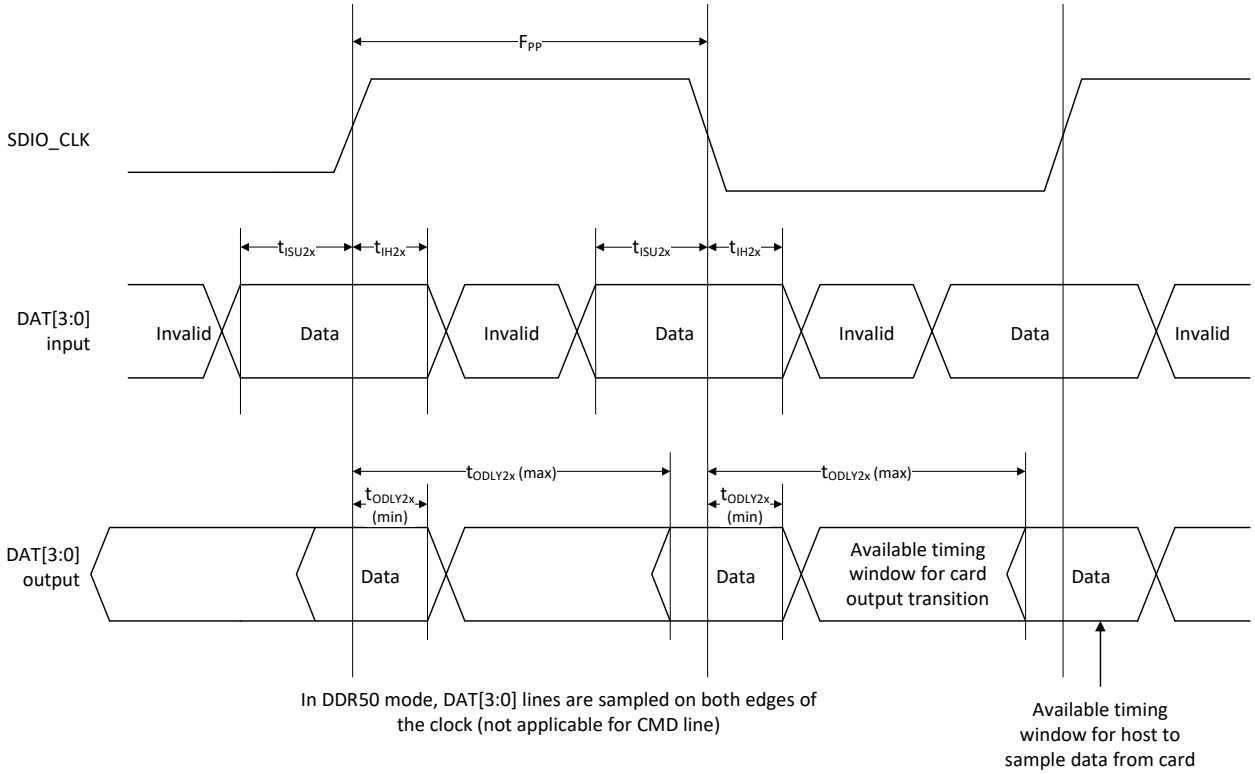


Table 58. SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6.0	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3.0	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15pF (1 Card)

18.2 PCI Express Interface Parameters

Table 59. PCI Express Interface Parameters

Parameter	Symbol	Comments	Min	Typ	Max	Unit
General						
Baud rate	BPS	–	–	2.5	–	Gbaud
Reference clock peak-to-peak differential amplitude[80]	V_{IH}[82]	Differential Input High Voltage	150	–	–	mV
	V_{IL}[82]	Differential Input Low Voltage	–	–	–150	mV
	V_{cross}[83, 84, 85]	Absolute crossing point Voltage	250	–	550	mV
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80.0	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40.0	50.0	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10.0	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10.0	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65.0	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, program-mable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV

Table 59. PCI Express Interface Parameters (Cont.)

Parameter	Symbol	Comments	Min	Typ	Max	Unit
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20.0	mV
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	–	25.0	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20.0	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90.0	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80.0	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6.0	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

Note
80. The reference clock inputs comply with the requirements of PCI Express CEM v2.0.
81. Measurements taken from differential waveform.
82. Measurements taken from single ended waveform.
83. Measurements at crossing point where the instantaneous voltage value of the rising edge REFCLK+ equals the falling edge of REFCLK-.
84. Refers to the total variations from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for the requirements.

18.3 JTAG Timing

Table 60. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

19. Power-Up Sequence and Timing

19.1 Sequencing of Reset and Regulator Control Signals

The CYW5459x has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 39, Figure 40 on page 111, Figure 41 on page 111, and Figure 42 on page 111). The timing values indicated are minimum required values; longer delays are also acceptable.

19.1.1 Description of Control Signals

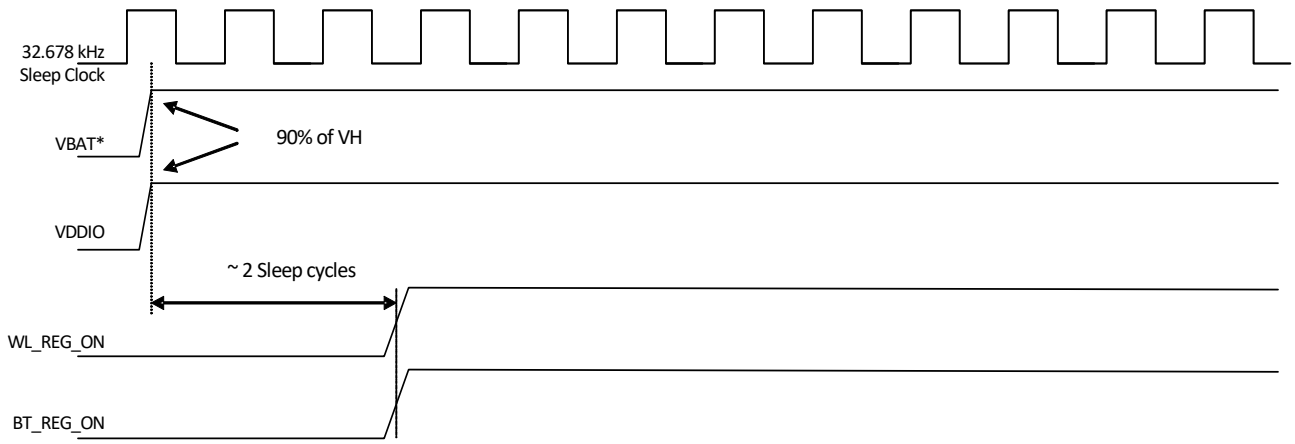
- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW5459x regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW5459x regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Notes

- The CYW5459x has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO and PCIe access.
- VBAT, VDDIO, WPT_1P8, and WPT_3P3 should not rise 10%–90% faster than 40 microseconds.

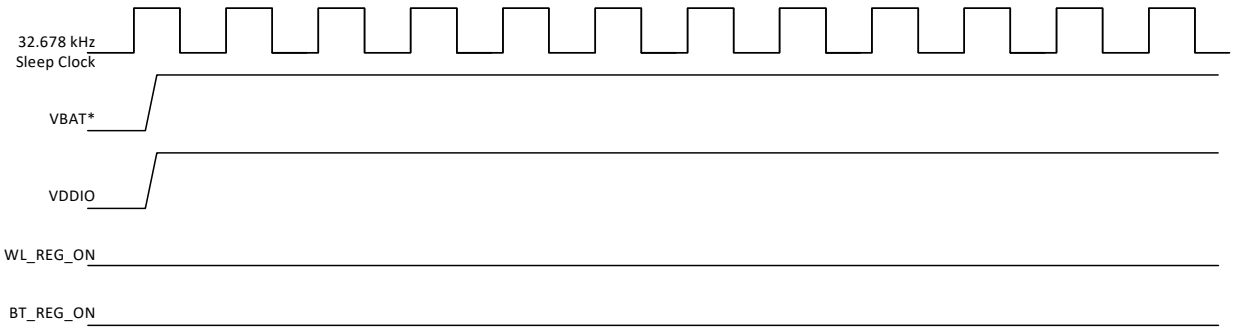
19.1.2 Control Signal Timing Diagrams

Figure 39. WLAN = ON, Bluetooth = ON



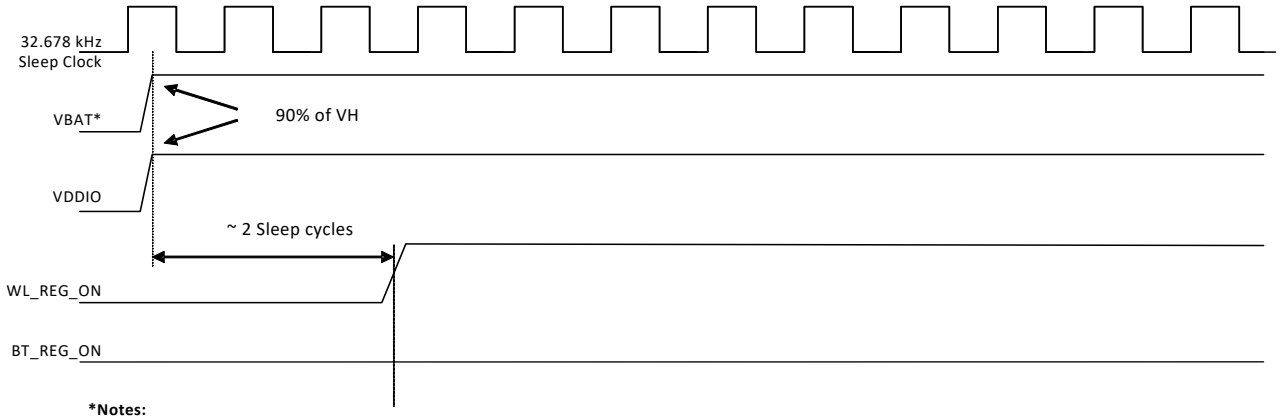
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 40. WLAN = OFF, Bluetooth = OFF



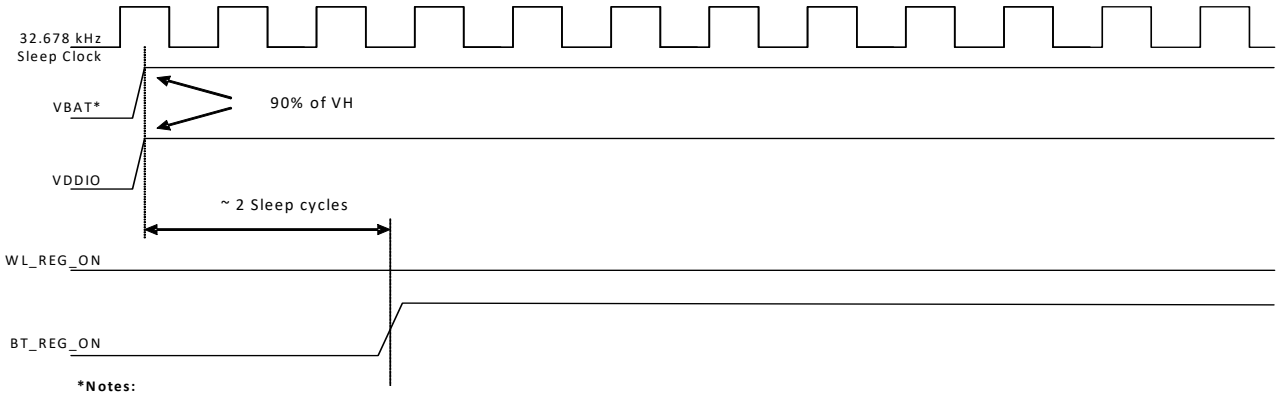
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 41. WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

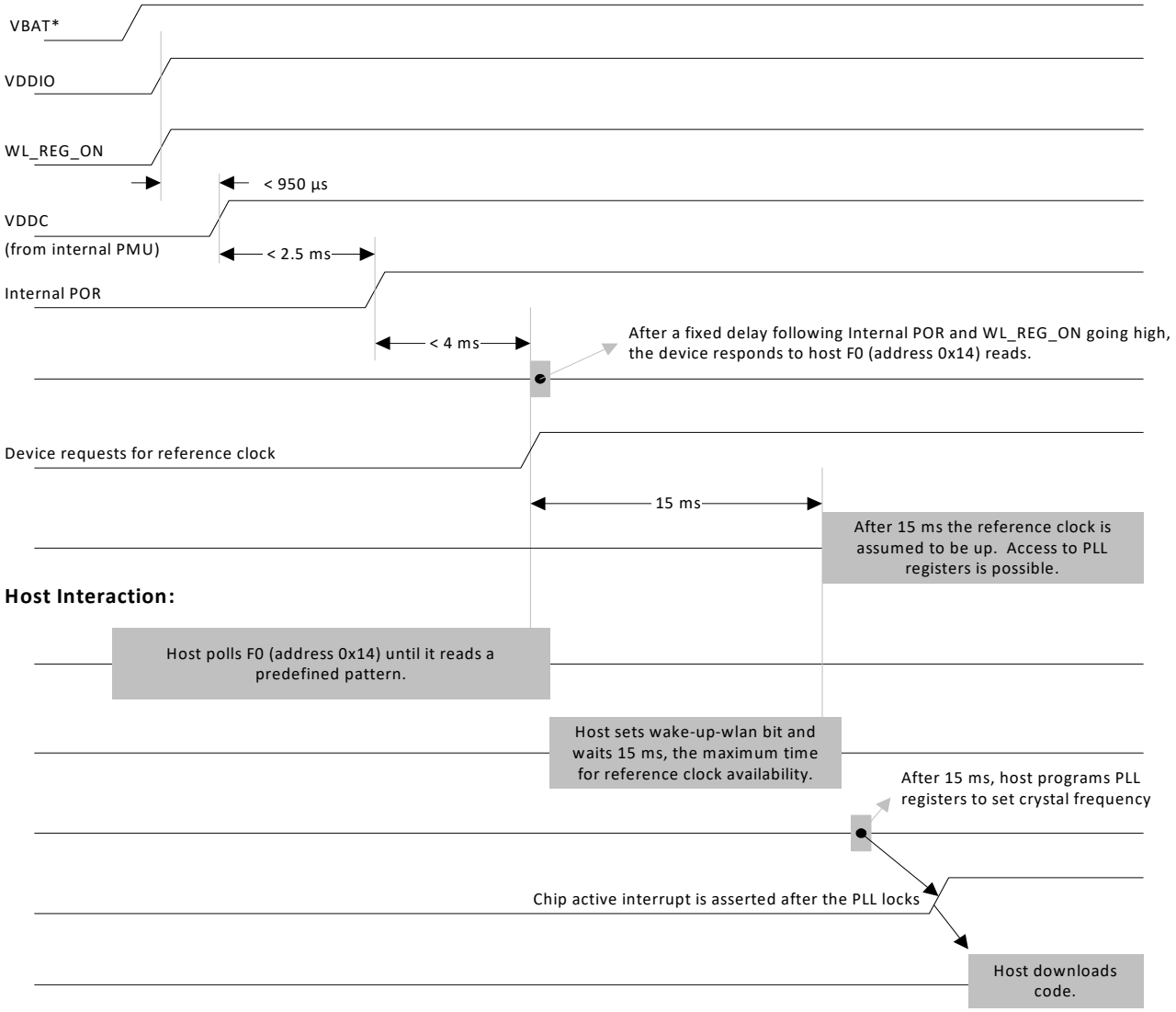
Figure 42. WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

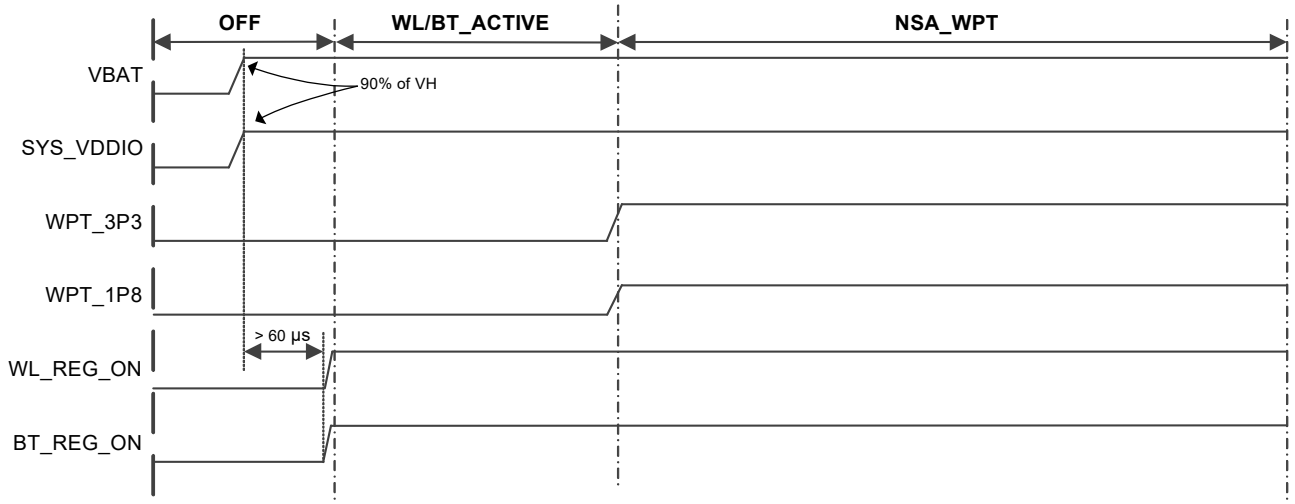
Figure 43 shows the WLAN boot-up sequence from power-up to firmware download.

Figure 43. WLAN Boot-Up Sequence for SDIO Host



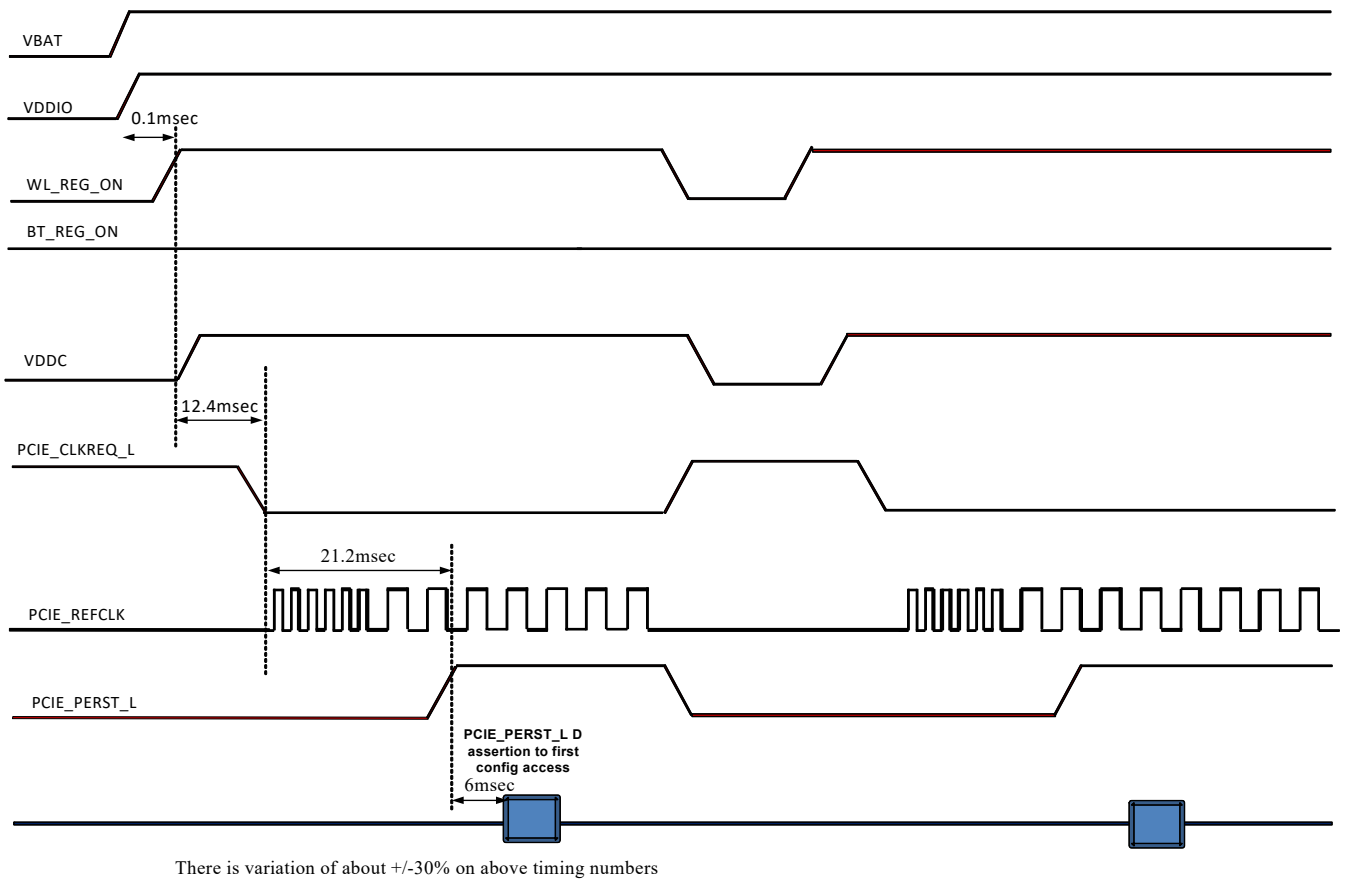
***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 44. VBAT to WPT



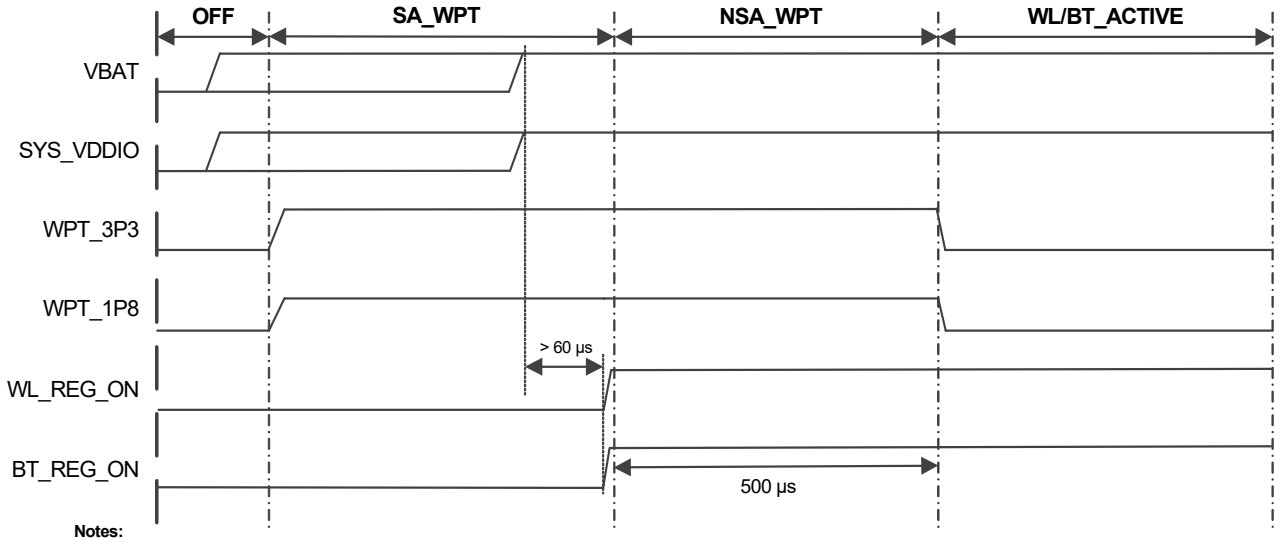
Notes:
1. VBAT, SYS_VDDIO, WPT_1P8, and WPT_3P3 should not rise 10%–90% faster than 40 µs.

Figure 45. WLAN Power-Up Sequence for PCIe Host



There is variation of about +/-30% on above timing numbers

Figure 46. WPT to VBAT



Notes:
1. VBAT, SYS_VDDIO, WPT_1P8, and WPT_3P3 should not rise 10%–90% faster than 40 µs.
2. Maintain 500 µs of NSA transition mode if PMU is needed from SA mode to Active mode.
3. WL_REG_ON should be asserted only when VBAT is stable.

20. Package Information

20.1 Package Thermal Characteristics

The information in Table 61 is based on the following conditions:

- No heat sink, T_A = 85°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = 0.96W continuous dissipation.
- Absolute junction temperature limits are maintained through active thermal monitoring or turning off one of the TX chains, or both.

Table 61. WLBGA Package Thermal Characteristics

Characteristic	WLBGA
θ_{JA} (°C/W) (value in still air)	33.8
θ_{JB} (°C/W)	6.53
θ_{JC} (°C/W)	2.63
Ψ_{JT} (°C/W)	10.2
Ψ_{JB} (°C/W)	15.71
Maximum Junction Temperature T_j (°C)	125
Maximum Power Dissipation (W)	0.96

20.2 Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$

The package thermal characterization parameter PSI_{JT} (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter $Theta_{JC}$ (θ_{JC}). The reason for this is that θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

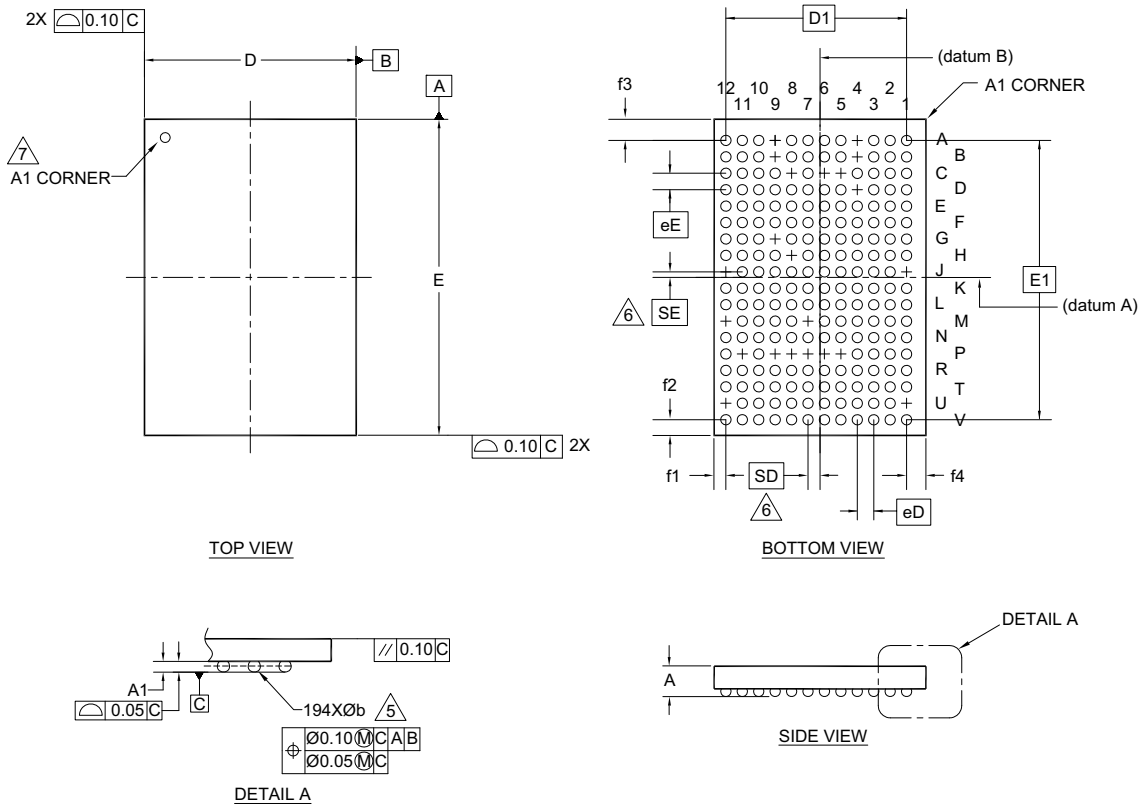
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

20.3 Environmental Characteristics

For environmental characteristics data, see Table 26 on page 68.

21. Mechanical Information

Figure 47. CYW5459x WLBGA Package Dimensions



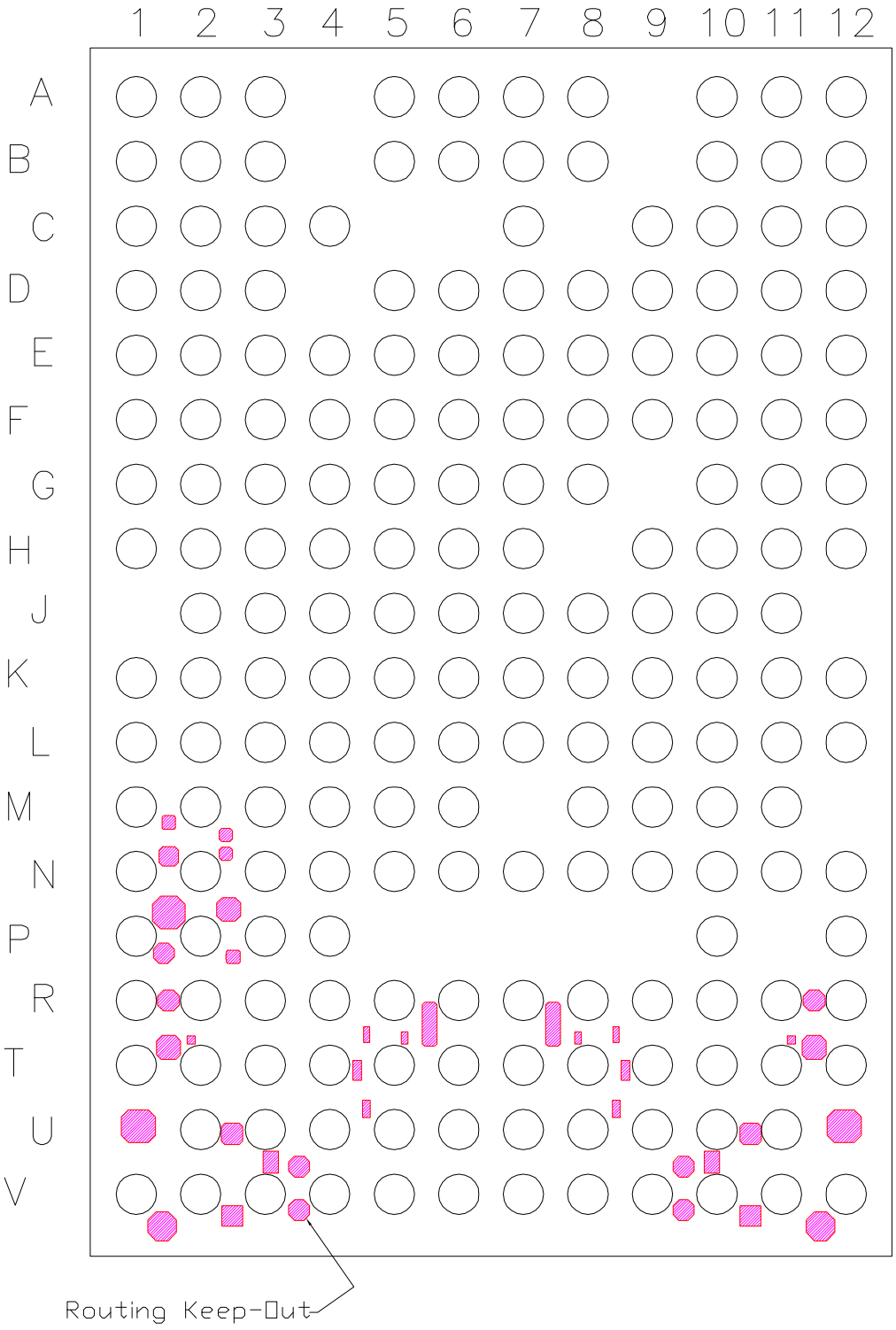
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.450	0.500	0.550
A1	0.160	0.190	0.220
D	5.115	5.155	5.195
E	7.658	7.698	7.738
D1		4.400 REF	
E1		6.800 REF	
MD		12	
ME		18	
N		194	
∅ b	0.20	0.25	0.30
eD		0.400 BSC	
eE		0.400 BSC	
SD		0.292 BSC	
SE		0.135 BSC	
f1		0.285 BSC	
f2		0.384 BSC	
f3		0.514 BSC	
f4		0.470 BSC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
7. A1 CORNER TO BE IDENTIFIED BY LASER MARK
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

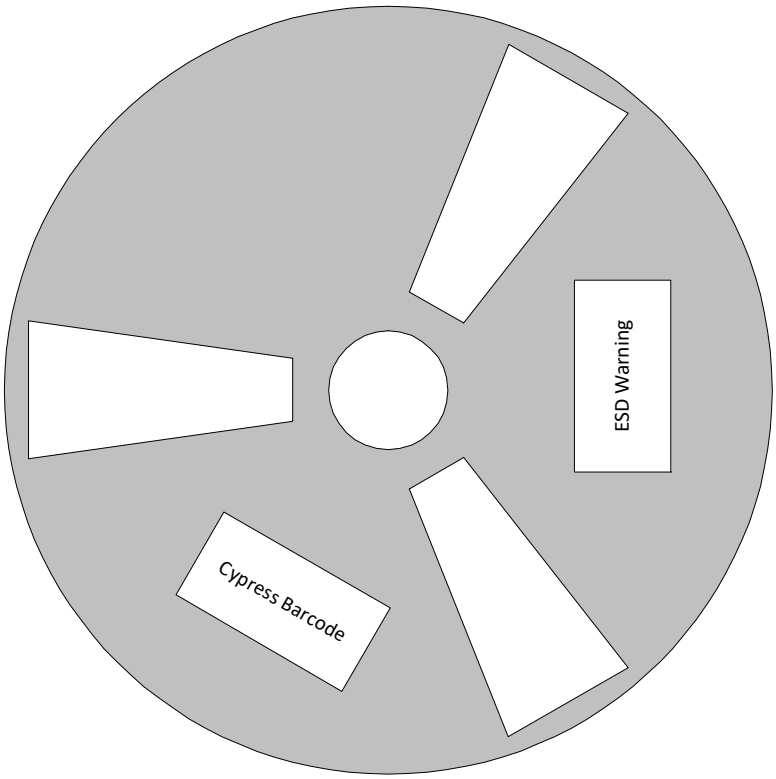
002-23200 *A

Figure 48. WLBGA Keep-Out Areas for PCB Layout (Top View, Balls Facing Down)



21.1 Tape, Reel, and Packing Specification

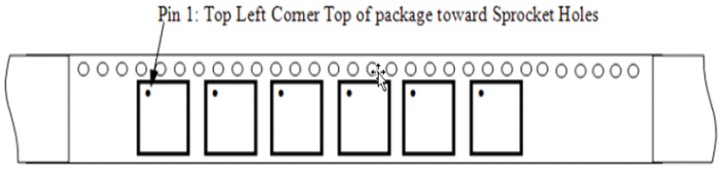
Figure 49. Reel, Labeling and Packaging



Reel Diameter: 330 +/- 2.0 mm

Device Orientation/Mix Lot Number

Each reel may contain up to three lot numbers, independent of the date code. Individual lots must be labeled on the box, moisture barrier bag, and the reel.



Pin 1 Orientation L relative to the carrier tape sprocket holes

22. Ordering Information

Table 62. Part Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW54591RKUBG	194-ball WLBGA (5.16 × 7.7mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN and Bluetooth 5.1 IEEE 802.11ac 2×2 RSDB combo	–40°C to +85°C
CYW54591RKUBGT	194-ball WLBGA (5.16 × 7.7mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN and Bluetooth 5.1 IEEE 802.11ac 2×2 RSDB combo, Tape and Reel.	–40°C to +85°C
CY54590RKUBG	194-ball WLBGA (5.16 × 7.7mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN and Bluetooth 5.1 IEEE 802.11ac 2x2 MIMO combo	–40°C to +85°C
CY54590RKUBGT	194-ball WLBGA (5.16 × 7.7mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN and Bluetooth 5.1 IEEE 802.11ac 2x2 MIMO combo, Tape and Reel	–40°C to +85°C

Note
85. CYW5459x parts receive Commercial grade testing.

23. Additional Information

23.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: cypress.com/glossary.

Table 63. Acronyms used in this Document

Term	Description
A2DP	advanced audio distribution profiles
AES	advanced encryption standard
AES-CTR	advanced encryption standard-counter mode
ALU	arithmetic logic unit
AoA	angle of arrival
AoD	angle of departure
APB	advanced peripheral bus
APU	audio processing unit
BBC	bluetooth baseband core
BER	bit-error rate
CBC-MAC	cipher block chaining message authentication code
CCK	complementary code keying
CCM	counter with cipher block chaining message authentication code
CML	common mode logic
CRC	cyclic redundancy check
CSC	cypress serial control
CTS	clear to send
DMA	direct memory access
DSSS	direct sequence spread spectrum
DTE	data termination equipment
ED	erroneous data
EDR	enhanced data rate
EIR	extended inquiry response
EPR	encryption pause resume
ESR	equivalent series resistance
eSCO	extended synchronous connections
FEC	forward error correction
FEM	front-end module
FFT	fast fourier transform
HEC	header error control
HID	human interface device
HCI	host control interface
HS	high-speed
IFC	inter-frame spacing

Term	Description
IHR	internal hardware registers
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LO	local oscillator
LPO	low-power oscillator
LSTO	link supervision timeout
LTE	long term evolution
MIB	management information base
MIC	message integrity check
MSb	most significant bit
NAV	network allocation vector
OFDM	orthogonal frequency division multiplexing
PBF	packet boundary flag
PDM	pulse density modulation
PLC	packet loss concealment
PLL	phase locked loop
POR	power-on reset
PMU	power management unit
PSM	programmable state machine
QoS	quality of service
RSDB	real simultaneous dual-band
RSSI	receiver signal strength indication
RTS	request to send
RX/TX	receive, transmit
RXE	receive engine
SAM	slot availability mask
SDIO	Secure Digital Input Output
SPI	serial peripheral interface
SP3T	single pole 3 throw
SSP	secure simple pairing
SSR	sniff subrating
SWD	serial wire debug

Table 63. Acronyms used in this Document (Cont.)

Term	Description
IBSS	independent basic service set
TBTT	target beacon transmission time
TCXO	temperature compensated crystal oscillator
TKIP	temporal key integrity protocol
TSF	timing synchronization function
TSSI	transmit signal strength indicator
TXE	transmit engine
TXOP	transmit opportunity
UART	universal asynchronous receiver/transmitter
WBS	wideband speed
WD	watchdog
WEP	wired equivalent privacy
WMM	Wi-Fi multimedia
WPA	Wi-Fi protected access
WPS	Wi-Fi protected setup

23.2 References

The references in this section may be used in conjunction with this document.

Note
Cypress provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site (see IoT Resources).

For Cypress documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Bluetooth MWS Coexistence 2–wire Transport Interface Specification	–	www.bluetooth.com

23.3 IoT Resources

Cypress provides a wealth of data at www.cypress.com/solutions/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (community.cypress.com)

Document History

Document Title: CYW5459x, Single-Chip Wi-Fi 5 IEEE 802.11 ac 2×2 MAC/Baseband/Radio with RSDB and Bluetooth 5.1 for Commercial/Consumer Applications Document Number: 002-29787			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6812660	02/26/2020	Initial release.
*A	7137192	05/10/2021	Updated the title as “Single-Chip Wi-Fi 5 IEEE 802.11 ac 2×2 MAC/Baseband/Radio with RSDB and Bluetooth 5.1 for Commercial/Consumer Applications”. Updated the Part number as CYW5459x throughout the document. Updated Bluetooth Key Features and Standards Compliance. Added SDIO in Figure 1, Figure 2, Figure 3 and Figure 4. Updated Features and IEEE 802.11ac PHY. Added SDIO in Table 1, Table 22, Table 24, and Table 27. Updated SPROM Interface. Added SDIO v3.0 and SDIO Timing sections. Updated Figure 24. Added A5-A8, B6, B8 SDIO Parts in the Table 17. Added “WLAN SDIO Bus” in Table 18. Updated Table 20 and Table 21. Updated Table 36, Table 37 and Table 38. Added Figure 43. Changed Bluetooth 4.2 to Bluetooth 5.1 and added Part Numbers: “CY54590RKUBG”, “CY54590RKUBGT” in Table 62. Replaced Bluetooth 5.0 with Bluetooth 5.1 throughout the document.
*B	7202656	07/28/2021	Updated Table 27 max values. Updated Table 59.

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