SPOC™+ 12V

BTS54220-LBE

SPI Power Controller

Data Sheet

Rev. 2.2, 2016-10-10

Automotive

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 2.2, 2016-10-10	
All	Package name changed General: Typos corrected and wording improved **Table 1**: Channel description improved **Table 4**: Footnote added **Table 5**: Updated and Footnote added **Chapter 5.1.3**: Updated **Chapter 5.1.6**: Note added **Chapter 5.2**: Updated **Chapter 6.3**: Updated **Chapter 7.2**: Updated **Figure 28** updated

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	Parameter P_9.4.19: Test Condition updated Parameter P_9.4.20: Test Condition updated Parameter P_9.4.22: Max. Value improved Parameter P_9.4.24: Min. Value improved Parameter P_9.4.26: Min. Value improved Parameter P_9.4.28: Min. Value improved Parameter P_9.4.30: Min. Value improved Parameter P_9.4.32: Min. Value improved Parameter P_9.4.34: Test Condition updated and Max. Value improved **Chapter 9.5**: Content improved **Figure 33**: Content updated **Figure 34**: Content updated **Chapter 9.6**: Content improved **Chapter 9.6.3** added **Chapter 9.7**: Content improved **Chapter 9.7.8**: Descriptions improved and Footnote added Chapter 9.8 removed. Redundant information **Figure 35**: Content updated **Table 16** updated
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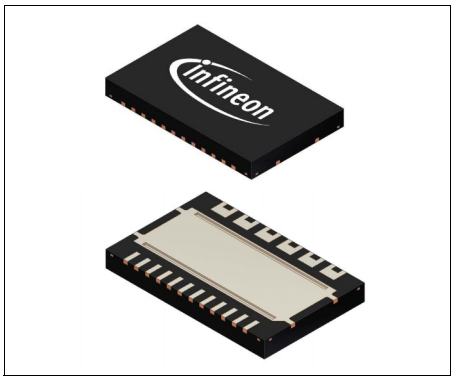
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1 Overview



TSON-24-10

Features

- 8-bit serial peripheral interface (daisy chain capable SPI) for control and diagnosis
- CMOS compatible parallel input pins for two channels
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Integrated control for one external smart power switch
- Very low stand-by current
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

Description

The BTS54220-LBE is a four channel high-side smart power switch in TSON-24-10 package providing embedded protective functions. It is specially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is designed to drive exterior lamps up to 65 W and 27 W, HIDL or the equivalent LED light.

Table 1 Product Summary

Operating Voltage Power Switch	V_S	5.5 … 28 V
Logic Supply Voltage	V_{DD}	3.8 … 5.5 V
Over Voltage Protection	$V_{S(AZ,min)}$	42 V
Maximum Stand-By Current at 25 °C	$I_{VS(STB)}$	1 µA
Maximum ON State Resistance at T_j = 150 °C 9 mΩ channels (Channel 1, 4)	$R_{DS(ON,max)}$	18.2 mΩ
Maximum ON State Resistance at T_j = 150 °C 27 mΩ channels (Channel 2, 3)	$R_{DS(ON,max)}$	55 mΩ
SPI Access Frequency	$f_{SCLK(max)}$	3 MHz

Configuration and status diagnosis are done via SPI. An 8-bit serial peripheral interface (SPI) is used. The SPI is daisy chain capable.

Type	Package	Marking
BTS54220-LBE	TSON-24-10	BTS54220-LBE

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The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over temperature flag per output is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to V_S diagnosis.

27 mΩ channels can be configured to bulb or LED mode for maximum flexibility.

The BTS54220-LBE provides a fail-safe feature via a Limp Home Input (LHI) pin and direct Input pins.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART technology.

Applications

- High-side power switch for 12 V in automotive or industrial applications such as lighting, heating, motor driving, energy and power distribution
- Especially designed for standard exterior lighting like high beam, low beam, position light, tail light, brake light, parking light, license plate light, indicators and equivalent in the LED technology
- Replaces electromechanical relays, fuses and discrete circuits

Protective Functions

- Reverse battery protection with external components
- Short circuit to ground protection
- Stable behavior at under voltage
- Current limitation
- Absolute and dynamic temperature sensor
- Thermal shutdown with latch after a limited amount of retries
- Overvoltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio (k_{ILIS}) configurable for LEDs or bulbs
- Very fast diagnosis in LED mode
- Feedback on over temperature via SPI
- Short circuit to V_S detection
- Monitoring of Input pins status

Application Specific Functions

- Fail-safe activation via LHI pin and control via input pins
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs
- LED mode selection available
- SPI with daisy chain capability
- Switch bypass monitoring for detecting short circuit to V_S

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2 Block Diagram

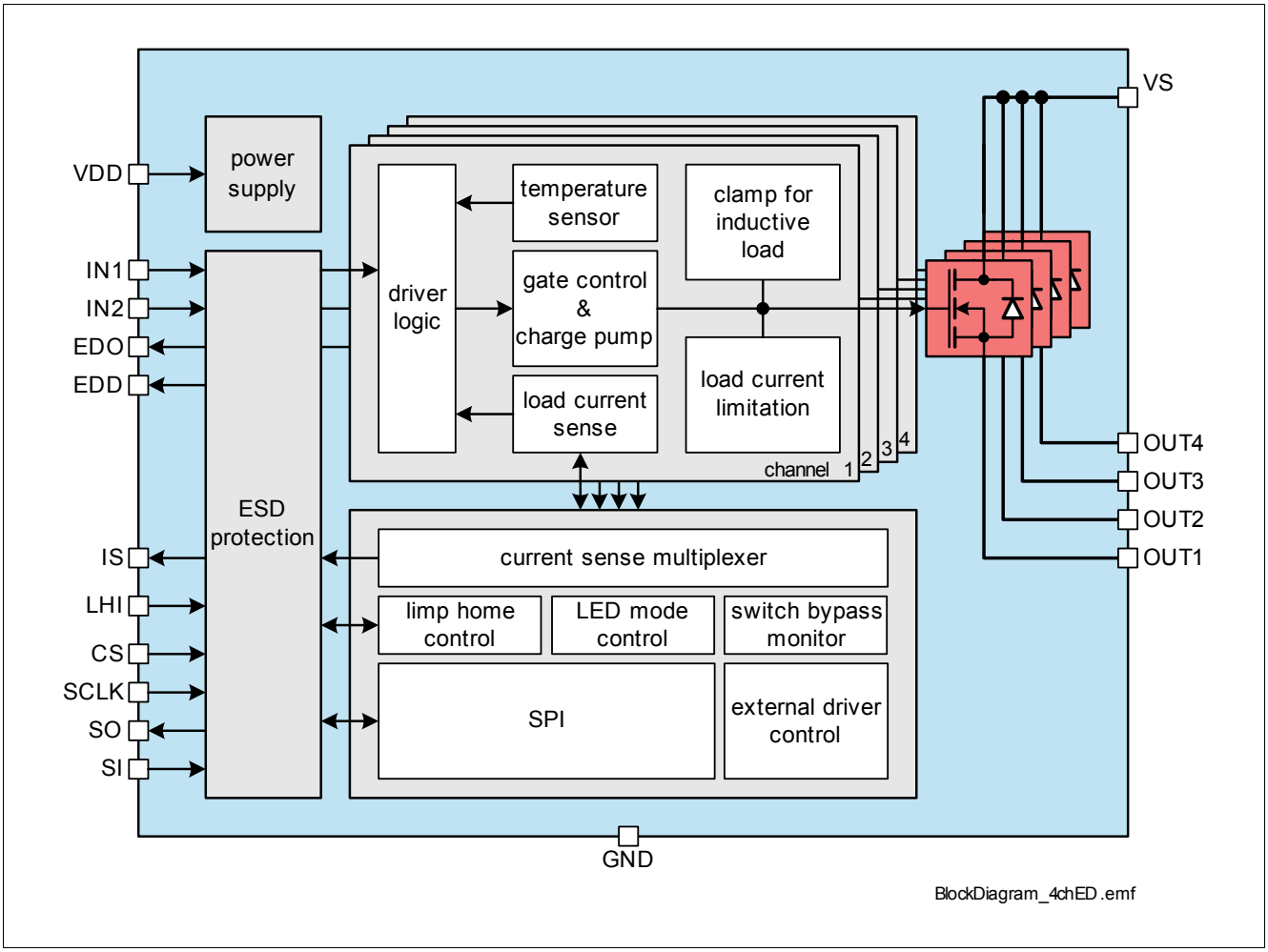


Figure 1 Block Diagram BTS54220-LBE

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2.1 Terms

Figure 2 shows all terms used in this data sheet, with associated convention for positive values.

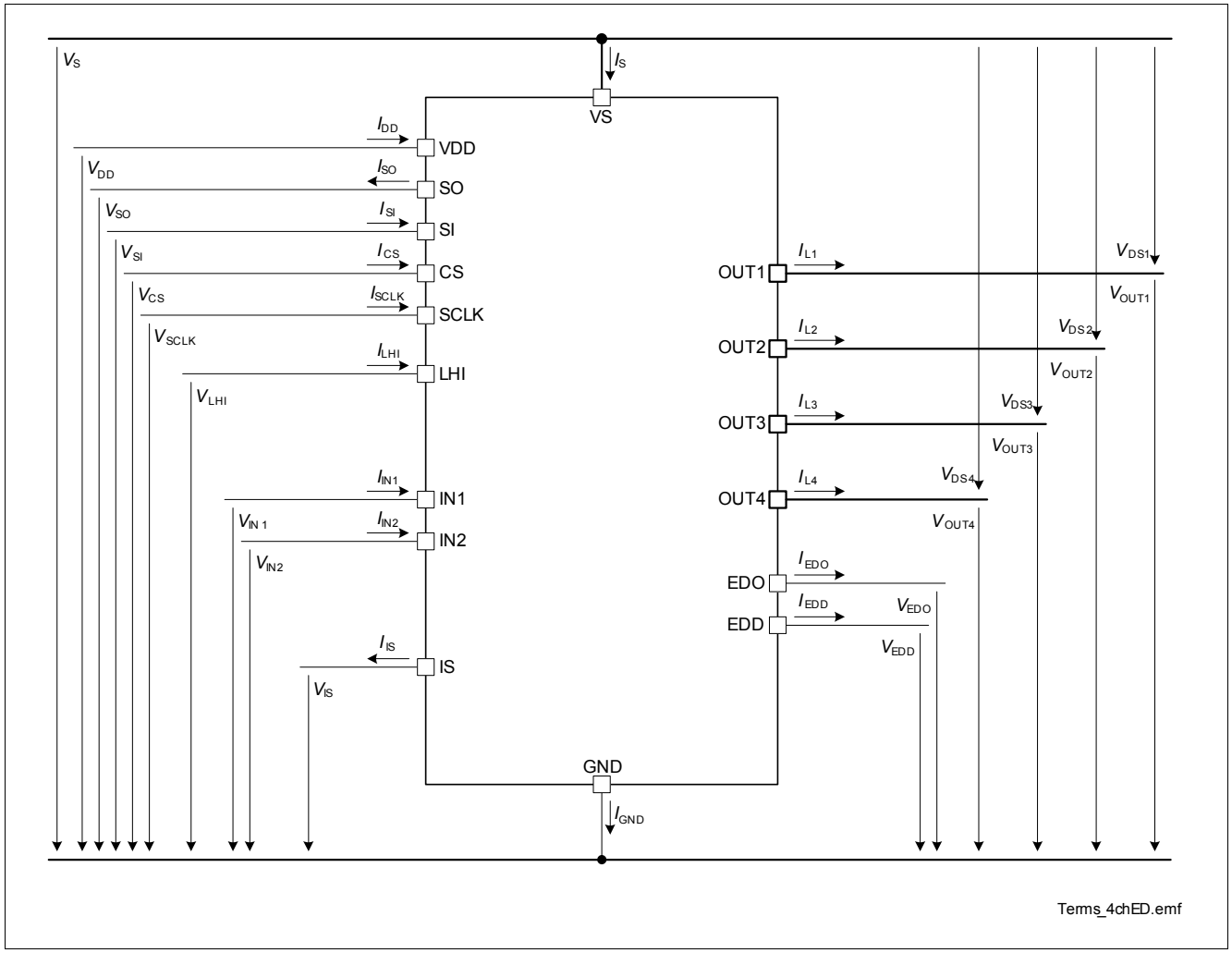


Figure 2 Voltage and Current Definition

In all tables of electrical characteristics, symbols related to channels without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS1} ... V_{DS4}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. **`HWCR.STB`**) with the exception of the bits in the Diagnosis frames which are marked only with `PARAMETER` (e.g. **`VSMON`**).

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3 Pin Configuration

3.1 Pin Assignment BTS54220-LBE

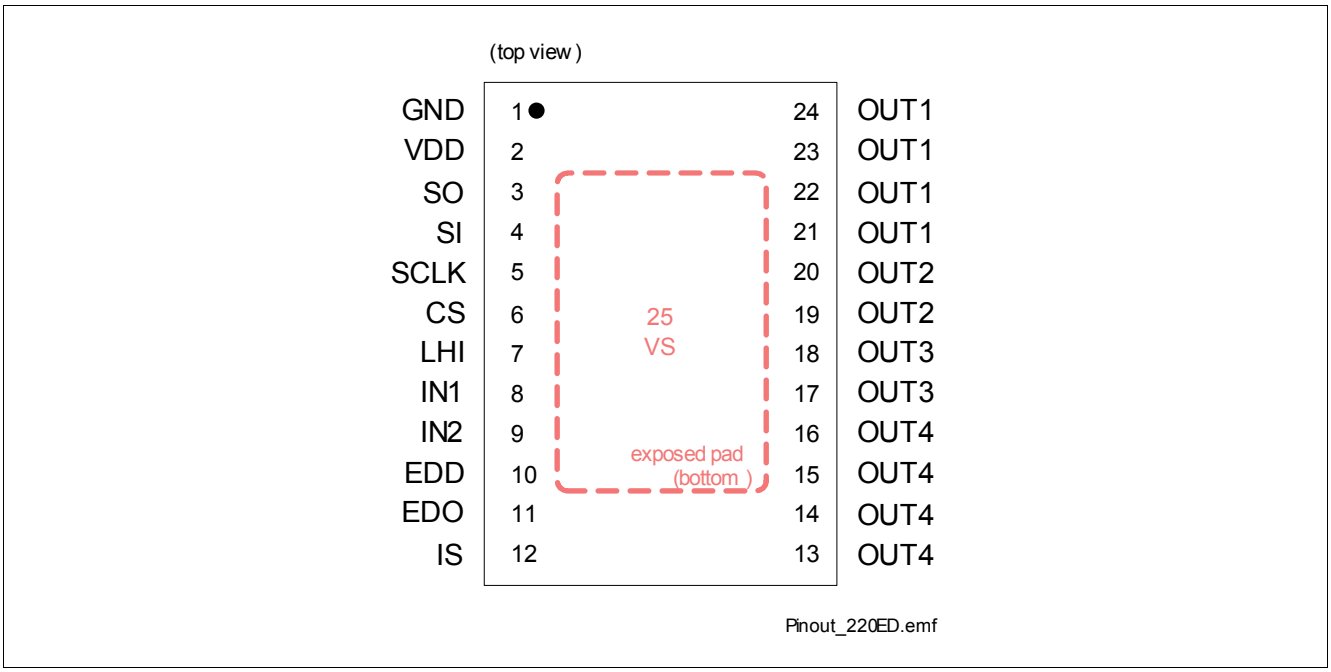


Figure 3 Pin Configuration TSON-24-10

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3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
25	VS	–	Positive power supply for high-side power switch
1	GND	–	Ground connection
2	VDD	–	Logic supply (5 V)
SPI & Diagnosis Pins			
3	SO	O	Serial output of SPI interface
4	SI	I	Serial input of SPI interface (“high” active)
5	SCLK	I	Serial clock of SPI interface (“high” active)
6	CS	I	Chip select of SPI interface (“low” active); Integrated pull up to VDD
12	IS	O	Current sense output signal
Limp Home Input Pin (integrated pull-down, leave unused Limp Home Input pin unconnected)			
7	LHI	I	Limp home activation signal (“high” active)
Parallel Input Pins (integrated pull-down, leave unused pins unconnected)			
8	IN1	I	Input signal of channel 1 (“high” active)
9	IN2	I	Input signal of channel 2 (“high” active)
External Driver Pins (leave unused external driver pins unconnected)			
10	EDD	O	External driver diagnosis enable signal for external driver
11	EDO	O	External driver output for activation for external driver
Power Output Pins			
21, 22, 23, 24 [1)]	OUT1	O	Protected high-side power output of channel 1
19, 20 [1)]	OUT2	O	Protected high-side power output of channel 2
17, 18 [1)]	OUT3	O	Protected high-side power output of channel 3
13, 14, 15, 16 [1)]	OUT4	O	Protected high-side power output of channel 4

1) All outputs pins of each channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

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4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T_j = -40 to +150 °C; all voltages with respect to ground

Typical resistive loads connected to the outputs (unless otherwise specified):

9 mΩ channels: R_L = 2.2 Ω

27 mΩ channels: R_L = 6.8 Ω (33 Ω when **LGCR.LEDn** = “1”)

Table 2 Absolute Maximum Ratings[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage							
Power supply voltage	V_S	-0.3		28	V	–	P_4.1.1
Logic supply voltage	V_{DD}	-0.3		5.5	V	–	P_4.1.2
Reverse polarity voltage	$-V_{S(rev)}$	–		16	V	[2)] T_{jStart} = 25 °C t ≤ 2 min. See **Chapter 10** for setup	P_4.1.3
Supply voltage for short circuit protection (single pulse)	$V_{S(SC)}$	0		28	V	[3)] R_{ECU} = 20 mΩ l = 0 or 5 m R_{Cable} = 16 mΩ/m L_{Cable} = 1 µH/m	P_4.1.5
Permanent short circuit number channel activations All channels	n_{RSC1}	-		100	k	[3)] V_{DD} = 5 V t_{ON} = 300 ms	P_4.1.6
Voltage at power transistor	V_{DS}	–		42	V	–	P_4.1.8
Supply voltage for load dump protection	$V_{S(LD)}$	–		42	V	[4)] R_I = 2 Ω t = 400 ms	P_4.1.9
Current through ground pin	I_{GND}	-100		25	mA	t ≤ 2 min.	P_4.1.10
Current through VDD pin	I_{DD}	-25		30	mA	t ≤ 2 min.	P_4.1.11
Power Stages							
Load current	$\|I_L\|$	–		$I_{L(LIM)}$	A	[5)]	P_4.1.12
Maximum energy dissipation single pulse - $I_{L(nom)}$ 9 mΩ ch.	E_{AS}	–		145	mJ	[6)] $T_{j(0)}$ = 150 °C $I_{L(0)}$ = $I_{L(nom)}$ = P_6.6.15	P_4.1.13
Maximum energy dissipation single pulse - $I_{L(nom)}$ 27 mΩ ch.	E_{AS}	–		135	mJ	[6)] $T_{j(0)}$ = 150 °C $I_{L(0)}$ = $I_{L(nom)}$ = P_6.6.16	P_4.1.14

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Table 2 Absolute Maximum Ratings[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Diagnosis Pin							
Voltage at sense pin IS	V_{IS}	-0.3		V_S	V	–	P_4.1.24
Current through sense pin IS	I_{IS}	-10		40	mA	$t \leq 2$ min.	P_4.1.25
Input Pins							
Voltage at input pins	V_{IN}	-0.3		6.0	V	–	P_4.1.26
Current through input pins	I_{IN}	-0.75		0.75	mA	–	P_4.1.27
Current through input pins	I_{IN}	-2.0		10	mA	$t \leq 2$ min.	P_4.1.28
SPI Pins							
Voltage at chip select pin	V_{CS}	-0.3		6.0	V	–	P_4.1.29
Current through chip select pin	I_{CS}	-0.75		0.75	mA	–	P_4.1.30
Current through chip select pin	I_{CS}	-2.0		10	mA	$t \leq 2$ min.	P_4.1.31
Voltage at serial input pin	V_{SI}	-0.3		6.0	V	–	P_4.1.32
Current through serial input pin	I_{SI}	-0.75		0.75	mA	–	P_4.1.33
Current through serial input pin	I_{SI}	-2.0		10	mA	$t \leq 2$ min.	P_4.1.34
Voltage at serial clock pin	V_{SCLK}	-0.3		6.0	V	–	P_4.1.35
Current through serial clock pin	I_{SCLK}	-0.75		0.75	mA	–	P_4.1.36
Current through serial clock pin	I_{SCLK}	-2.0		10	mA	$t \leq 2$ min.	P_4.1.37
Current through serial output pin SO	I_{SO}	-0.75		0.75	mA	–	P_4.1.38
Current through serial output pin SO	I_{SO}	-10		2.0	mA	$t \leq 2$ min.	P_4.1.39
Limp Home Input Pin							
Voltage at Limp Home Input pin	V_{LHI}	-0.3		6.0	V	–	P_4.1.40
Current through Limp Home Input pin	I_{LHI}	-0.75		0.75	mA	–	P_4.1.41
Current through Limp Home Input pin	I_{LHI}	-2.0		10	mA	$t \leq 2$ min.	P_4.1.42
External Driver Pins							
Voltage at external driver output	V_{EDO}	-0.3		6.0	V	–	P_4.1.43
Current through external driver output	I_{EDO}	-10		1.0	mA	$t \leq 2$ min.	P_4.1.44
Voltage at external driver diagnosis enable	V_{EDD}	-0.3		6.0	V	–	P_4.1.55
Current through external driver diagnosis enable	I_{EDD}	-10		1.0	mA	$t \leq 2$ min.	P_4.1.56
Temperatures							
Junction temperature	T_j	-40		150	°C	–	P_4.1.45
Dynamic temperature increase while switching	ΔT_j	–		60	K	–	P_4.1.46
Storage temperature	T_{stg}	-55		150	°C	–	P_4.1.47
ESD Susceptibility							

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Table 2 Absolute Maximum Ratings[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility HBM OUT pins vs. VS	V_{ESD}	-4		4	kV	7) HBM	P_4.1.48
ESD susceptibility HBM all pins vs. VDD	V_{ESD}	-1.5		1.5	kV	7) HBM	P_4.1.54
ESD susceptibility HBM other pins vs. GND incl. OUT pins vs. GND	V_{ESD}	-2		2	kV	7) HBM	P_4.1.49
ESD Resistivity to GND	V_{ESD}	-500		500	V	8) CDM	P_4.1.51
ESD Resistivity Pin 1, 12, 13, 24 (corner pins) to GND	$V_{ESD1, 12, 13, 24}$	-750		750	V	8) CDM	P_4.1.52

1) Not subject to production test, specified by design.

2) Device is mounted on an FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip and package) was simulated on a 76.4 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) EOL tests according to AECQ100-012. Threshold limit for short circuit failures: 100 ppm. Please refer to the legal disclaimer for short-circuit capability at the end of this document.

4) R_I is the internal resistance of the load dump pulse generator.

5) Current limitation is a protection feature. Protection features are not designed for continuous repetitive operation.

6) Pulse shape represents inductive switch OFF: $I_{D(t)} = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

7) ESD resistivity, HBM according to ANSI/ESDA/JEDEC JS-001-2010

8) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

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4.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	2	–	K/W	1) $T_{j(0)}$ = 105 °C measured to pin 25	P_4.2.1
Junction to Ambient	R_{thJA}	–	21	–	K/W	1)2) $T_{j(0)}$ = 105 °C	P_4.2.2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.4 * 114.3 * 1.5 mm board with 2 inner copper layers (2 * 70 µm Cu, 2 * 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

4.2.1 PCB Setup

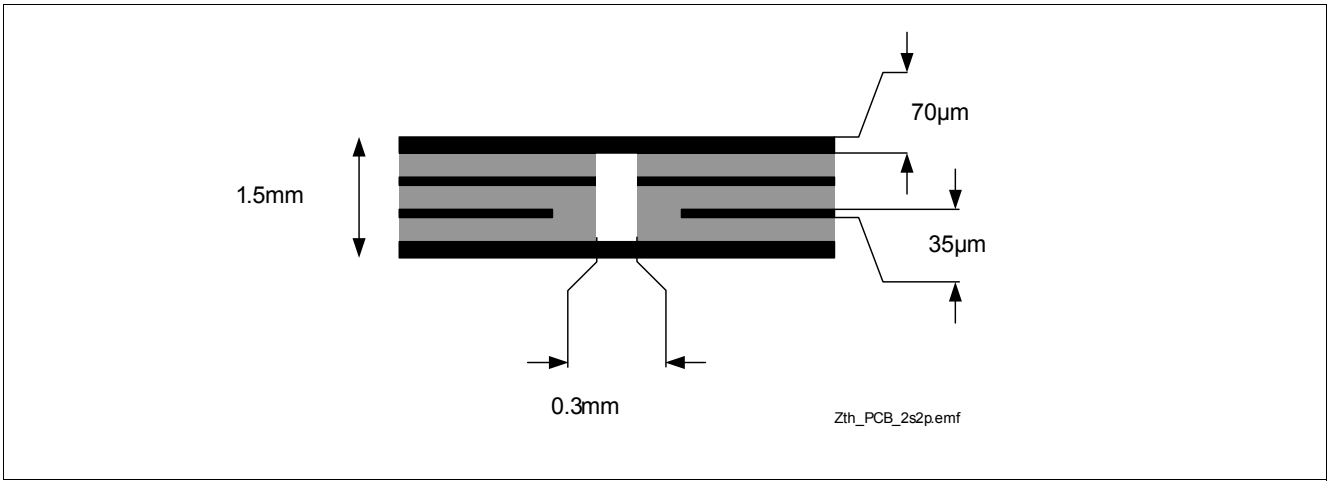


Figure 4 2s2p PCB Cross Section

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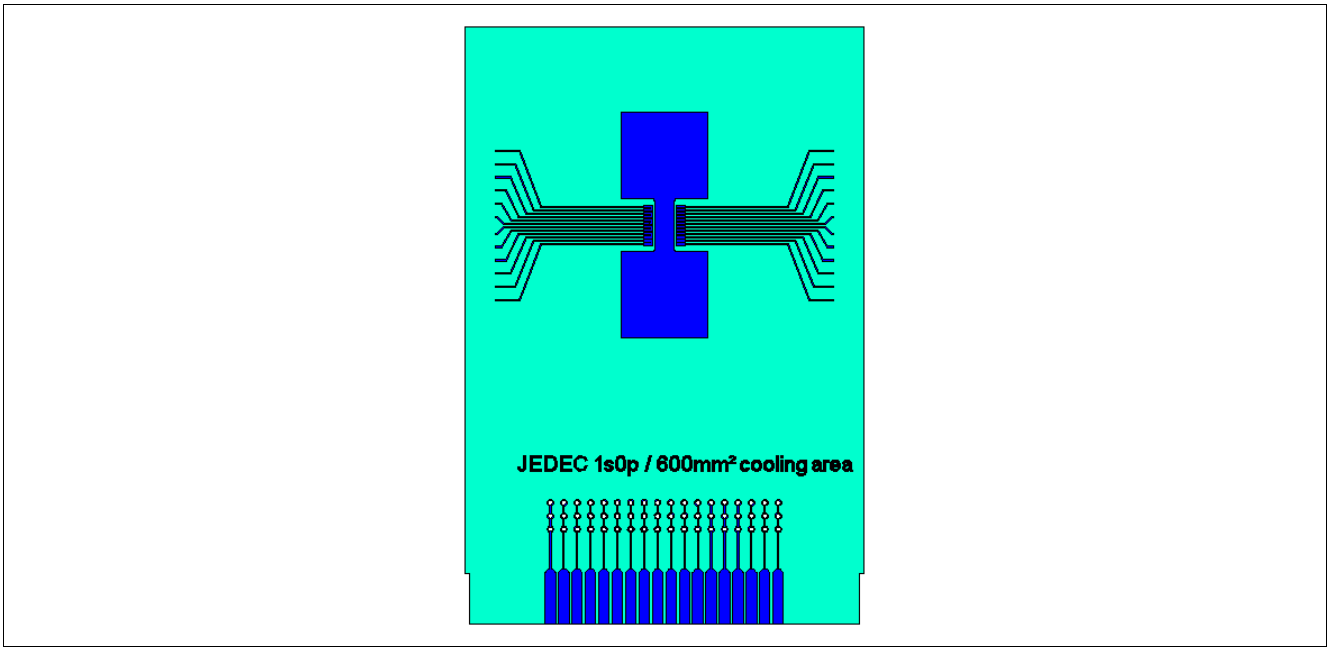


Figure 5 PC Board for Thermal Simulation with 600 mm² Cooling Area

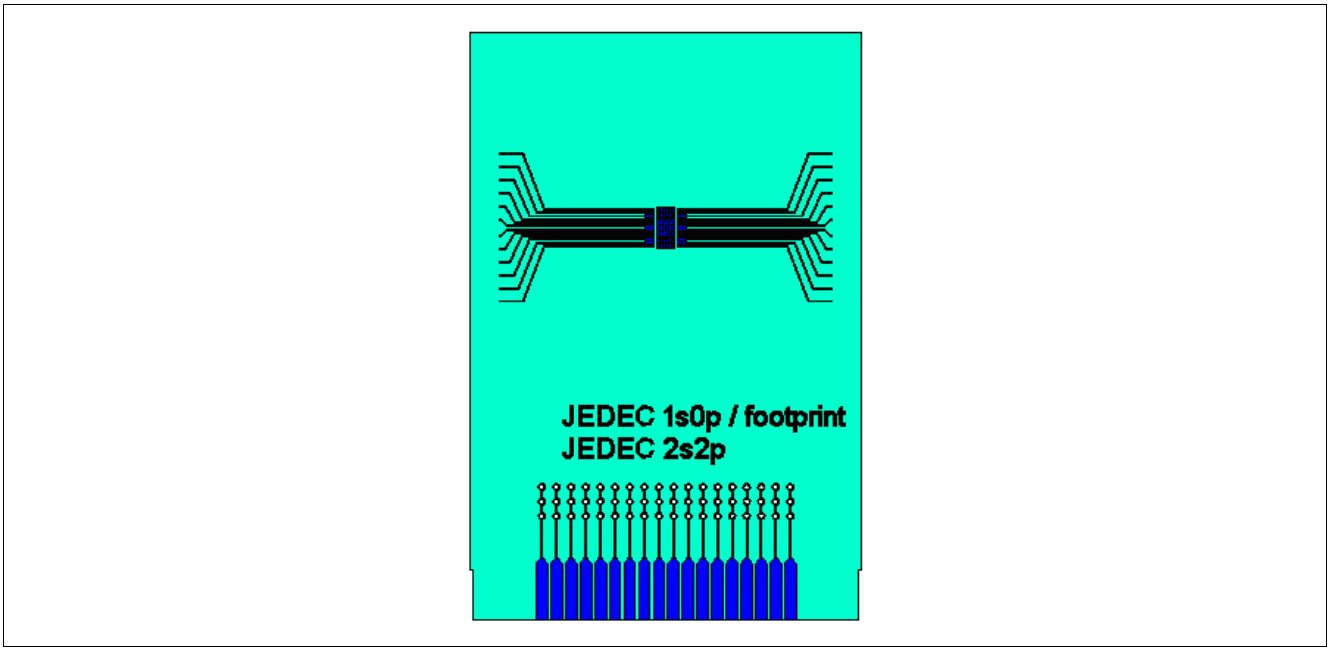


Figure 6 PC Board for Thermal Simulation with 2s2p Cooling Area

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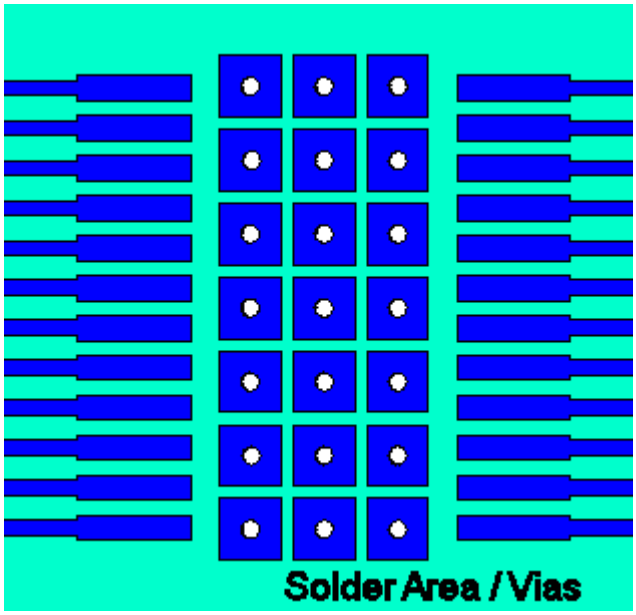


Figure 7 Solder Area / Vias

4.2.2 Thermal Impedance

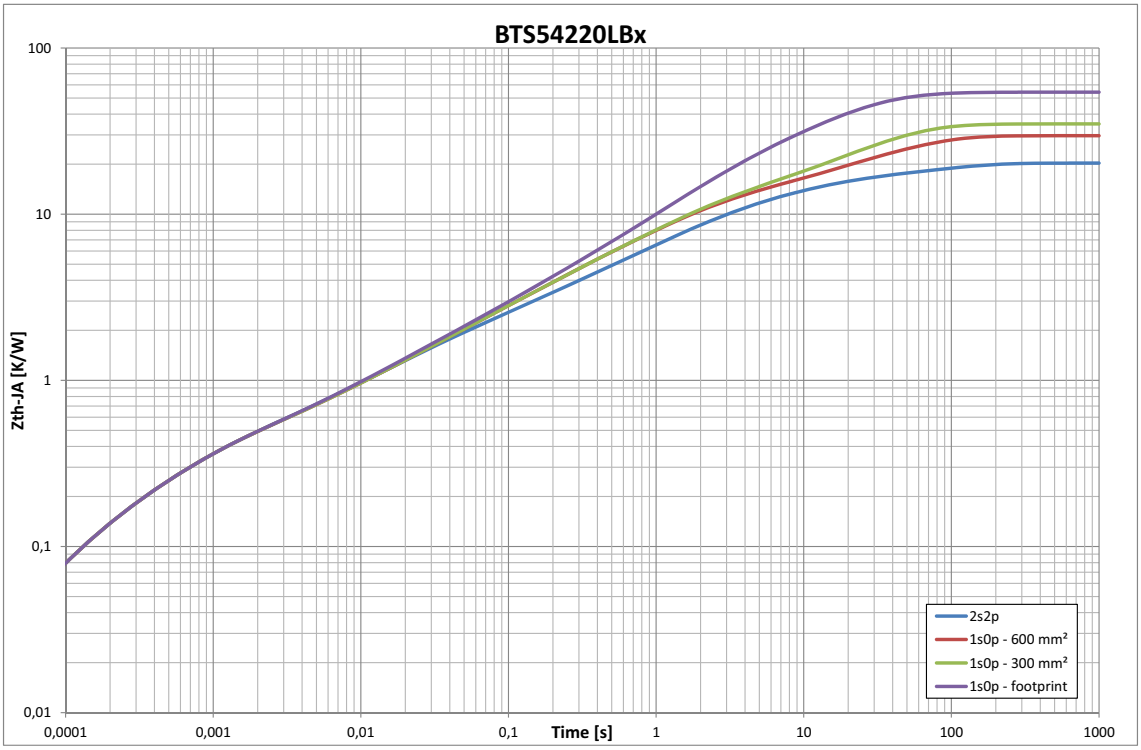


Figure 8 Typical Thermal Impedance. PCB setup according Figure 6

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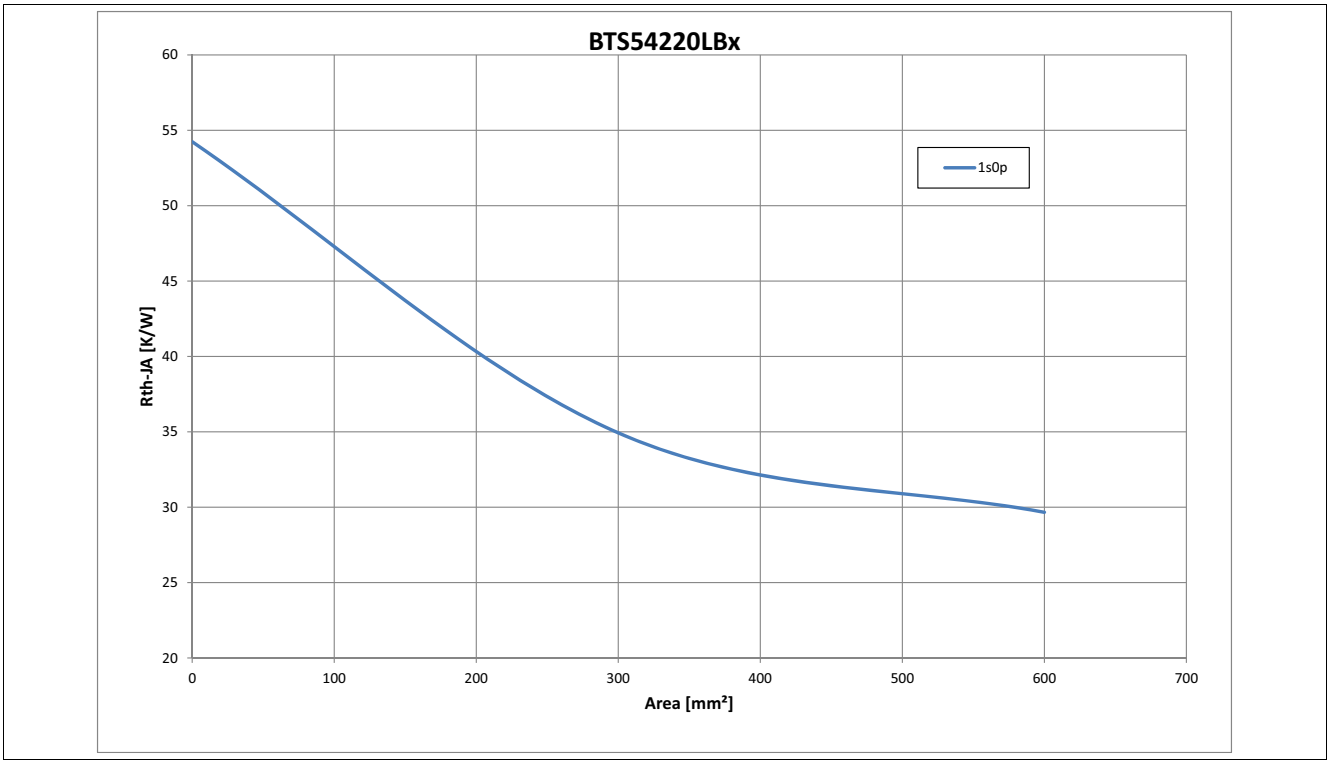


Figure 9 Typical Thermal Resistance. PCB setup 1s0p

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5 Power Supply

The BTS54220-LBE is supplied by two voltage sources:

- V_S (analog supply voltage)
- V_{DD} (digital supply voltage)

The V_S supply line is connected to a battery feed and used for the driving circuitry of the power stages, while V_{DD} is used for the SPI logic and for driving SO pin.

V_S and V_{DD} supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold. More in detail:

- An undervoltage on V_{DD} supply prevents SPI communication. SPI registers are reset to default values. The retry counters used to protect the channels are reset therefore the channels are in “unlimited restart” mode.
- An undervoltage on V_S supply switches OFF all channels, even in Limp Home mode. The channels are enabled again as soon as $V_S = V_{S(OP)}$.

The voltage at pin VS is also monitored. In case of a negative voltage transient resulting in $V_S < V_{SMON}$ with **DCR.MUX** ≠ “111_B”, any SPI command sent by the micro-controller is not accepted (see **Chapter 9.5** for further details).

An overview of channel behavior according to different V_S and V_{DD} supply voltages is shown in **Table 4** (the table is valid after a successful supply voltage ramp-up).

Table 4 Device capability as function of V_S and V_{DD}

	$V_{DD} \le V_{DD(PO)}$ ($V_{DD(PO)}$ = P_5.3.17)	$V_{DD} > V_{DD(PO)}$
$V_S \le V_{SMON}$ (V_{SMON} = P_5.3.12)	Channels are OFF	Channels are OFF
	SPI registers reset	SPI registers protected[1]
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication available[2] (f_{SCLK} = 3 MHz)
	Limp Home mode not available	Limp Home mode not available
$V_{SMON} < V_S \le V_{S(UV)}$ ($V_{S(UV)}$ = P_5.3.2)	Channels are OFF	Channels are OFF
	SPI registers reset	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication available (f_{SCLK} = 3 MHz)
	Limp Home mode available (channels are OFF)	Limp Home mode available (channels are OFF)
$V_S > V_{S(UV)}$[3]	Channels cannot be controlled by SPI	Channels can be switched ON and OFF
	SPI registers reset	SPI registers available
	SPI communication not available (f_{SCLK} = 0 MHz)	SPI communication available (f_{SCLK} = 3 MHz)
	Limp Home mode available	Limp Home mode available

1) If **DCR.MUX** ≠ 111_B, otherwise SPI registers are available.
2) SPI response depends on **DCR.MUX** value. See **Chapter 9.5** for further details.
3) The undervoltage condition on V_S supply must be considered. See **Chapter 5.2.1** for further details.

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5.1 Operation modes

BTS54220-LBE has the following operation modes:

- Stand-by mode
- Idle mode
- Ready mode
- Operative mode
- Limp Home mode

The transition between operation modes is determined according to these variables:

- logic level at LHI pin
- logic level at INn pins
- **DCR.MUX** bits state
- **OUT.OUTn** bits state

The state diagram including the possible transitions is shown in **Figure 10**. The behavior of BTS54220-LBE as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S and V_{DD} supply voltages, some changes within the same operation mode can be seen accordingly.

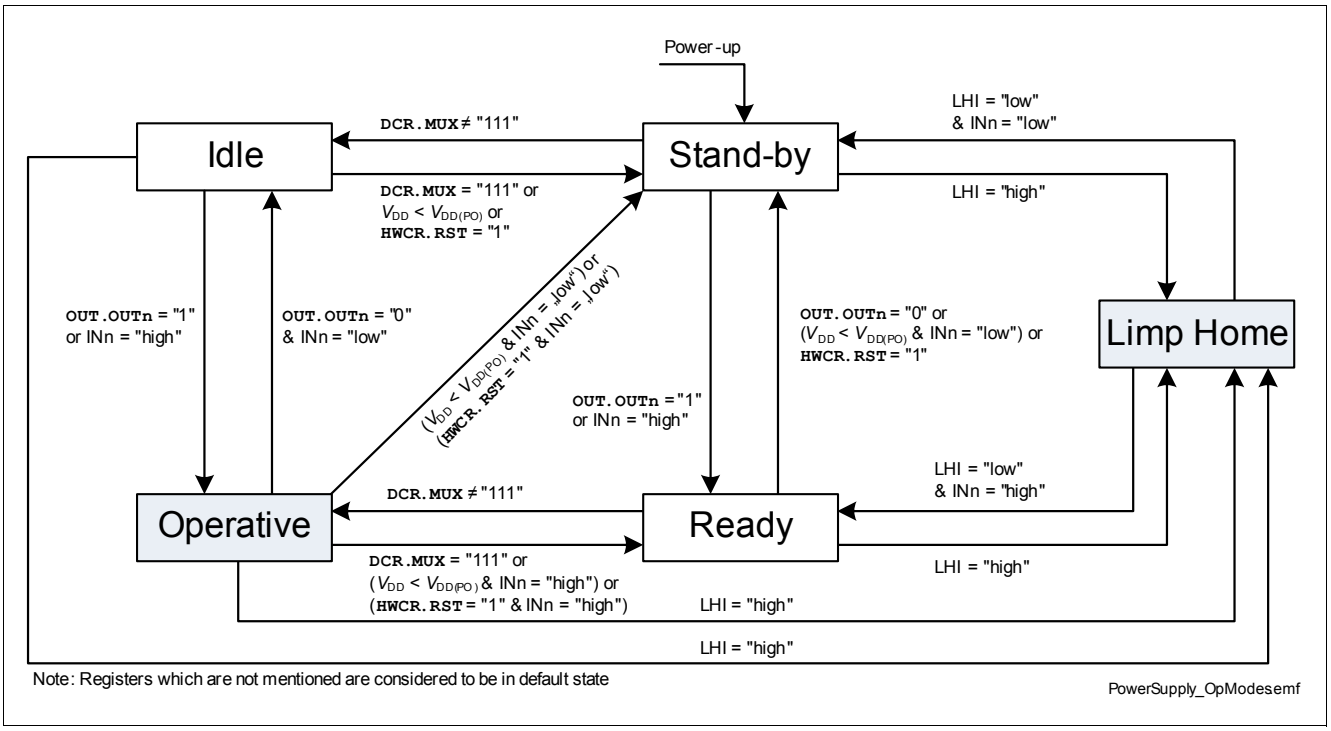


Figure 10 Operation Mode state diagram

There are three parameters describing the behavior of BTS54220-LBE:

- status of output channels
- status of SPI registers
- status of SPI communication

It is necessary to set **DCR.MUX** to a value different from 111_B to command a switch ON of one or more channels. In alternative it is necessary to set the LHI to “high” - in this case the logic state of the Input pins is reflected to the outputs (if there is no undervoltage condition on V_S supply).

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Table 5 shows the correlation between device operation modes, V_S and V_{DD} supply voltages, and the state of the most important functions (channel status, SPI communication and SPI registers).

Table 5 Device function in relation to operation modes, V_S and V_{DD} voltages

Operation Mode	Function	$V_S \le V_{SMON}$	$V_{SMON} > V_S \le V_{S(UV)}$	$V_S > V_{S(UV)}$
Stand-by	Channels	OFF	OFF	OFF
	SPI comm.	available[1)]	available[1)]	available[1)]
	SPI registers	available[1)]	available[1)]	available[1)]
Idle	Channels	OFF	OFF	OFF
	SPI comm.	all commands rejected[1)]	available[1)]	available[1)]
	SPI registers	available[1)]	available[1)]	available[1)]
Ready	Channels	OFF	OFF	OFF
	SPI comm.	available[1)]	available[1)]	available[1)]
	SPI registers	available[1)]	available[1)]	available[1)]
Operative	Channels	OFF	OFF	follow **OUT.OUTn** and/or Input pins
	SPI comm.	all commands rejected[1)]	available[1)]	available[1)]
	SPI registers	available[1)]	available[1)]	available[1)]
Limp Home	Channels	OFF	OFF	follow Input pins
	SPI comm.	available (read-only)[1)2)]	available (read-only)[1)2)]	available (read-only)[1)2)]
	SPI registers	reset	reset	reset

1) If $V_{DD} > V_{DD(PO)}$, otherwise not available or in reset.

2) **HWCR.CTC** and **HWCR.RST** commands are accepted.

5.1.1 Power-up

The Power-up condition is entered when one of the supply voltages (V_S or V_{DD}) is applied to the device. Both supplies are rising until they are above the undervoltage thresholds $V_{S(OP)}$ and $V_{DD(PO)}$ therefore the internal power-on signals are set.

5.1.2 Stand-by mode

When BTS54220-LBE is in Stand-by mode, all outputs are OFF. The SPI registers can be programmed if $V_{DD} > V_{DD(PO)}$. The current consumption is minimum (see parameter $I_{VS(STB)}$). The circuitry that monitors V_S versus the threshold V_{SMON} is disabled, allowing the programming of the registers. Even if one Input pin is set to “high” or if one **OUT.OUTn** bit is set to “1”, all outputs stay switched OFF.

5.1.3 Idle mode

In Idle mode, the internal supply circuitry is working and the device current consumption is increased. All channels are OFF and a command to switch ON one or more outputs (either via SPI or via Input pins) is accepted and executed, bringing the device into Operative mode.

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5.1.4 Ready mode

In Ready mode, one or more outputs received a command to switch ON (either via SPI or via Input pins). Nevertheless all outputs are OFF because of **DCR.MUX** bits still set to 111_B. It is necessary to change the value of those bits to bring the device into Operative mode and switch ON the channels.

5.1.5 Operative mode

Operative mode is the normal operation mode of BTS54220-LBE when no Limp Home condition is set and one or more outputs are switched ON. Device current consumption is specified by parameter I_{GND}. An undervoltage condition on V_{DD} supply voltage brings the device into Stand-by mode (if all Input pins are set to “low”) or into Ready mode (if at least one Input pin is set to “high”).

5.1.6 Limp Home mode

BTS54220-LBE enters Limp Home mode when LHI pin is set to “high”. SPI registers are reset to the default values after $t_{LHI(ac)}$ from the rising edge at pin LHI (see **Figure 11** for further details). SPI communication is possible but only in read-only mode (SPI registers can be read but cannot be written, meaning that current sensing is not available). When $V_S \leq V_{SMON}$ and **DCR.MUX** $\neq 111_B$ the logic state detected at pin LHI is ignored and the device doesn’t enter Limp Home mode.

*Note: The only write commands excepted in Limp Home mode are **HWCR.CTC** and **HWCR.RST** to clear the protection latches.*

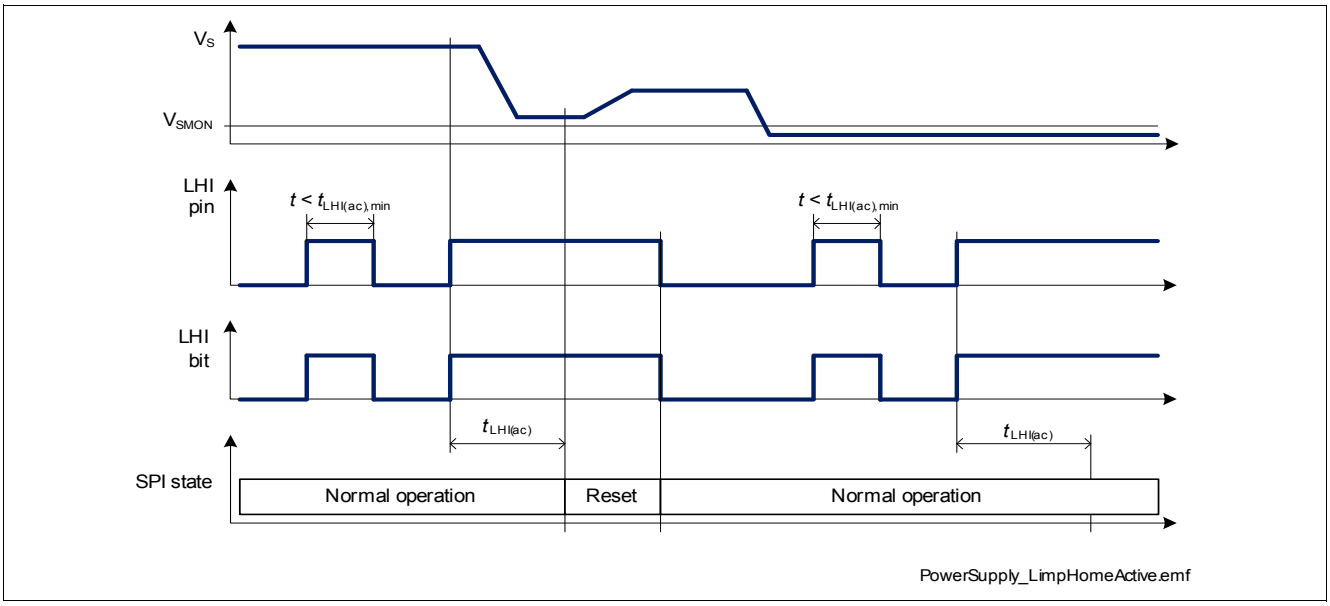


Figure 11 Limp Home Activation as function of V_S

5.2 Reset condition

One of the following 3 conditions resets the SPI registers to their default values:

- V_{DD} is not present or below the undervoltage threshold $V_{DD(PO)}$
- LHI pin is set to “high” and $V_S > V_{SMON}$
- a reset command (**HWCR.RST** = 1_B) is executed

In particular, all channels are switched OFF (if the device is not in Limp Home mode with one or more Input pins set to “high”). In case of lack of V_{DD} supply the internal retry counters are disabled therefore all channels are in “unlimited restart” mode.

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5.2.1 Undervoltage on V_S

Between $V_{S(OP)}$ and $V_{S(UV)}$ the undervoltage mechanism is triggered. If the device is operative and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the logic switches OFF the channels. As soon as the supply voltage V_S is above the minimum operative voltage threshold $V_{S(OP)}$, the channels having either the corresponding Input pin set to “high” or the `OUT.OUTn` bit set to “1” are switched ON again (as shown in **Figure 12**).

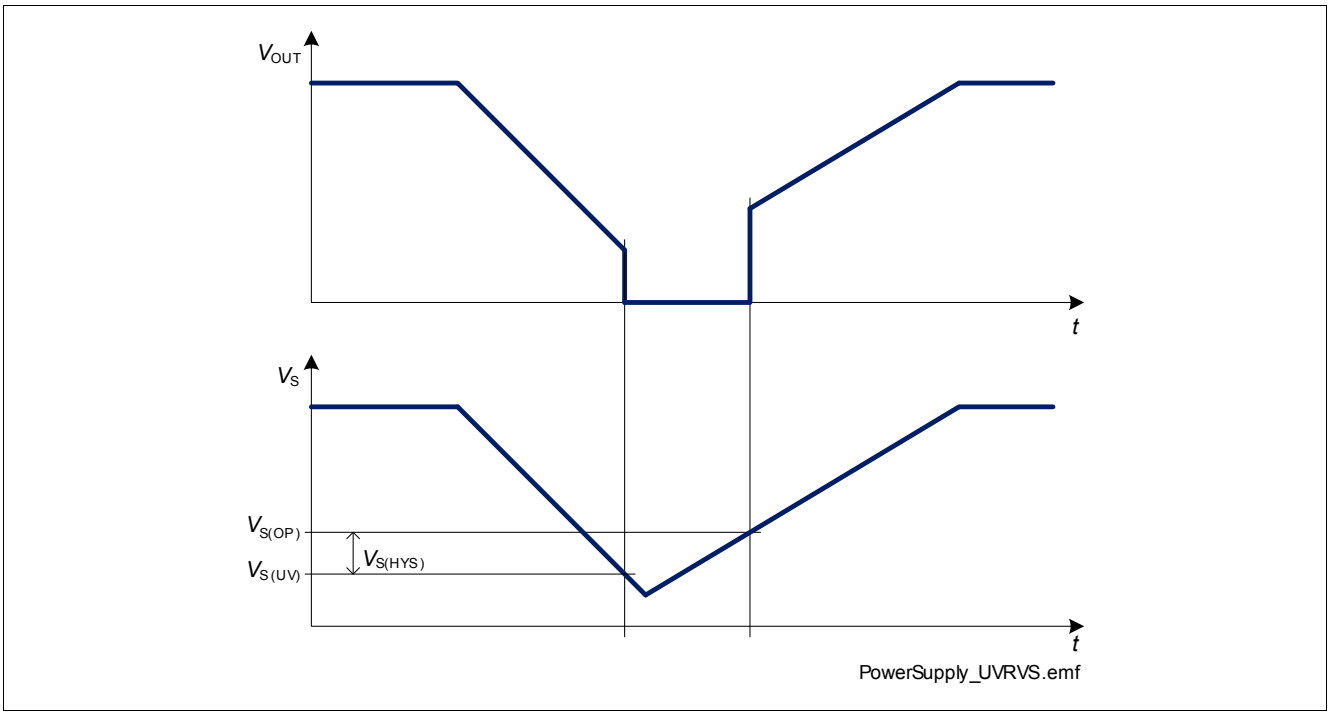


Figure 12 V_S undervoltage behavior

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5.3 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
Typical values: V_S = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

9 mΩ channels: R_L = 2.2 Ω

27 mΩ channels: R_L = 6.8 Ω (33 Ω when **LGCR.LEDn** = "1")

Table 6 Electrical Characteristics Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Operating voltage power switch	$V_{S(OP)}$	5.5	–	28[1)]	V	V_{DS} < 0.5 V	P_5.3.1
Undervoltage shutdown	$V_{S(UV)}$	–	–	4.5	V	OUTn = ON From V_{DS} < 1 V to I_{Ln} = 0 A (see **Figure 12**)	P_5.3.2
Undervoltage shutdown Hysteresis	$V_{S(HYS)}$	–	350	–	mV	[1)]	P_5.3.3
Stand-by current for whole device with loads	$I_{VS(STB)}$	–	0.1	1	µA	[1)] V_{DD} = 0 V V_{LHI} = 0 V T_j = 25 °C	P_5.3.7
Stand-by current for whole device with loads	$I_{VS(STB)}$	–	0.1	2.5	µA	[1)] V_{DD} = 0 V V_{LHI} = 0 V T_j = 85 °C	P_5.3.8
Stand-by current for whole device with loads	$I_{VS(STB)}$	–	8	20	µA	V_{DD} = 0 V V_{LHI} = 0 V T_j = 150 °C	P_5.3.9
Idle current for whole device with loads, all channels OFF	$I_{VS(idle)}$	–	2.25	5	mA	V_{DD} = 5 V **DCR.MUX** = 110_B	P_5.3.10
Operating current for whole device	I_{GND}	–	11	18	mA	f_{SCLK} = 0 MHz	P_5.3.11
V_S threshold for Limp Home validation	V_{SMON}	0.6	1.2	1.8	V	**VSMON** = 1	P_5.3.12
VDD pin							
Logic supply voltage	V_{DD}	3.8	–	5.5[1)]	V	f_{SCLK} = 3 MHz	P_5.3.13
Logic supply current Normal operation	I_{DD}	–	125	220	µA	f_{SCLK} = 0 MHz V_{CS} = V_{DD}= 5 V **DCR.MUX** ≠ 111_B	P_5.3.14
Logic Stand-by current	$I_{DD(STB)}$	–	35	70	µA	f_{SCLK} = 0 MHz V_{CS} = V_{DD}= 5 V **DCR.MUX** = 111_B	P_5.3.16

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Table 6 Electrical Characteristics Power Supply (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-On reset threshold voltage	$V_{DD(PO)}$	2.3	2.75	3.8	V	SI = 0 V SCLK = 0 V CS = 0 V SO from 0 to Z	P_5.3.17
LHI Input Characteristics							
L-input level at pin LHI	$V_{LHI(L)}$	-0.3	–	1.0	V	**LHI** = 1 (see **Chapter 9.6.1**)	P_5.3.18
H-input level at pin LHI	$V_{LHI(H)}$	2.6	–	6.0	V	–	P_5.3.19
L-input current through pin LHI	$I_{LHI(L)}$	3	27	75	µA	V_{LHI} = 1.0 V	P_5.3.20
H-input current through pin LHI	$I_{LHI(H)}$	7	30	75	µA	V_{LHI} = 2.6 V	P_5.3.21
Timings							
Power-On wake up time	$t_{WU(PO)}$	–	200	–	µs	1)	P_5.3.22
Limp Home acknowledgement time	$t_{LHI(ac)}$	5	–	30	µs	V_{DD} = 5 V polling of Standard Diagnosis (see **Chapter 9.6.1**) until **LHI** = **STB** = 1	P_5.3.23
Reset command delay time	$t_{d(RST)}$	–	–	100	µs	1)	P_5.3.25

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing at V_S = 13.5 V, V_{DD} = 4.3 V and T_j = 25 °C

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6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs with charge pumps. There are four channels implemented in the device. Each channel can be switched on via SPI register **OUT** or via an input pin, when available. Channels 2 and 3 provide a load type configuration for bulbs or LEDs in register **LGCR** (see **Chapter 9.7.4**). The load type configuration can be changed in ON- as well as in OFF-state.

6.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on the junction temperature T_j. **Figure 13** shows the variation of $R_{DS(ON)}$ across the whole temperature range. The value “1” corresponds to the typical $R_{DS(ON)}$ measured at T_J = 25°C.

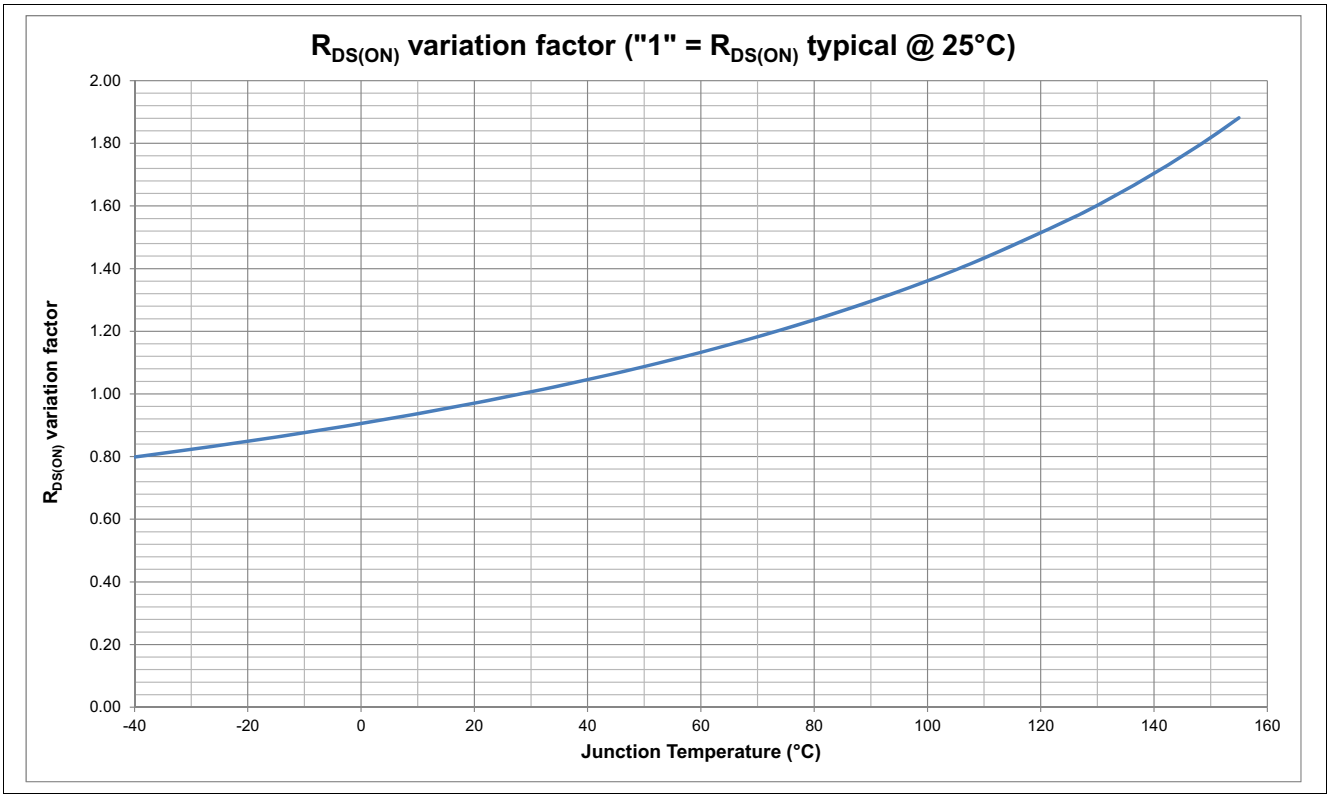


Figure 13 $R_{DS(ON)}$ variation factor

The behavior in reverse polarity mode is described in **Chapter 7**.

6.2 Input Circuit

There are two ways of using the input pins in combination with the register **OUT** by programming bit **HWCR.COL** in register **HWCR** (see **Chapter 9.7.6**).

- **HWCR.COL** = 0: A channel is switched ON either by the according **OUT.OUTn** bit or by the input pin.
- **HWCR.COL** = 1: A channel is switched ON by the according **OUT.OUTn** bit only, when the input pin is “high”. In this configuration, a PWM signal can be applied to the input pin and the channel is activated by the SPI register **OUT** (see **Chapter 9.7.1**).

The default state (**HWCR.COL** = 0) is the OR-combination of the input signal and the SPI-bit. In Limp Home Mode (LHI pin set to “high”) the combinatorial logic is switched to OR-mode to enable a channel activation via the input pins only.

Figure 14 shows the complete input switch matrix.

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The zener diode protects the input circuit against ESD pulses. The current sink to ground ensures that the input signal is low in case of an open input pin.

6.3 Input Status Monitor

The level of the input stage can be monitored via the input status monitor. The input status is indicated in the **OUT** register for the available input pin. After setting the bit **SWCR.SWR** = 1_B, the readout of **OUT.INSTn** shows the state of the input pins.

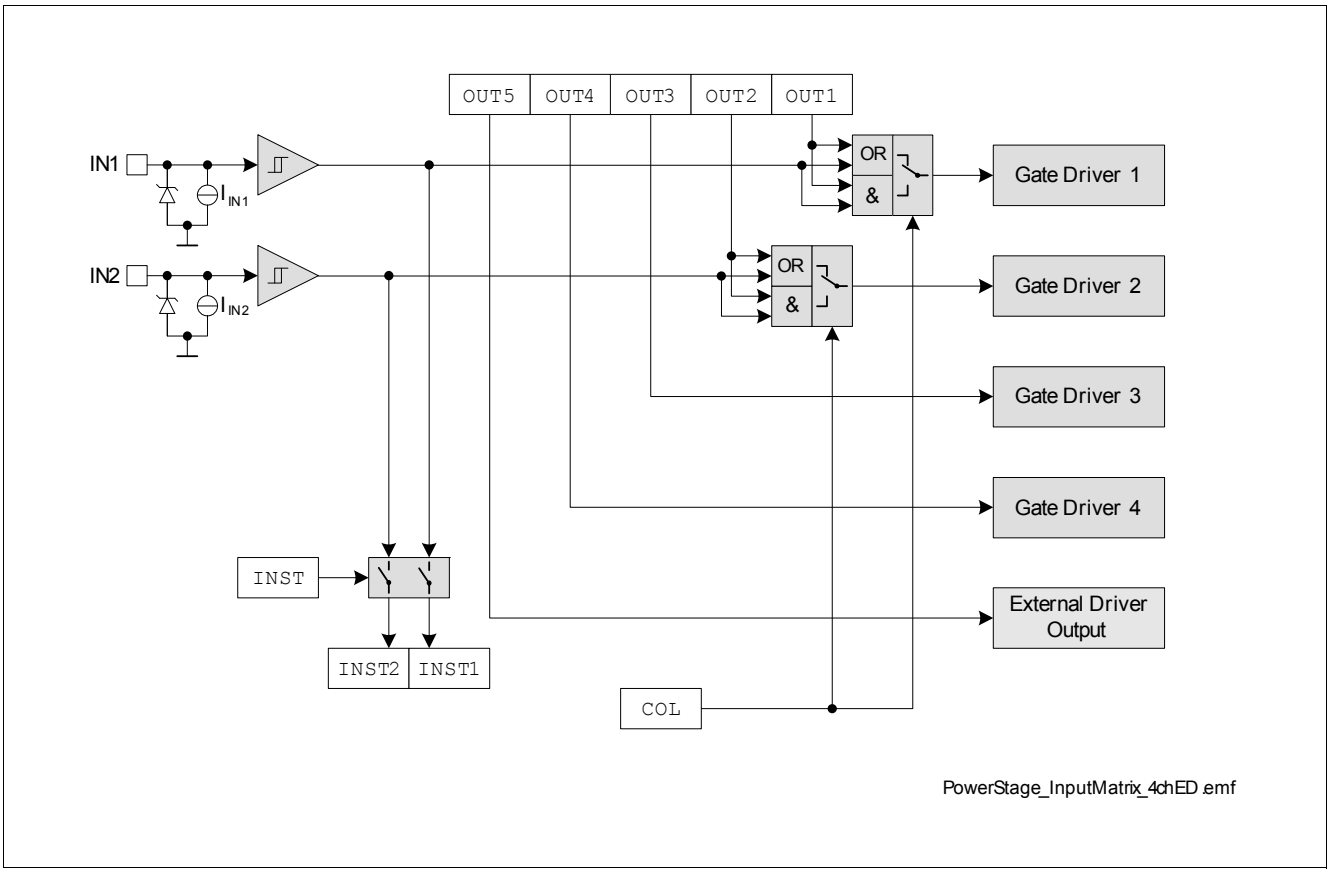


Figure 14 Input Switch Matrix

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6.4 Power Stage Output

The power stages are built to be used in high side configuration (**Figure 15**).

The power DMOS switches with a dedicated slope, which is optimized in terms of electromagnetic emission (EME). Defined slew rates allow lowest EME during PWM operation at low switching losses.

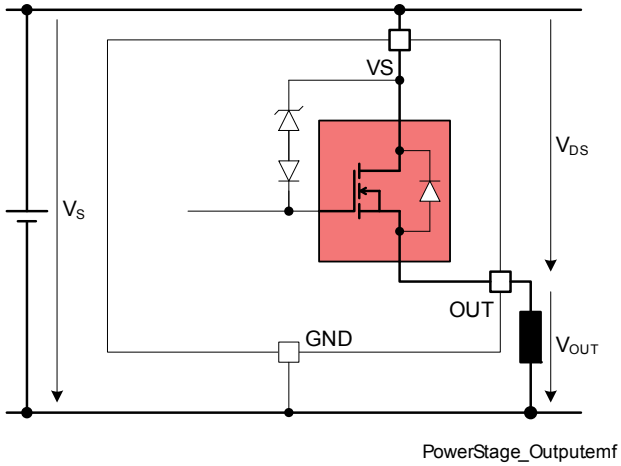


Figure 15 Power Stage Output

6.4.1 Bulb and LED Mode

Channel 2 and channel 3 can be configured in bulb and LED mode via the SPI initialization registers **LGCR** when **SWCR.SWR** = 0. The default state is **LGCR.LEDn** = 0. During LED mode the following parameters are changed for an optimized functionality with LED loads: ON-state resistance $R_{DS(ON)}$, switching timings ($t_{delay(ON)}$, $t_{delay(OFF)}$, t_{ON}, t_{OFF}), slew rates dV/dt_{ON} and dV/dt_{OFF}, load current protections $I_{L(LIM)}$ and current sense ratio k_{ILIS}.

6.4.2 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.

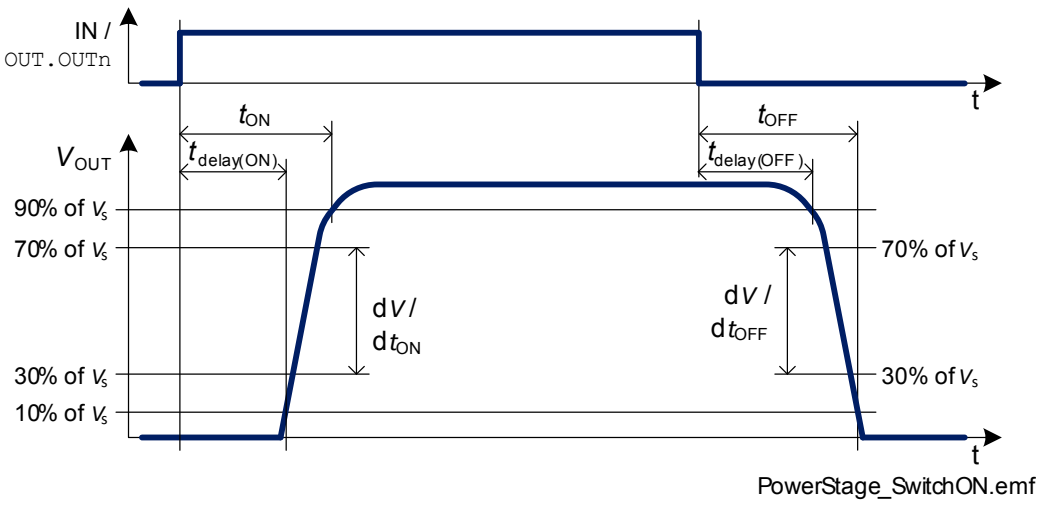


Figure 16 Switching a Load (resistive)

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6.4.3 Switching Inductive Loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, there is a voltage clamp mechanism implemented which limits that negative output voltage to a certain level ($V_{DS(CL)}$ (**Chapter 6.6**)). See **Figure 15** for details.Please refer also to **Chapter 7.4**. The maximum allowed load inductance is limited.

6.4.4 Switching Channels in Parallel

In case of appearance of a short circuit with channels in parallel driving a single load, BTS54220-LBE output stages are not synchronized in the restart event. When all channels connected to the same load are in temperature limitation, the channel which has cooled down the fastest doesn't wait for the other ones to be cooled down as well to restart. Thus, it is not recommended to use the device with channels in parallel.

Note: In case of parallel channel operation, short circuit robustness may be reduced and n_{RSC1} is not guaranteed any more.

6.5 External Driver Control

One external smart power driver can be driven by the BTS54220-LBE via the external driver control block. There are two control outputs available: one output for controlling the input (EDO) and one output for diagnosis enable input (EDD). The current sense output of the external smart power driver can be connected to the IS pin. For details please refer to **Chapter 10**.

The external driver output signals can be used only with applied V_{DD} voltage. The output is internally pulled down. The external driver can be activated via SPI bit `OUT.OUTn` with n = 5.

Note: The usable duty cycle range and diagnostic timings depend on the external driver's characteristics.

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6.6 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
Typical values: V_S = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

9 mΩ channels: R_L = 2.2 Ω

27 mΩ channels: R_L = 6.8 Ω (33 Ω when **LGCR.LEDn** = “1”)

Table 7 Electrical Characteristics Power Stages

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Characteristics							
On-State resistance 9 mΩ ch.	$R_{DS(ON)}$	–	9	–	mΩ	1) V_S = 9 V to 18 V I_L = 7.5 A T_j = 25 °C	P_6.6.1
On-State resistance 9 mΩ ch.	$R_{DS(ON)}$	–	–	18.2	mΩ	V_S = 9 V to 18 V I_L = 7.5 A T_j = 150 °C	P_6.6.2
On-State resistance 27 mΩ ch.	$R_{DS(ON)}$	–	27	–	mΩ	1) V_S = 9 V to 18 V I_L = 2.6 A T_j = 25 °C **LGCR.LEDn** = 0	P_6.6.5
On-State resistance 27 mΩ ch.	$R_{DS(ON)}$	–	–	55	mΩ	V_S = 9 V to 18 V I_L = 2.6 A T_j = 150 °C **LGCR.LEDn** = 0	P_6.6.6
On-State resistance 27 mΩ ch. in LED mode	$R_{DS(ON)}$	–	97	–	mΩ	1) V_S = 9 V to 18 V I_L = 0.6 A T_j = 25 °C **LGCR.LEDn** = 1	P_6.6.7
On-State resistance 27 mΩ ch. in LED mode	$R_{DS(ON)}$	–	–	195	mΩ	V_S = 9 V to 18 V I_L = 0.6 A T_j = 150 °C **LGCR.LEDn** = 1	P_6.6.8
Nominal load current 9 mΩ ch. (all channels active)	$I_{L(nom)}$	–	5	–	A	1) T_A = 85 °C T_j < 150 °C	P_6.6.15
Nominal load current 27 mΩ ch. (all channels active)	$I_{L(nom)}$	–	3	–	A	1) T_A = 85 °C T_j < 150 °C	P_6.6.16
Output clamp	$V_{DS(CL)}$	42	47	54	V	I_L = 20 mA	P_6.6.19

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Table 7 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current per channel $T_j \leq 85°C$ 9 mΩ ch.	$I_{L(OFF)}$	–	0.02	1.4	µA	[2] V_{IN} = 0 V or floating OUT.OUTn = 0 $T_j \leq 85°C$ Stand-by or Idle mode	P_6.6.20
Output leakage current per channel $T_j \leq 85°C$ 27 mΩ ch.	$I_{L(OFF)}$	–	0.02	0.5	µA	[2] V_{IN} = 0 V or floating OUT.OUTn = 0 $T_j \leq 85°C$ Stand-by or Idle mode	P_6.6.21
Output leakage current per channel T_j = 150°C 9 mΩ ch.	$I_{L(OFF)}$	–	6	18	µA	V_{IN} = 0 V or floating OUT.OUTn = 0 T_j = 150°C Stand-by or Idle mode	P_6.6.24
Output leakage current per channel T_j = 150°C 27 mΩ ch.	$I_{L(OFF)}$	–	1.7	6	µA	V_{IN} = 0 V or floating OUT.OUTn = 0 T_j = 150°C Stand-by or Idle mode	P_6.6.25
Input Characteristics							
L-input level	$V_{IN(L)}$	-0.3	–	1.0	V	–	P_6.6.28
H-input level	$V_{IN(H)}$	2.6	–	6.0	V	–	P_6.6.29
L-input current	$I_{IN(L)}$	3	27	75	µA	V_{IN} = 1.0 V	P_6.6.30
H-input current	$I_{IN(H)}$	7	30	75	µA	V_{IN} = 2.6 V	P_6.6.31
Timings							
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) 9 mΩ ch.	$t_{delay(ON)}$	30	75	140	µs	V_S = 13.5 V T_j = -40 °C	P_6.6.32
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) 9 mΩ ch.	$t_{delay(ON)}$	–	45	–	µs	[1] V_S = 13.5 V T_j = 25 °C	P_6.6.96
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) 9 mΩ ch.	$t_{delay(ON)}$	15	30	55	µs	V_S = 13.5 V T_j = 150 °C	P_6.6.97
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) 27 mΩ ch.	$t_{delay(ON)}$	10	30	70	µs	V_S = 13.5 V LGCR.LEDn = 0	P_6.6.34

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Table 7 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn-ON delay to 10% V_S (Logical propagation delay from input INn to output OUTn) 27 mΩ ch. in LED mode	$t_{delay(ON)}$	3	10	25	µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.35
Turn-OFF delay to 90% V_S (Logical propagation delay from input INn to output OUTn) 9 mΩ ch.	$t_{delay(OFF)}$	20	50	100	µs	V_S = 13.5 V	P_6.6.39
Turn-OFF delay to 90% V_S (Logical propagation delay from input INn to output OUTn) 27 mΩ ch.	$t_{delay(OFF)}$	10	30	70	µs	V_S = 13.5 V **LGCR.LEDn** = 0	P_6.6.41
Turn-OFF delay to 90% V_S (Logical propagation delay from input INn to output OUTn) 27 mΩ ch. in LED mode	$t_{delay(OFF)}$	3	10	25	µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.42
Turn-ON time to 90% 9 mΩ ch.	t_{ON}	45	95	170	µs	V_S = 13.5 V T_j = -40 °C	P_6.6.46
Turn-ON time to 90% V_S 9 mΩ ch.	t_{ON}	–	65	–	µs	[1] V_S = 13.5 V T_j = 25 °C	P_6.6.100
Turn-ON time to 90% V_S 9 mΩ ch.	t_{ON}	30	55	90	µs	V_S = 13.5 V T_j = 150 °C	P_6.6.101
Turn-ON time to 90% V_S 27 mΩ ch.	t_{ON}	30	75	180	µs	V_S = 13.5 V **LGCR.LEDn** = 0	P_6.6.48
Turn-ON time to 90% V_S 27 mΩ ch. in LED mode	t_{ON}	10	25	55	µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.49
Turn-OFF time to 10% V_S 9 mΩ ch.	t_{OFF}	30	70	120	µs	V_S = 13.5 V	P_6.6.53
Turn-OFF time to 10% V_S 27 mΩ ch.	t_{OFF}	30	85	180	µs	V_S = 13.5 V **LGCR.LEDn** = 0	P_6.6.55
Turn-OFF time to 10% V_S 27 mΩ ch. in LED mode	t_{OFF}	10	30	55	µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.56

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Table 7 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn-ON/OFF matching 9 mΩ ch.	t_{ON} - t_{OFF}	-20	25	80	µs	V_S = 13.5 V T_j = -40°C	P_6.6.60
Turn-ON/OFF matching 9 mΩ ch.	t_{ON} - t_{OFF}	–	-5	–	µs	[1] V_S = 13.5 V T_j = 25°C	P_6.6.61
Turn-ON/OFF matching 9 mΩ ch.	t_{ON} - t_{OFF}	-50	-20	10	µs	V_S = 13.5 V T_j = 150°C	P_6.6.62
Turn-ON/OFF matching 27 mΩ ch.	t_{ON} - t_{OFF}	-50	-10	30	µs	V_S = 13.5 V **LGCR.LEDn** = 0	P_6.6.66
Turn-ON/OFF matching 27 mΩ ch. in LED mode	t_{ON} - t_{OFF}	-25	-5	15	µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.67
Turn-ON slew rate 30% to 70% V_S 9 mΩ ch.	dV/ dt_{ON}	0.3	0.6	0.9	V/µs	V_S = 13.5 V	P_6.6.71
Turn-ON slew rate 30% to 70% V_S 27 mΩ ch.	dV/ dt_{ON}	0.1	0.25	0.5	V/µs	V_S = 13.5 V **LGCR.LEDn** = 0	P_6.6.73
Turn-ON slew rate 30% to 70% V_S 27 mΩ ch. in LED mode	dV/ dt_{ON}	0.35	0.88	1.75	V/µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.74
Turn-OFF slew rate 70% to 30% V_S 9 mΩ ch.	-dV/dt_{OFF}	0.3	0.6	0.9	V/µs	V_S = 13.5 V	P_6.6.78
Turn-OFF slew rate 70% to 30% V_S 27 mΩ ch.	-dV/dt_{OFF}	0.1	0.25	0.5	V/µs	V_S = 13.5 V **LGCR.LEDn** = 0	P_6.6.80
Turn-OFF slew rate 70% to 30% V_S 27 mΩ ch. in LED mode	-dV/dt_{OFF}	0.35	0.88	1.75	V/µs	V_S = 13.5 V **LGCR.LEDn** = 1	P_6.6.81
External Driver Control							
L level external driver output voltage	$V_{EDO(L)}$	0	–	0.5	V	I_{EDO} = -0.2 mA	P_6.6.85
H level external driver output voltage	$V_{EDO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{EDO} = 0.2 mA V_{DD} = 4.3 V	P_6.6.86
External driver output enable time	$t_{EDO(en)}$	–	–	4	µs	[1] C_L = 50 pF	P_6.6.87
External driver output disable time	$t_{EDO(dis)}$	–	–	4	µs	[1] C_L = 50 pF	P_6.6.88
L level external driver diagnosis enable voltage	$V_{EDD(L)}$	0	–	0.5	V	I_{EDD} = -0.2 mA	P_6.6.89
H level external driver diagnosis enable voltage	$V_{EDD(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{EDD} = 0.2 mA V_{DD} = 4.3 V	P_6.6.90

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Table 7 Electrical Characteristics Power Stages (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
External driver diagnosis enable enable time	$t_{EDD(en)}$	–	–	4	µs	1) C_L = 50 pF	P_6.6.91
External driver diagnosis enable disable time	$t_{EDD(dis)}$	–	–	4	µs	1) C_L = 50 pF	P_6.6.92
Output Voltage Drop							
Output voltage drop limitation at small load currents All channels	$V_{DS(NL)}$	-	10	25	mV	I_L = 50 mA `LGCR.GBRn` = 1	P_6.6.93

1) Not subject to production test, specified by design.

2) Tested at T_j = -40 °C

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7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

7.1 Over Load Protection

The load current I_L is limited by the device itself in case of over load or short circuit to ground. All channels have 2 steps of current limitation which are selected automatically depending on the voltage V_{DS} across the power DMOS as show in **Figure 17**. Please note that $V_{OUT} = V_S - V_{DS}$. The current limitation threshold when V_{DS} = 5 V is taken as reference.

Current limitation to the value $I_{L(LIM)}$ is realized by increasing the resistance of the output channel, which leads to fast DMOS temperature rise.

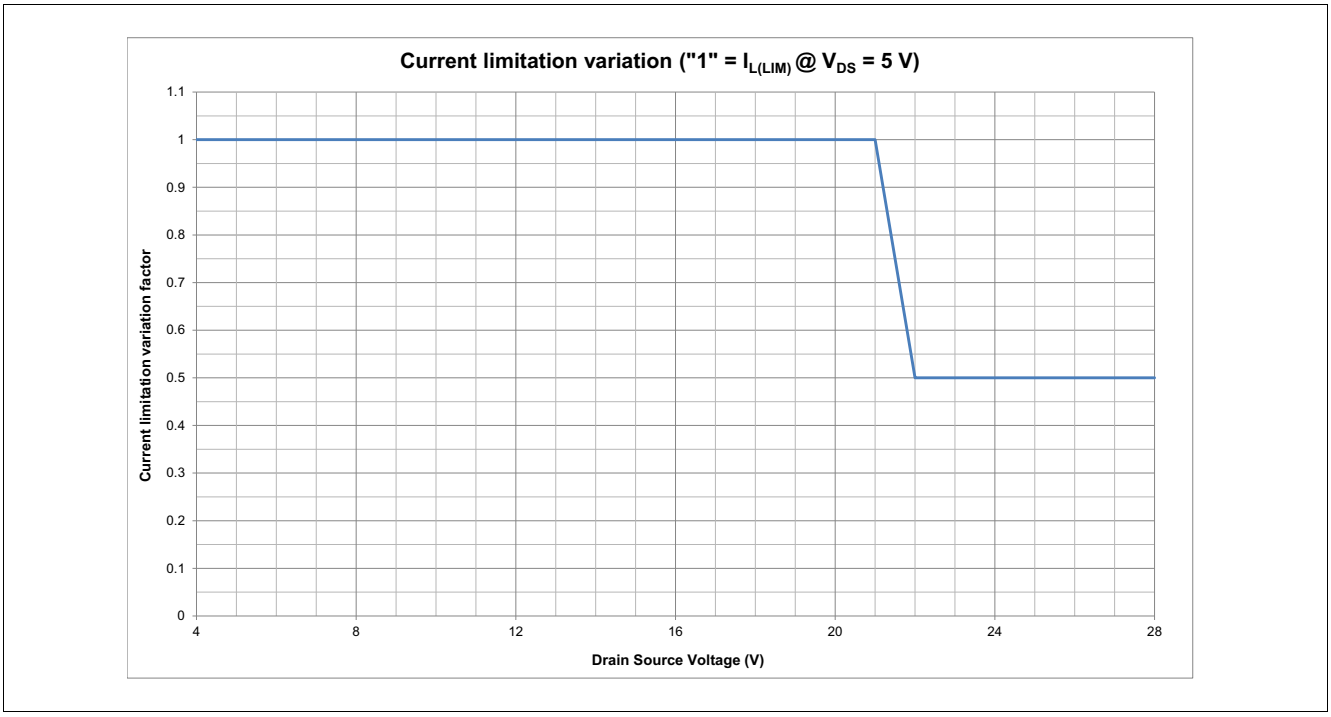


Figure 17 Typical Current Limitation variation according to V_{DS} voltage

7.2 Over Temperature Protection

Each channel incorporates both an absolute ($T_{j(SC)}$) and a dynamic ($\Delta T_{j(SW)}$) temperature sensor. An increase of junction temperature T_j above one of the two thresholds ($T_{j(SC)}$ or $\Delta T_{j(SW)}$) switches OFF an overheated channel to prevent destruction. Any protective switch OFF deactivates the output until the temperature has reached an acceptable value.

Each protective switch OFF event increments the error counter by one. The number of automatic reactivations is limited by n_{retry}. If this number of retries is reached the channel turns OFF and latches OFF.

The error information related to the given channel is available on the Standard Diagnosis and Errors Diagnosis. Executing **HWCR.CTC** = 1_B will clear all thermal counters and errors on all channels. If the channel is active (either **OUT.OUTn** = 1_B or INn = “high” and **DCR.MUX** ≠ 111_B) it is turned on immediately after the SPI command. In addition the execution of the reset command (**HWCR.RST** = 1_B) will clear the thermal counters.

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For the condition $n < n_{retry}$ the counter of automatic reactivations is reset by every channel activation if **HWCR.RCR** bit is set to 1. In **Figure 20** the different behavior of retry counters according to **HWCR.RCR** bit value can be seen.

In Limp Home Mode, the thermal counters of the protection functions are only operative if V_{DD} is provided in the specified range. Otherwise the counters are not active and all channels are in „unlimited restart“ mode.

In case of the short circuit to ground, current sense ratio (k_{ILIS}) is deactivated as soon as $V_{DS} > V_{DS(SB)}$ (Switch bypass monitor threshold). Usually a short circuit to ground condition tends to set $V_{DS} = V_S$ therefore in most of the cases no current sensing diagnostic is possible in short circuit.

The error information related to the given channel are available also on Warnings Diagnosis (**ERRn** bits).

Refer to **Figure 18** and **Figure 19** for details.

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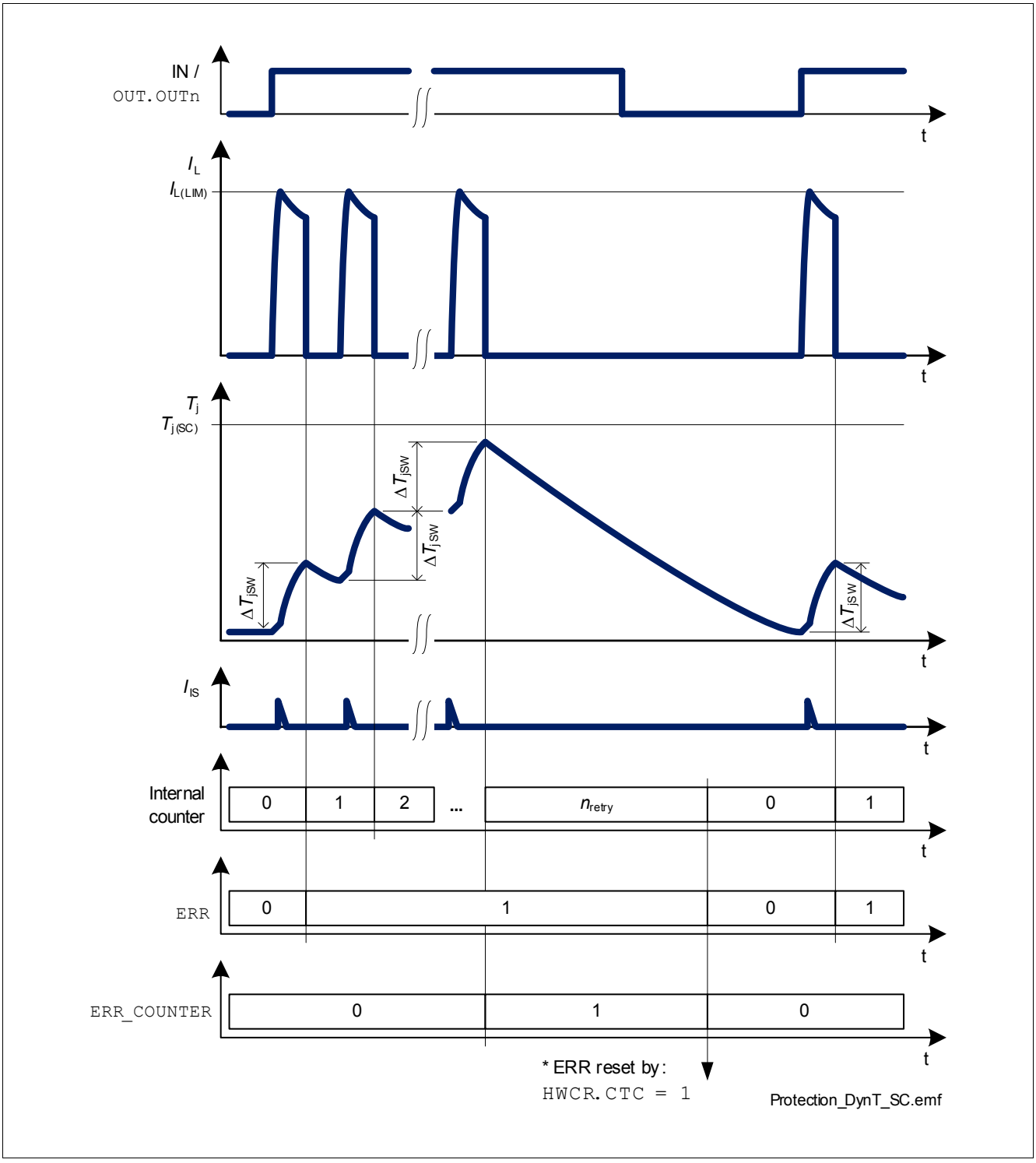


Figure 18 Dynamic Temperature Sensor Operations - Short Circuit

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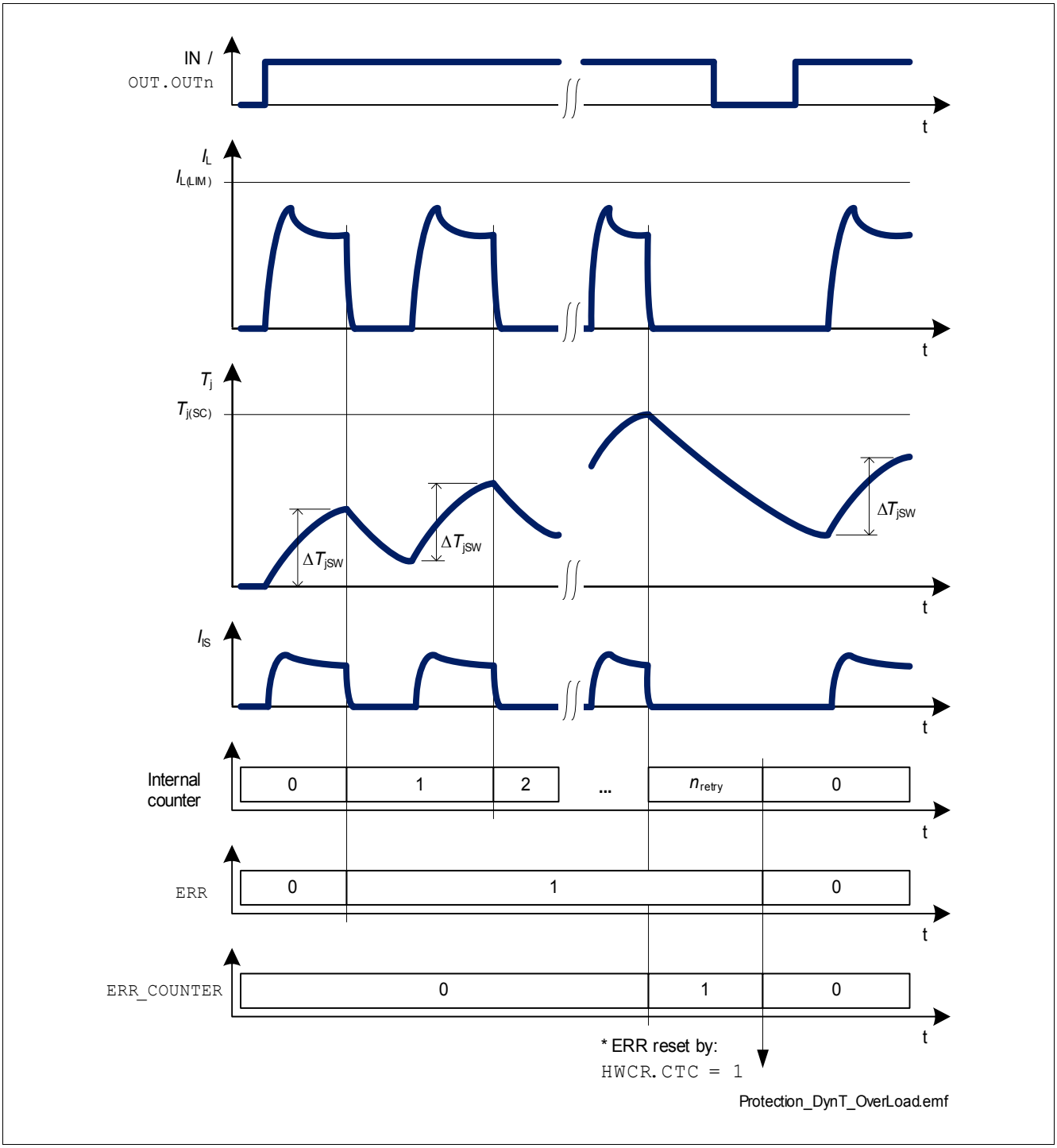


Figure 19 Dynamic and Absolute Temperature Sensor Operations - Overload Condition

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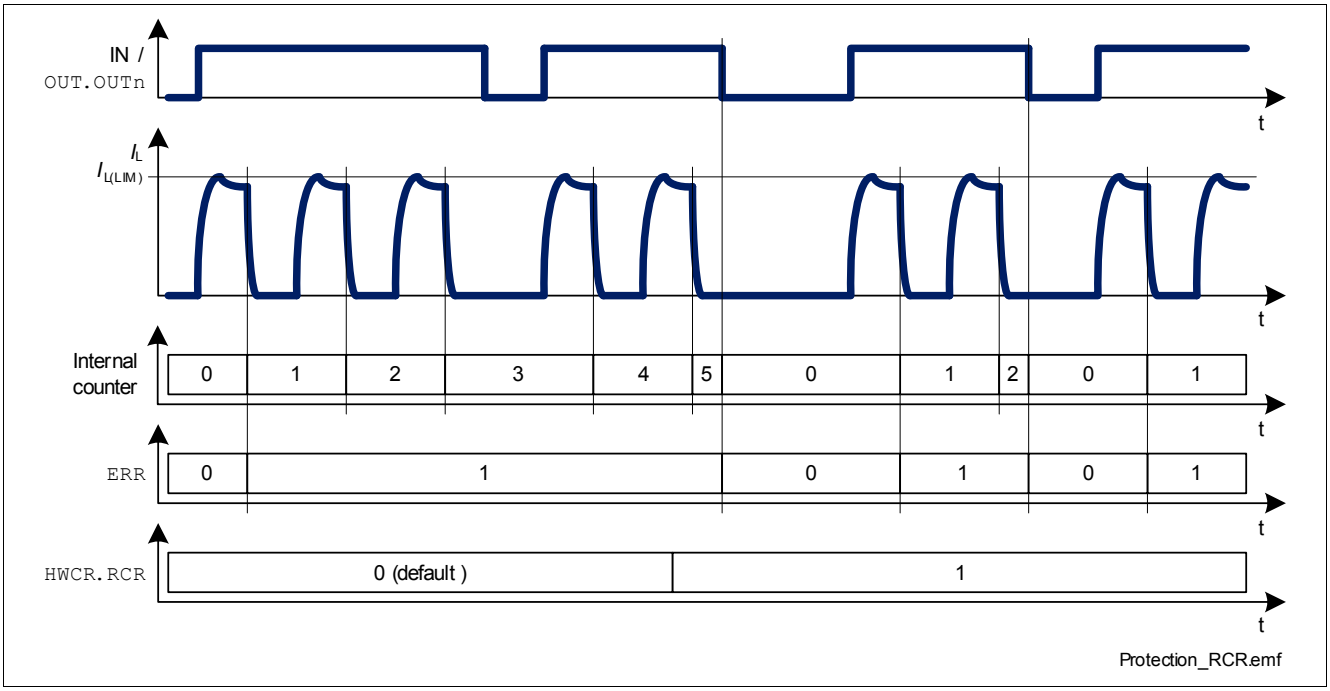


Figure 20 Different counter reset according to HWCR.RCR bit value

7.3 Reverse Polarity Protection

In reverse polarity condition, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads.The current through ground pin GND, sense pin IS, logic power supply pin VDD, SPI pins, input pins, external driver pins and Limp Home Input pin has to be limited as well (please refer to the maximum ratings listed on **Chapter 4.1**).

Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.

7.4 Over Voltage Protection

In the case of supply voltages between $V_{S(SC)max}$ and $V_{S(AZ)}$ the output transistors are still operational and follow the input or the **OUT** register. Parameters are not warranted and lifetime is reduced compared to nominal voltage supply.

In addition to the output clamp for inductive loads as described in **Chapter 6.4.3**, there is a clamp mechanism available for over voltage protection for the logic and all channels.

7.5 Loss of Ground

In case of complete loss of the device ground connection, but loads connected to ground, the BTS54220-LBE securely changes to or stays in OFF-state. Please refer to **Chapter 10** where an application setup is described.

7.6 Loss of V_S

In case of loss of V_S connection in ON-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from V_S to ground. For example, a suppressor diode is recommended between V_S and GND.

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7.7 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_S = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

9 mΩ channels: R_L = 2.2 Ω

27 mΩ channels: R_L = 6.8 Ω (33 Ω when **LGCR.LEDn** = “1”)

Table 8 Electrical Characteristics Protection Functions

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Over Load Protection							
Load current limitation 9 mΩ ch.	$I_{L(LIM)}$	63	82	99	A	1) V_{DS} = 5 V	P_7.7.1
Load current limitation 9 mΩ ch.	$I_{L(LIM)}$	–	41	–	A	1) V_{DS} = 26 V	P_7.7.2
Load current limitation 27 mΩ ch.	$I_{L(LIM)}$	30	42	56	A	1) V_{DS} = 5 V **LGCR.LEDn** = 0	P_7.7.5
Load current limitation 27 mΩ ch.	$I_{L(LIM)}$	–	21	–	A	1) V_{DS} = 26 V **LGCR.LEDn** = 0	P_7.7.6
Load current limitation 27 mΩ ch. in LED mode	$I_{L(LIM)}$	9.5	12	17	A	V_{DS} = 5 V T_j = -40 °C **LGCR.LEDn** = 1	P_7.7.7
Load current limitation 27 mΩ ch. in LED mode	$I_{L(LIM)}$	–	5	–	A	1) V_{DS} = 26 V **LGCR.LEDn** = 1	P_7.7.8
Over Temperature Protection							
Thermal shut down temperature	$T_{j(SC)}$	150	170	200	°C	1)	P_7.7.14
Thermal hysteresis of thermal shutdown	$\Delta T_{j(SC)}$	–	20	–	K	1)	P_7.7.15
Dynamic temperature increase limitation while switching	$\Delta T_{j(SW)}$	–	80	–	K	1)	P_7.7.16
Number of automatic retries at dynamic temperature sensor or over temperature shut down	n_{retry}	–	8	9		1)	P_7.7.17
Reverse Polarity							
Drain source diode voltage during reverse polarity 9 mΩ ch.	$V_{DS(REV)}$	400	600	740	mV	$I_L = I_{L(nom)}$ = P_6.6.15 T_j = 150 °C	P_7.7.18

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Table 8 Electrical Characteristics Protection Functions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Drain source diode voltage during reverse polarity 27 mΩ ch.	$V_{DS(REV)}$	400	650	800	mV	$I_L = I_{L(nom)}$ = P_6.6.16 T_j = 150 °C	P_7.7.19
Over Voltage							
Overvoltage protection	$V_{S(AZ)}$	42	47	54	V	I_S = 4 mA	P_7.7.22

1) Not subject to production test, specified by design.

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8 Diagnosis

For diagnosis purpose, the BTS54220-LBE provides a current sense signal at pin IS and a diagnosis word via SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage.

Please refer to **Figure 21** for details.

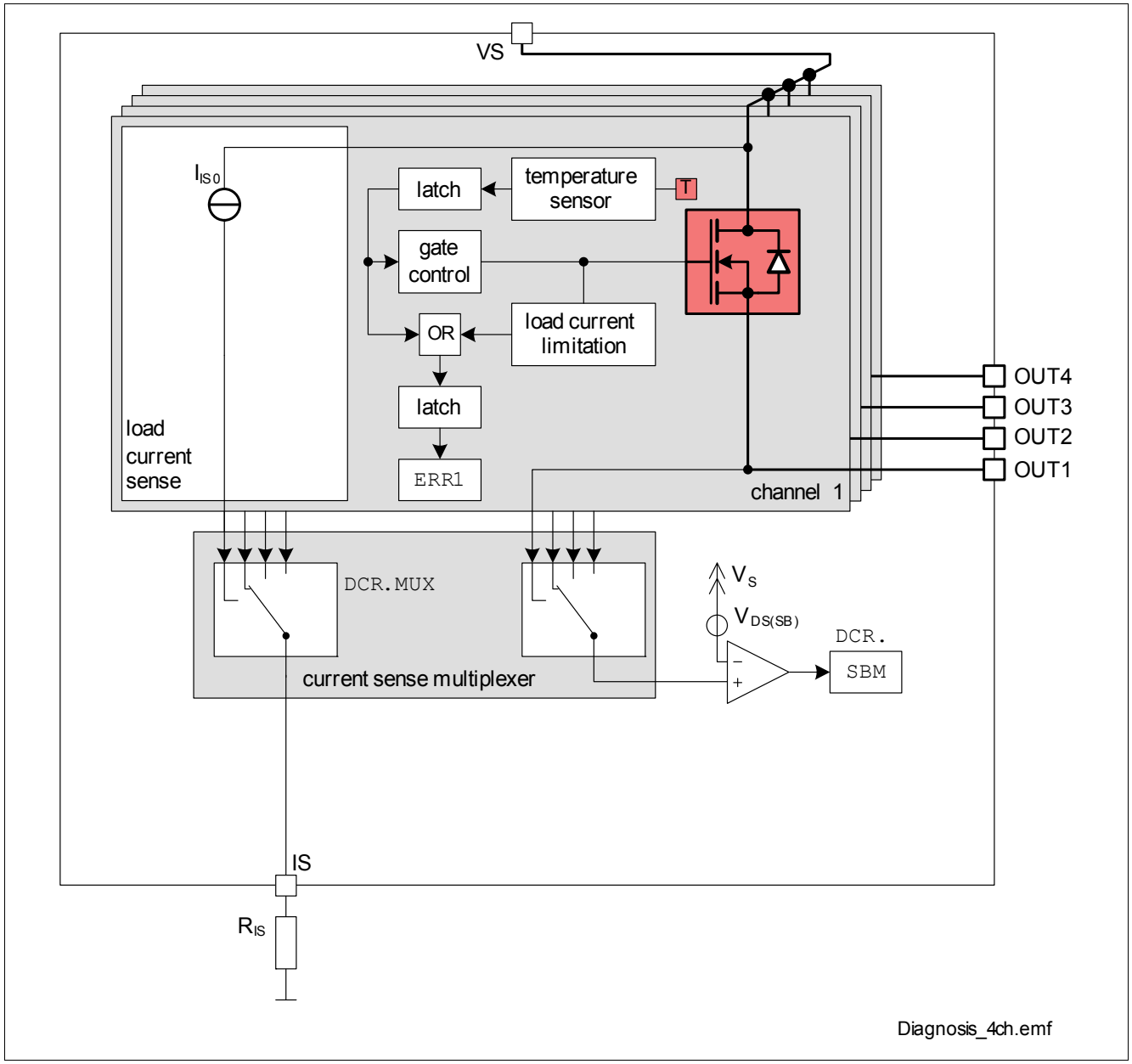


Figure 21 Block Diagram: Diagnosis

For diagnosis feedback at different operation modes, please see **Table 9**.

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Table 9 Operation Modes [1]

Operation Mode	Input Level OUT.OUTn	Output Level V_{OUT}	Current Sense I_{IS}	Error Flag ERR_COUNTERn[2]	Warning Flag ERRn[3]	DCR.SBM bit
Normal Operation (**Channel OFF**)	L / 0 (OFF-state)	GND	Z	0	0	1
Short Circuit to GND		GND	Z	0	0	1
Thermal shut down		Z	Z	0[2]	0[2]	X
Short Circuit to V_S		V_S	Z	0	0	0
Open Load		Z	Z	0	0	X
Normal Operation (**Channel ON**)	H / 1 (ON-state)	~V_S	I_L / k_{ILIS}	0	0	0
Current Limitation		< V_S	Z	0	0	X
Dynamic or Absolute Thermal Limitation → Channel switched OFF		Z	Z	0	1	X
Dynamic or Absolute Thermal Limitation n_{retry} reached → Channel latched OFF		Z	Z	1[2]	1	X
Short Circuit to GND		~GND	Z	0	0	1
Short Circuit to V_S		V_S	< I_L / k_{ILIS}	0	0	0
Open Load		V_S	Z	0	0	0

1) L = “low” level, H = “high” level, Z = high impedance, potential depends on leakage currents and external circuit. X = undefined.

2) The over temperature flag is set latched and can be cleared by setting HWCR.CTC = 1_B.

3) The warning flags are latched until they are reset (see HWCR.RCR description).

8.1 Diagnosis Word at SPI

Diagnostic information about the status of each channel is provided through SPI. In the Standard Diagnosis the ERR_MUX bit reports if there is a channel which had already enough restarts to reach the maximum allowed number of retries n_{retry} (P_7.7.17). If 2 or more channels are latched OFF due to that, ERR_MUX bits aren't enough to identify which channels are OFF. In such cases, it is possible to get an overview channel by channel using ERR_COUNTERn bits in Errors Diagnosis (see **Chapter 9.6.2**)

It is possible to check if one or more channels had some retries during switching ON, although the limit of n_{retry} was not reached. An overview channel by channel of thermal counter status is available using ERRn bits in Warnings Diagnosis (see **Chapter 9.6.3**).

For both ERR_COUNTERn and ERRn the information on channel n is given at bit n-1 (e.g. bit 0 indicates status of channel 1).

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8.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

8.2.1 Current Sense Signal

The current sense signal (ratio $k_{ILIS} = I_L / I_S$) is provided during ON-state as long as no failure mode occurs. For dedicated channels the ratio k_{ILIS} can be adjusted to the load type (LED or bulb) via SPI register **LGCR**. The accuracy of the ratio k_{ILIS} depends on the load current and temperature. Usually a resistor R_{IS} is connected to the current sense pin. It is recommended to use resistors 1.5 kΩ < R_{IS} < 5 kΩ. A typical value is 2.7 kΩ.

The current sense signal of a channel is not active when the channel is OFF or when the protection functions (current limitation, over temperature or dynamic temperature sensors) are active. If the maximum number of automatic reactivations n_{retry} is reached ($n = n_{retry}$), the current sense signal of the affected channel is deactivated until the reset of the counters by setting **HWCR.CTC** bit to 1.

Details about timings between the current sense signal I_{IS} and the output voltage V_{OUT} and the load current I_L can be found in **Figure 22**.

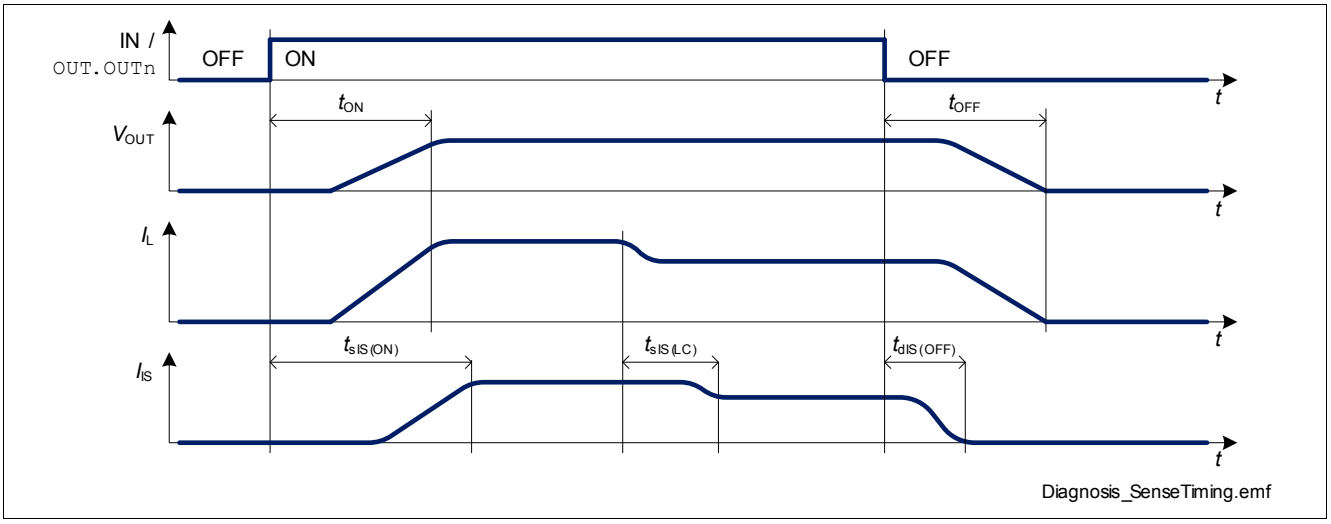


Figure 22 Current Sense Signal Timings

8.2.2 Current Sense Multiplexer

There is a current sense multiplexer implemented in the BTS54220-LBE that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register **DCR.MUX**. The sense current can also be disabled by SPI register **DCR.MUX**. For details on timing of the current sense multiplexer, please refer to **Figure 23**.

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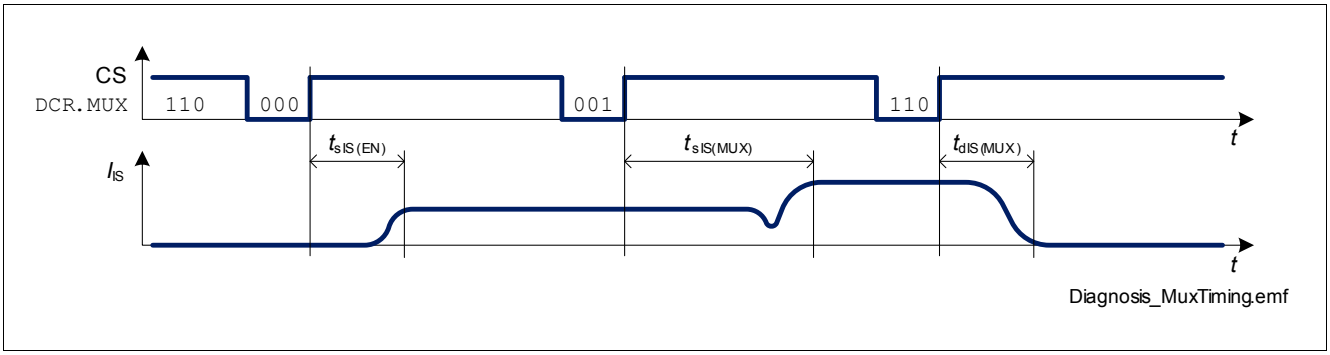


Figure 23 Current Sense Multiplexer Timings

8.2.3 Open Load at ON Diagnosis

If a channel is ON in Open Load condition, a small current can still flow, for example because of humidity. The parameter $I_{L(OL)}$ gives the threshold of recognition for such leakage current. If the voltage measured at the sense resistor R_{SENSE} corresponds to a current $I_{IS(OL)}$ (4 µA), then the current flowing at the output in ON state is within the limits given by $I_{L(OL)}$. **Figure 24** shows the sense current behavior once a channel in Open Load at ON condition is selected with the sense current multiplexer. The red curve show a typical product curve. The blue line shows the ideal k_{ILIS} ratio.

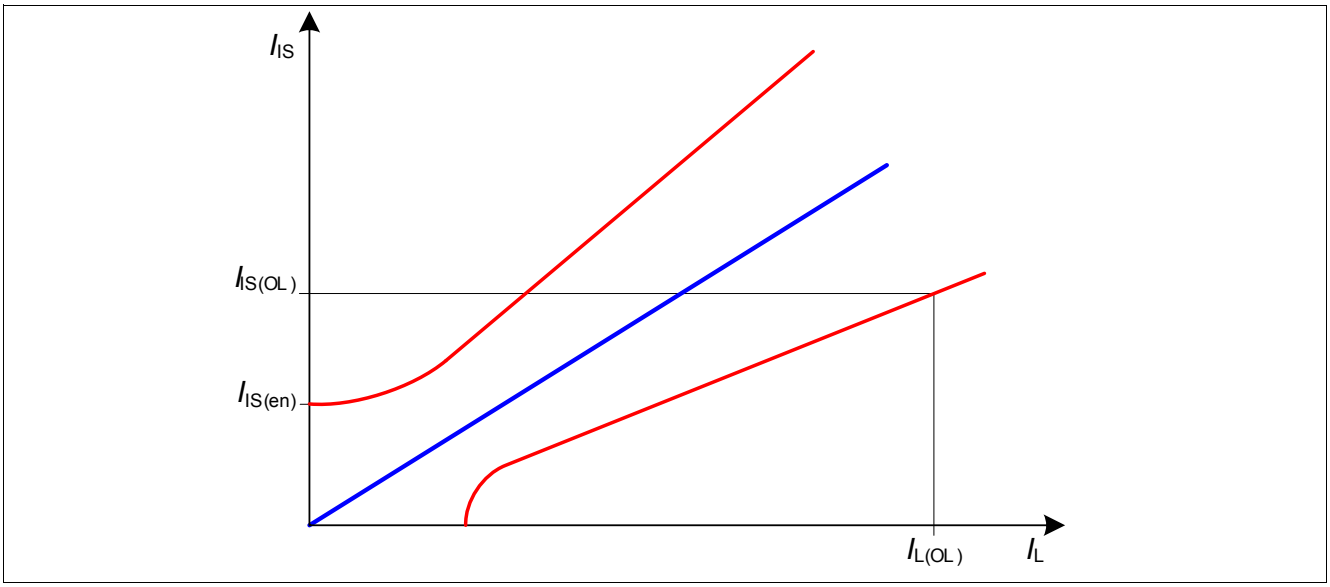


Figure 24 Current Sense Ratio in Open Load at ON condition

8.3 Switch Bypass Monitor Diagnosis

To detect short circuit to V_S, there is a switch bypass monitor implemented. In case of short circuit between the output pin OUT and VS in ON-state, the current flows through the power transistor as well as through the short circuit (bypass) with undefined share between the two. As a result, the current sense signal shows lower values than expected by the load current. In OFF-state, the output voltage remains close to V_S potential which leads to a small V_{DS}.

The switch bypass monitor compares the threshold $V_{DS(SB)}$ with the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (**DCR.MUX**). The result of the comparison can be read in SPI register **DCR.SBM**.

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8.4 Gate Back Regulation

To increase the current sense accuracy, the Gate Back Regulation (GBR) function is implemented. This function monitors the V_{DS} voltage at the output and if the value is equal to or lower than $V_{DS(NL)}$ the output DMOS gate is partially discharged. This increases output DMOS resistance so that V_{DS} = $V_{DS(NL)}$ even for very small output currents. The V_{DS} increase allows the current sensing circuitry to work with better accuracy, providing tighter k_{ILIS} values for output currents in the low range.

This function is active by default (**LGCR.GBRn** bits set to “1” after a reset). According to output current, GBR function can be left active or disabled. Even if left active, Gate Back Regulation circuitry may not be working because the measured V_{DS} is bigger than $V_{DS(NL)}$ (depending on output current, junction temperature, output DMOS resistance).

Due to production and temperature variations, GBR circuitry can affect kILIS performance in negative way for some output current values. For this reason, **Table 10** and **Table 11** indicate for which output currents it is necessary to deactivate GBR (setting the corresponding **LGCR.GBRn** bit to “0”) to reach the desired current accuracy. If no indication is given, then the GBR function is assumed to be enabled (**LGCR.GBRn** bit set to “1”). It is recommended to keep GBR circuitry enabled for Open Load at ON diagnosis.

The circuitry that controls GBR function can be deactivated with the following SPI command sequence:

- **SWCR.SWR** = 1 (SPI command: 11001100_B)
- **LGCR.GBRn** = 0 (SPI command: $1101aaaa_B$ where “$aaaa$”$_B$ is the new value for **LGCR.GBRn** bits)
- (optional but recommended: **SWCR.SWR** = 0 (SPI command: 11000100_B)

Refer to **Chapter 9.7** for more details.

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8.5 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C

Typical values: V_S = 13.5 V, V_{DD}= 4.3 V, T_j = 25 °C

Typical resistive loads connected to the outputs (unless otherwise specified):

9 mΩ channels: R_L = 2.2 Ω

27 mΩ channels: R_L = 6.8 Ω (33 Ω when **LGCR.LEDn** = “1”)

Measurement setup used for k_{ILIS} (unless otherwise specified):

Channel 1, 4: when I_L ≤ 1.3 A both channels are ON at the same time with equal I_L, channels 2, 3 have I_L = 0
Channel 2, 3: when I_L ≤ 1.3 A both channels are ON at the same time with equal I_L, channels 1, 4 have I_L = 0

When I_L ≥ 2.0 A only the measured channel is ON, all other channels have I_L = 0

Table 10 Electrical Characteristics Diagnosis k_{ILIS} 9 mΩ ch.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense ratio I_{L04} = 450 mA	k_{ILIS04}	-67 %	4500	+142 %		–	P_8.5.5
Current sense ratio I_{L05} = 600 mA	k_{ILIS05}	-56 %	4500	+56 %		–	P_8.5.6
Current sense ratio I_{L07} = 1.3 A	k_{ILIS07}	-33 %	4500	+41 %		**LGCR.GBRn** = 0	P_8.5.8
Current sense ratio I_{L09} = 2.6 A	k_{ILIS09}	-18 %	4500	+18 %		**LGCR.GBRn** = 0	P_8.5.10
Current sense ratio I_{L10} = 4 A	k_{ILIS10}	-15 %	4500	+15 %		–	P_8.5.11
Current sense ratio I_{L11} = 7.5 A	k_{ILIS11}	-11 %	4500	+11 %		–	P_8.5.12

Table 11 Electrical Characteristics Diagnosis k_{ILIS} 27 mΩ ch.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition 27 mΩ ch.							
Current sense ratio I_{L03} = 300 mA	k_{ILIS03}	-42 %	2000	+42 %		–	P_8.5.28
Current sense ratio I_{L05} = 600 mA	k_{ILIS05}	-33 %	2000	+33 %		–	P_8.5.30
Current sense ratio I_{L07} = 1.3 A	k_{ILIS07}	-21 %	2000	+21 %		–	P_8.5.32
Current sense ratio I_{L09} = 2.6 A	k_{ILIS09}	-12 %	2000	+12 %		–	P_8.5.34
Current sense ratio I_{L10} = 4 A	k_{ILIS10}	-11 %	2000	+11 %		–	P_8.5.35

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Table 11 Electrical Characteristics Diagnosis k_{ILIS} 27 mΩ ch. (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition 27 mΩ ch. in LED mode							
Current sense ratio I_{L00} = 20 mA	k_{ILIS00}	-52 %	620	+52 %		–	P_8.5.37
Current sense ratio I_{L02} = 150 mA	k_{ILIS02}	-33 %	570	+33 %		–	P_8.5.39
Current sense ratio I_{L03} = 300 mA	k_{ILIS03}	-25 %	570	+25 %		LGCR.GBRn = 0	P_8.5.40
Current sense ratio I_{L05} = 600 mA	k_{ILIS05}	-14 %	570	+14 %		–	P_8.5.42
Current sense ratio I_{L06} = 1 A	k_{ILIS06}	-11 %	570	+11 %		–	P_8.5.43

Table 12 Electrical Characteristics Diagnosis

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Sense pin maximum voltage	$V_{IS(AZ)}$	42	47	54	V	I_{IS} = 5 mA	P_8.5.75
Current Sense Drift Over Current and Temperature per Device							
Current sense drift over current and temperature per device 9 mΩ ch.	$\Delta k_{ILIS(T)}$	-10	–	10	%	1) k_{ILIS11} versus k_{ILIS09}	P_8.5.76
Current sense drift over current and temperature per device 27 mΩ ch.	$\Delta k_{ILIS(T)}$	-8	–	8	%	1) k_{ILIS09} versus k_{ILIS07} LGCR.LEDn = 0	P_8.5.77
Current sense drift over current and temperature per device 27 mΩ ch. in LED mode	$\Delta k_{ILIS(T)}$	-9.5	–	9.5	%	1) k_{ILIS05} versus k_{ILIS03} LGCR.LEDn = 1	P_8.5.78

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Table 12 Electrical Characteristics Diagnosis (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Drift of Unaffected Channel during Inverse Current of other Channels One channel with $I_{L(IC)}$ = - I_{Ln}, all other channels with I_{Ln} DCR.MUX ≠ <111, 110> and set to sense any of the channels not in Inverse current condition							
Current sense drift of unaffected channels during inverse current of one channel	$\Delta k_{ILIS(IC)}$	-20	–	20	%	1) I_{L1} = 7.5 A I_{L2} = 2.6 A I_{L3} = 2.6 A I_{L4} = 7.5 A	P_8.5.83
Sense Pin - Currents							
Maximum steady state current sense output current 9 mΩ ch.	$I_{IS(MAX)}$	4.5	–	15	mA	V_{IS} = 0 V V_S ≥ 8 V	P_8.5.86
Maximum steady state current sense output current 27 mΩ ch.	$I_{IS(MAX)}$	3.8	–	15	mA	V_{IS} = 0 V V_S ≥ 8 V	P_8.5.87
Current sense leakage / offset current	$I_{IS(en)}$	–	–	1	µA	1) T_j ≤ 85 °C I_L = 0 mA **DCR.MUX** ≠ <111,110>$_B$	P_8.5.118
Current sense leakage / offset current	$I_{IS(en)}$	–	–	3.2	µA	T_j = 150 °C I_L = 0 mA **DCR.MUX** ≠ <111,110>$_B$	P_8.5.90
Open load detection threshold in ON state 9 mΩ ch.	$I_{L(OL)}$	–	–	48.5	mA	$I_{IS(OL)}$ = 4 µA	P_8.5.91
Open load detection threshold in ON state 27 mΩ ch.	$I_{L(OL)}$	–	–	21.5	mA	$I_{IS(OL)}$ = 4 µA **LGCR.LEDn** = 0	P_8.5.93
Open load detection threshold in ON state 27 mΩ ch. in LED mode	$I_{L(OL)}$	–	–	7.5	mA	$I_{IS(OL)}$ = 4 µA **LGCR.LEDn** = 1	P_8.5.94
Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	0.01	1	µA	I_{L2} = 2.6 A **DCR.MUX** = 110$_B$	P_8.5.98
Sense Pin - Timings							
Current sense settling time after channel activation 9 mΩ ch.	$t_{sIS(ON)}$	–	–	250	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ	P_8.5.99
Current sense settling time after channel activation 27 mΩ ch.	$t_{sIS(ON)}$	–	–	250	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ **LGCR.LEDn** = 0	P_8.5.101

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Table 12 Electrical Characteristics Diagnosis (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current sense settling time after channel activation 27 mΩ ch. in LED mode	$t_{sIS(ON)}$	–	–	100	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ **LGCR.LEDn** = 1	P_8.5.102
Current sense desettling time after channel deactivation	$t_{dIS(OFF)}$	–	–	25	µs	V_S = 13.5 V R_{IS} = 2.7 kΩ	P_8.5.106
Current sense settling time after change of load current 9 mΩ ch.	$t_{sIS(LC)}$	–	–	25	µs	1) I_L = 4 A to 2.6 A V_S = 13.5 V R_{IS} = 2.7 kΩ	P_8.5.107
Current sense settling time after change of load current 27 mΩ ch.	$t_{sIS(LC)}$	–	–	25	µs	1) I_L = 2.6 A to 1.3 A V_S = 13.5 V R_{IS} = 2.7 kΩ **LGCR.LEDn** = 0	P_8.5.109
Current sense settling time after change of load current 27 mΩ ch. in LED mode	$t_{sIS(LC)}$	–	–	25	µs	1) I_L = 1.3 A to 0.6 A V_S = 13.5 V R_{IS} = 2.7 kΩ **LGCR.LEDn** = 1	P_8.5.110
Current sense settling time after current sense activation	$t_{sIS(EN)}$	–	–	25	µs	R_{IS} = 2.7 kΩ I_{L2} = 2.6 A **DCR.MUX**: $110_B \rightarrow 001_B$	P_8.5.114
Current sense settling time after multiplexer channel change	$t_{sIS(MUX)}$	–	–	25	µs	R_{IS} = 2.7 kΩ I_{L2} = 2.6 A I_{L3} = 4 A **DCR.MUX**: $001_B \rightarrow 010_B$	P_8.5.115
Current sense deactivation time	$t_{dIS(MUX)}$	–	–	25	µs	1) R_{IS} = 2.7 kΩ **DCR.MUX**: $010_B \rightarrow 110_B$	P_8.5.116
Switch Bypass Monitor							
Switch bypass monitor threshold	$V_{DS(SB)}$	1.5	3.3	4.5	V	OFF state	P_8.5.117

1) Not subject to production test, specified by design.

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9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CS. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CS indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CS. A modulo 8 counter ensures that data is taken only when a multiple of 8 bit has been transferred. The interface provides daisy chain capability with 8-bit SPI devices.

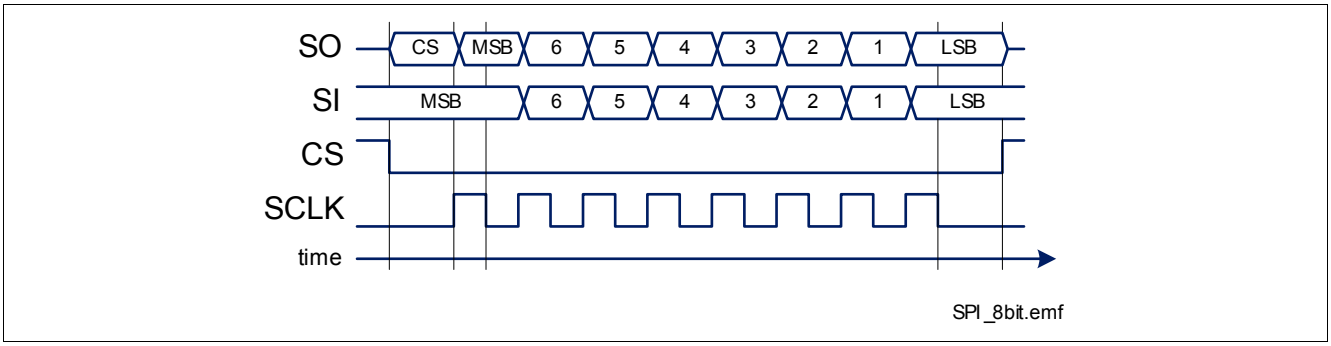


Figure 25 Serial Peripheral Interface

9.1 SPI Signal Description

CS - Chip Select

The system micro controller selects the BTS54220-LBE by means of the CS pin. Whenever the pin is in “low” state, data transfer can take place. When CS is in “high” state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CS “high” to “low” Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to “high” or “low” state depending on the signal level at pin SI.

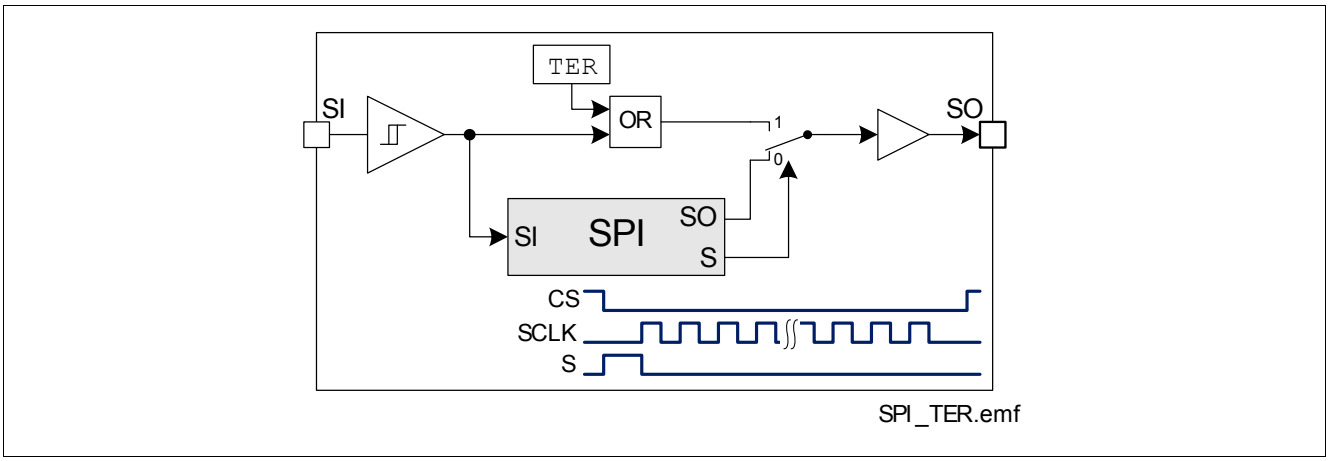


Figure 26 Combinatorial Logic for TER Flag

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CS “low” to “high” Transition

- Command decoding is only done, when after the falling edge of CS exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (**TER**) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select CS makes any transition, otherwise the command may be not accepted.

SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Chapter 9.5** for further information.

SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CS pin goes to “low” state. New data will appear at the SO pin following the rising edge of SCLK.

Please refer to **Chapter 9.5** for further information.

9.2 Daisy Chain Capability

The SPI of BTS54220-LBE provides daisy chain capability. In this configuration several devices are activated by the same CS signal MCS. The SI line of one device is connected with the SO line of another device (see **Figure 27**), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

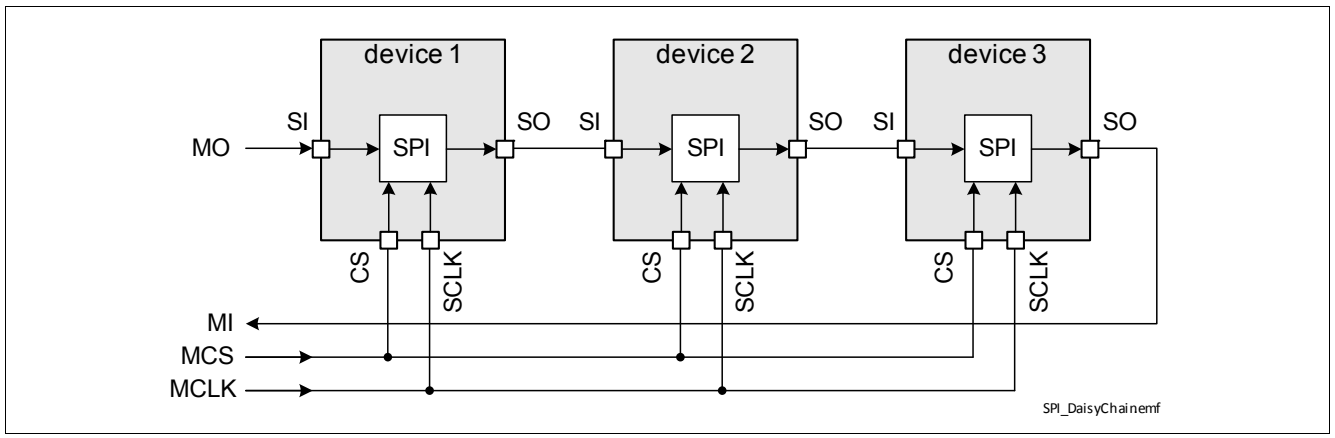


Figure 27 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After eight SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CS line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the MCS line must turn “high” (see **Figure 28**).

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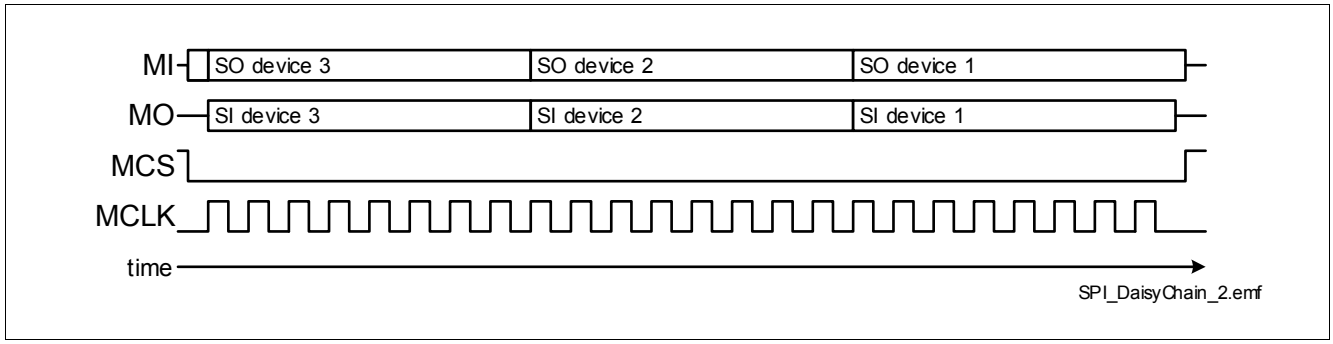


Figure 28 Data Transfer in Daisy Chain Configuration

9.3 Timing Diagrams

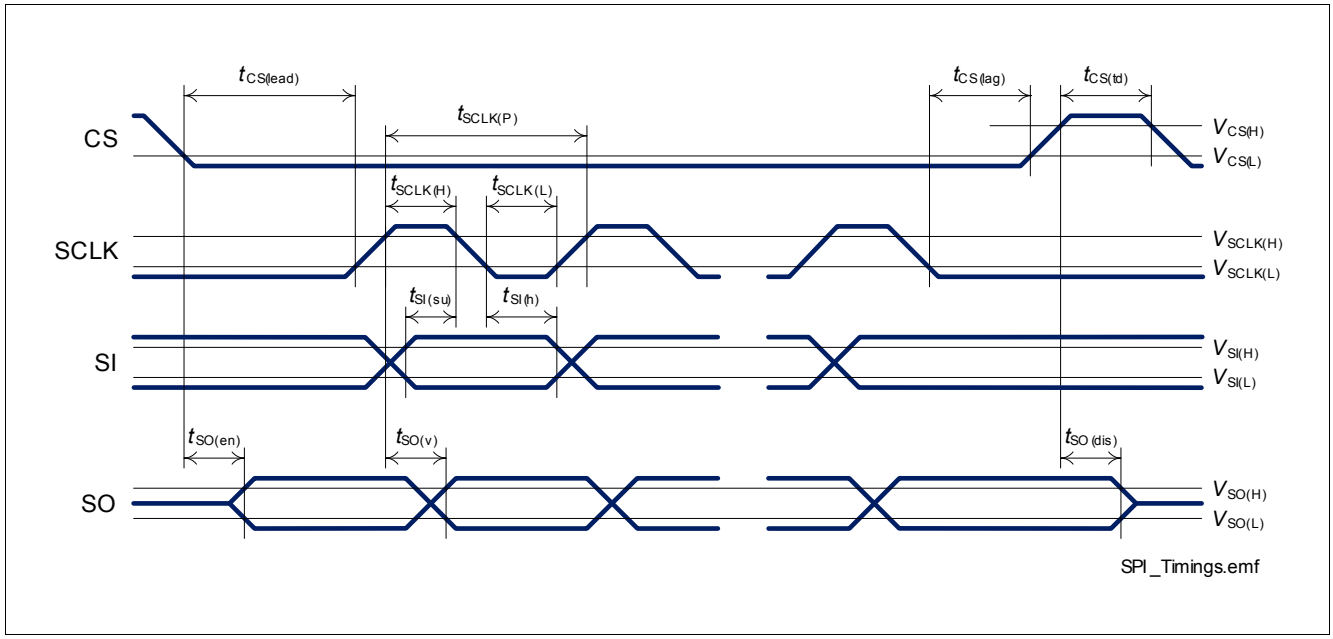


Figure 29 Timing Diagram SPI Access

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9.4 Electrical Characteristics

Unless otherwise specified: V_S = 7 V to 18 V, T_j = -40 °C to +150 °C, V_{DD} = 3.8 V to 5.5 V
Typical values: V_S = 13.5 V, T_j = 25 °C, V_{DD} = 4.3 V

Table 13 Electrical Characteristics Serial Peripheral Interface (SPI)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CS, SCLK, SI) - L Level of pin							
CS	$V_{CS(L)}$	-0.3	–	1.0	V	V_{DD} = 4.3 V	P_9.4.1
SCLK	$V_{SCLK(L)}$	-0.3	–	1.0	V	V_{DD} = 4.3 V	P_9.4.2
SI	$V_{SI(L)}$	-0.3	–	1.0	V	V_{DD} = 4.3 V	P_9.4.3
Input Characteristics (CS, SCLK, SI) - H Level of pin							
CS	$V_{CS(H)}$	2.6	–	V_{DD}	V	V_{DD} = 4.3 V	P_9.4.4
SCLK	$V_{SCLK(H)}$	2.6	–	V_{DD}	V	V_{DD} = 4.3 V	P_9.4.5
SI	$V_{SI(H)}$	2.6	–	V_{DD}	V	V_{DD} = 4.3 V	P_9.4.6
L-input pull-up current at CS pin	$-I_{CS(L)}$	7	30	75	µA	V_{DD} = 4.3 V V_{CS} = 1.0 V	P_9.4.7
H-input pull-up current at CS pin	$-I_{CS(H)}$	3	27	75	µA	V_{DD} = 4.3 V V_{CS} = 2.6 V	P_9.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(L)}$	3	27	75	µA	V_{SCLK} = 1.0 V V_{DD} = 4.3 V	P_9.4.9
SI	$I_{SI(L)}$	3	27	75	µA	V_{SI} = 1.0 V V_{DD} = 4.3 V	P_9.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(H)}$	7	30	75	µA	V_{SCLK} = 2.6 V V_{DD} = 4.3 V	P_9.4.11
SI	$I_{SI(H)}$	7	30	75	µA	V_{SI} = 2.6 V V_{DD} = 4.3 V	P_9.4.12
Output Characteristics (SO)							
L level output voltage	$V_{SO(L)}$	0	–	0.5	V	I_{SO} = -0.5 mA	P_9.4.13
H level output voltage	$V_{SO(H)}$	V_{DD} - 0.5 V	–	V_{DD}	V	I_{SO} = 0.5 mA V_{DD} = 4.3 V	P_9.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	µA	V_{CS} =V_{DD} V_{SO} = 0 V V_{SO} = V_{DD}	P_9.4.15
Timings							
Enable lead time (falling CS to rising SCLK)	$t_{CS(lead)}$	200	–	–	ns	–[1)]	P_9.4.16
Enable lag time (falling SCLK to rising CS)	$t_{CS(lag)}$	200	–	–	ns	–[1)]	P_9.4.17
Transfer delay time (rising CS to falling CS)	$t_{CS(td)}$	1	–	–	µs	–[1)]	P_9.4.18

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Table 13 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output enable time (falling CS to SO valid)	$t_{SO(en)}$	–	–	1	µs	1) C_L = 50 pF	P_9.4.19
Output disable time (rising CS to SO tristate)	$t_{SO(dis)}$	–	–	1	µs	1) C_L = 50 pF	P_9.4.20
Serial clock frequency	f_{SCLK}	0	–	3	MHz	–1)	P_9.4.22
Serial clock period	$t_{SCLK(P)}$	333	–	–	ns	–1)	P_9.4.24
Serial clock "high" time	$t_{SCLK(H)}$	150	–	–	ns	–1)	P_9.4.26
Serial clock "low" time	$t_{SCLK(L)}$	150	–	–	ns	–1)	P_9.4.28
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	65	–	–	ns	–1)	P_9.4.30
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	65	–	–	ns	–1)	P_9.4.32
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	166	ns	1) C_L = 50 pF	P_9.4.34

1) Not subject to production test, specified by design

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9.5 SPI Protocol

The relationship between SI and SO content during SPI communication is shown in **Figure 30**. SI line represents the frame sent from the µC and SO line is the answer provided by BTS54220-LBE. The “(previous response)” means that the frame sent back depends on the command frame sent from the µC before.

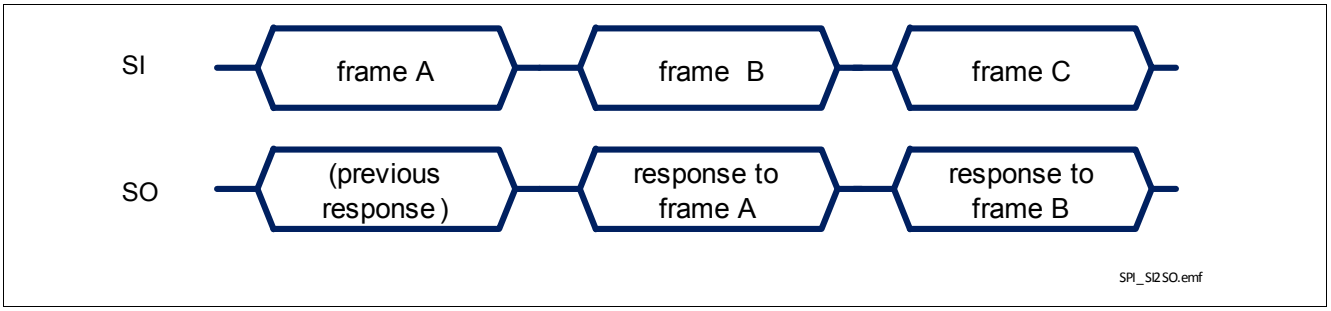


Figure 30 Relationship between SI and SO during SPI communication

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the µC. Although the biggest majority of commands and frames implemented in BTS54220-LBE can be decoded without the knowledge of what happened before, it is advisable to consider what the µC sent in the previous transmission to decode BTS54220-LBE response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register will look as follows:

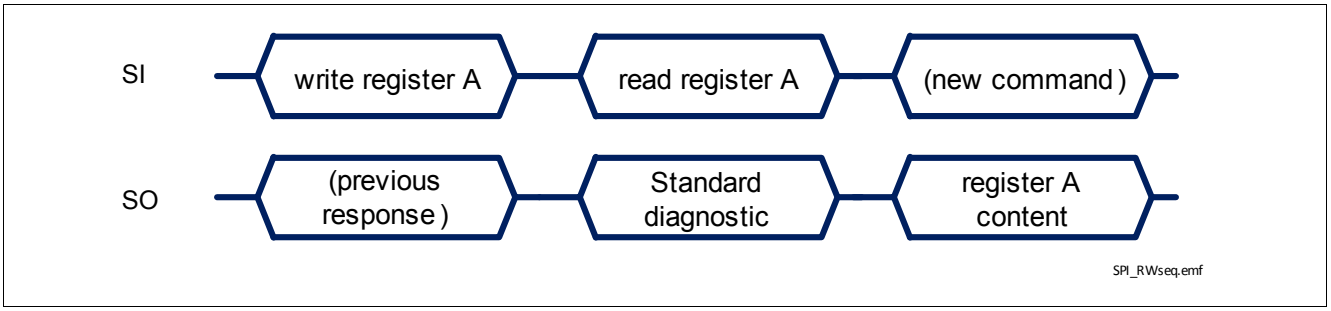


Figure 31 Register content sent back to µC

There are 3 special situations where the frame sent back to the µC doesn't depend on the previous received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8), shown in **Figure 32**
- when BTS54220-LBE logic supply comes out of Power-On reset condition, as shown in **Figure 33**
- when $V_S < V_{SMON}$ and **DCR.MUX** $\neq 111_B$, as shown in **Figure 34**

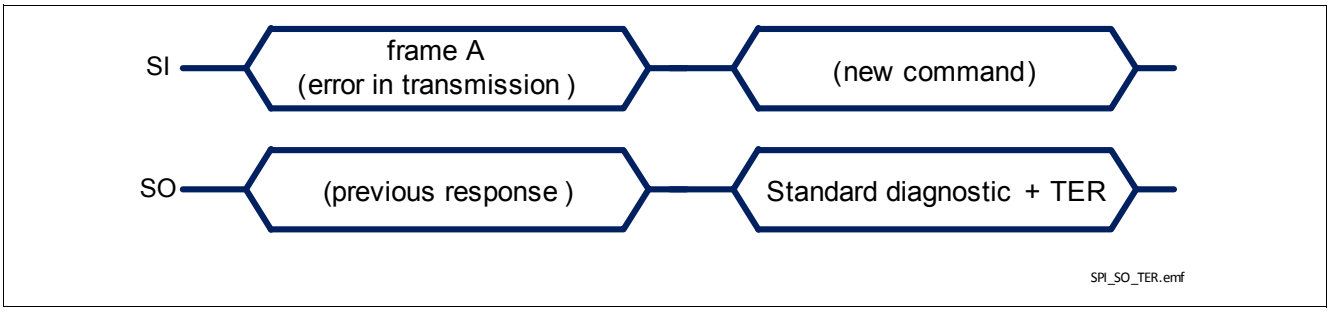


Figure 32 BTS54220-LBE response after an error in transmission

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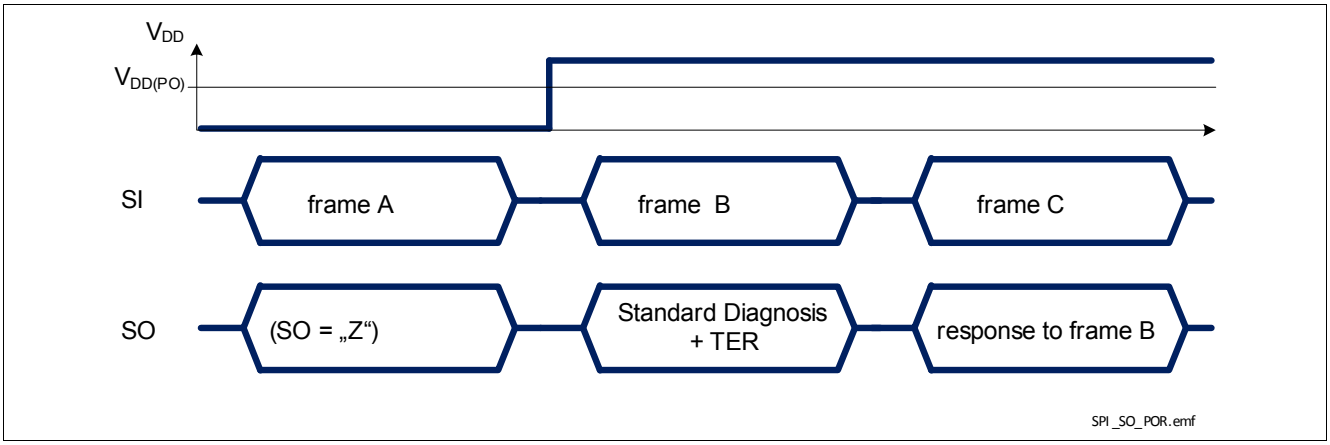


Figure 33 BTS54220-LBE response after coming out of Power-On reset at V_{DD}

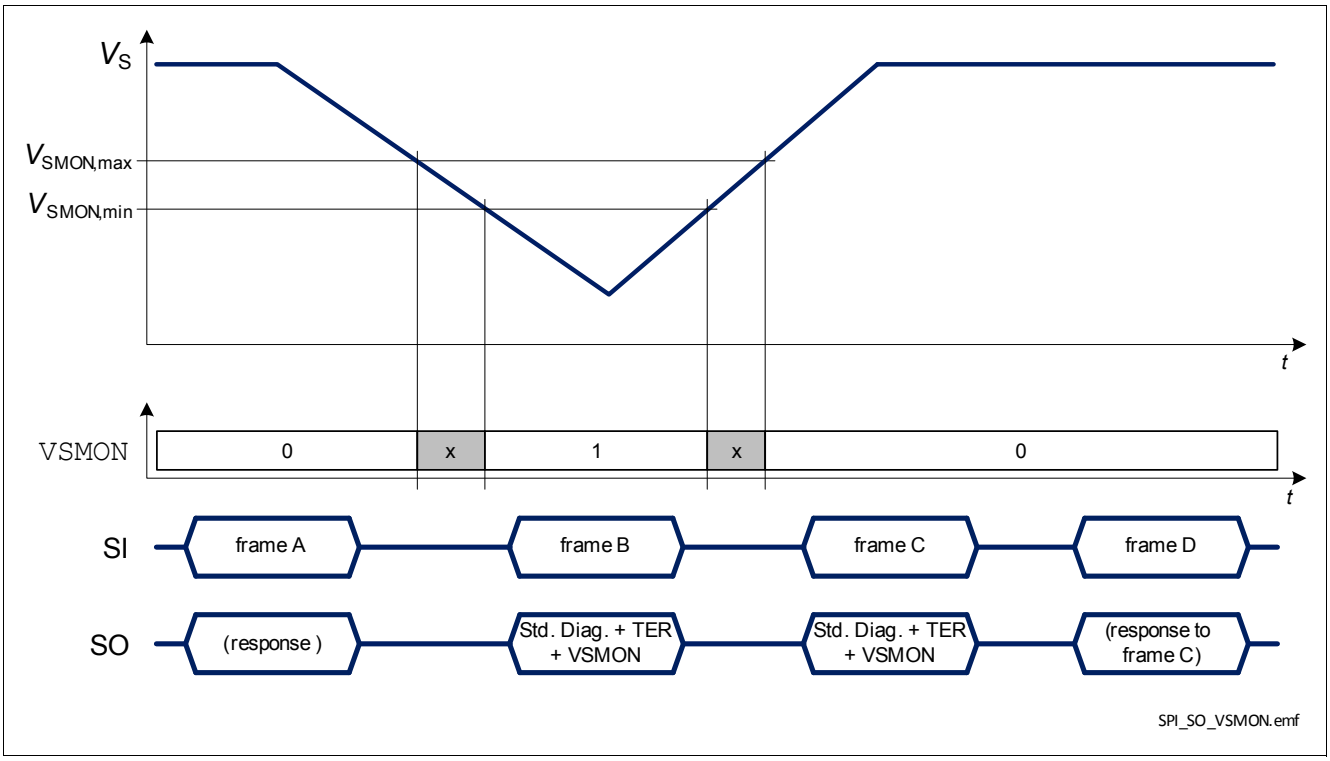


Figure 34 BTS54220-LBE response in case of a negative battery voltage transient

A summary of all possible SPI commands is presented in **Table 14**, including the answer that BTS54220-LBE will send back at the next transmission.

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Table 14 SPI Command Summary

Requested Operation	Frame sent to SPOC+ (SI pin)	Frame received from SPOC+ (SO pin) with the next command
Write OUT register	$100aaaaa_B$ where: "$aaaaa_B$" = new OUT register content	$0aaaaaaa_B$ (Standard Diagnosis)
Read OUT register	$00xx0000_B$ ("xx_B" = don't care)	$10aaaaaa_B$ ("$aaaaaa_B$" = OUT register content)
Write Configuration register	$11aabbbb_B$ where: "aa_B" = register address "$bbbb_B$" = new register content	$0aaaaaaa_B$ (Standard Diagnosis)
Read Configuration register	$01aa0000_B$ where: "aa_B" = register address	$11aabbbb_B$ where: "aa_B" = register address "$bbbb_B$" = register content
Read Standard Diagnosis	$0xxx0001_B$ ("xxx_B" = don't care)	$0aaaaaaa_B$ (Standard Diagnosis)
Read Errors Diagnosis	$0xxx0011_B$ ("xxx_B" = don't care)	$00aaaaaa_B$ (Error Diagnosis)
Read Warnings Diagnosis	$0xxx0101_B$ ("xxx_B" = don't care)	$00aaaaaa_B$ (Warning Diagnosis)

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9.6 SPI Diagnosis Registers

9.6.1 Standard Diagnosis

SO	7	6	5	4	3	2	1	0	Default
	0	TER	LHI	STB	VSMON	ERR_MUX			50_H

Field	Bits	Type	Description
TER	6	r	**Transmission Error** 0_B Previous transmission was successful (modulo 8 clocks received) 1_B (default) Previous transmission failed or first transmission after reset
LHI	5	r	**Limp Home monitor** 0_B (default) Normal mode operation 1_B Limp Home Mode
STB	4	r	**Standby mode monitor** 0_B Normal mode operation 1_B (default) Stand-by mode
VSMON	3	r	**V_S monitor** 0_B (default) V_S always > V_{SMON} since last Standard Diagnosis readout 1_B V_S < V_{SMON} at least once
ERR_MUX	2:0	r	**Diagnosis of Channel n in error** 000_B (default) No channel latched OFF 001_B Channel one latched OFF 010_B Channel two latched OFF 011_B Channel three latched OFF 100_B Channel four latched OFF 101_B Not used 110_B Not used 111_B More than one channel latched OFF

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9.6.2 Errors Diagnosis

SO	7	6	5	4	3	2	1	0	Default
	0	0	0	1	**ERR_COUNTERn**				10_H

Field	Bits	Type	Description
ERR_COUNTERn n = 4 to 1	3:0	r	**Diagnosis of Channel n** 0_B (default) No failure 1_B Over temperature counter reached to n_{retry}

9.6.3 Warnings Diagnosis

SO	7	6	5	4	3	2	1	0	Default
	0	0	1	0	**ERRn**				20_H

Field	Bits	Type	Description
ERRn n = 4 to 1	3:0	r	**Warning Diagnosis of Channel n** 0_B (default) No failure 1_B Over temperature counter > 0

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9.7 SPI Configuration Registers

The following table provides an overview on the registers available and the available addressing space.

Table 15 Register Overview

Register name	Register Bank	Address	SWCR.SWR bit	Content
OUT	0	(na)	0	Output configuration
OUT	0	(na)	1	Input status
SWCR	1	00	(na)	Swap configuration
LGCR	1	01	0	LED mode configuration
LGCR	1	01	1	Gate Back Regulation configuration
HWCR	1	10	(na)	Hardware configuration
DCR	1	11	(na)	Diagnostic configuration

9.7.1 Output Configuration Register

SWCR.SWR = 0

Bit	7	6	5	4	3	2	1	0	
Name	W = 1 R = 0	RB	5	4	3	2	1	0	Default
OUT	W/R	0	0	OUT.OUTn					80_H

9.7.2 Input Status Register

SWCR.SWR = 1

Bit	7	6	5	4	3	2	1	0	
Name	W = 1 R = 0	RB	5	4	3	2	1	0	Default
OUT	R	0	LHI	1	0	0	OUT.INSTn		90_H

9.7.3 Swap Configuration Register

Bit	7	6	5	4	3	2	1	0	Default
Name	W = 1 R = 0	RB	ADDR		3	2	1	0	
SWCR	W/R	1	00		SWCR.SWR	1	0	0	$C4_H$

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9.7.4 LED Mode Configuration Register

SWCR.SWR = 0

Name	W = 1 / R = 0	RB	ADDR	3	2	1	0	Default
LGCR	W/R	1	01	0	LGCR.LEDn		0	$D0_H$

9.7.5 Gate Back Regulation Register

SWCR.SWR = 1

Name	W = 1 / R = 0	RB	ADDR	3	2	1	0	Default
LGCR	W/R	1	01	LGCR.GBRn				DF_H

9.7.6 Hardware Configuration Register

Name	W = 1 / R = 0	RB	ADDR	3	2	1	0	Default
HWCR	R	1	10	HWCR.RCR	HWCR.COL	HWCR.STB	0	$E2_H$
	W	1	10	HWCR.RCR	HWCR.COL	HWCR.RST	HWCR.CTC	-

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9.7.7 Diagnosis Control Register

Name	W = 1 R = 0	RB	ADDR	3	2	1	0	Default
DCR	R	1	11	DCR.SBM	DCR.MUX			$F7_H$
	W	1	11	0	DCR.MUX			-

9.7.8 Configuration Register Bit Overview

Field	Bits	Type	Description
RB	6	rw	**Register Bank** 0_B (default) Read / write to OUT register 1_B Read / write to other registers
OUT.OUTn n = 5 to 1	4:0	rw	**Output Control Register of Channel n** 0_B (default) channel is OFF 1_B Channel is ON
OUT.INSTn n = 2 to 1	1:0	r	**Input Status Monitor Channel n** 0_B (default) Input signal is “low” 1_B Input signal is “high”
LGCR.LEDn n = 3 to 2	2:1	rw	**Set LED Mode for Channel n** 0_B (default) Channel n is in bulb mode 1_B Channel n is in LED mode
LGCR.GBRn n = 4 to 1	3:0	rw	**Gate Back Regulation for Channel n** 0_B Gate back regulation for Channel n is forced OFF 1_B (default) Gate back regulation for Channel n is active
HWCR.CTC	0	w	**Clear Thermal Counter** 0_B (default) Thermal latches are untouched 1_B Command: Clear all thermal latches
HWCR.RST	1	w	**Reset Command** 0_B (default) Normal operation 1_B Execute reset command
HWCR.STB	1	r	**Standby Mode** 0_B Device is awake 1_B (default) Device is in Standby mode
HWCR.COL	2	rw	**Input Combinatorial Logic Configuration** 0_B (default) Input signal OR-combined with according OUT register bit[1)] 1_B Input signal AND-combined with according OUT register bit
HWCR.RCR	3	rw	**Retry Counter Reset** 0_B (default) Retry Counter is reset only for HWCR.CTC=1 (and V_{DD} reset) 1_B Retry Counter is reset for every IN-pin or OUT.OUTn “high” to “low” transition for $n_{retry} < n_{retry,max}$ and also for HWCR.CTC=1 (and V_{DD} reset)

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Field	Bits	Type	Description
SWCR.SWR	1	rw	**Switch Register** 0_B (default) **OUT.OUTn** and **LGCR.LEDn** can be written and read 1_B **OUT.INSTn** can be read and **LGCR.GBRn** can be written and read
DCR.SBM	3	r	**Switch Bypass Monitor**[2] 0_B $V_{DS} < V_{DS(SB)}$ 1_B $V_{DS} > V_{DS(SB)}$
DCR.MUX	2:0	rw	**Set Current Sense Multiplexer Configuration in OFF-state** 000_B IS pin is high impedance 001_B IS pin is high impedance 010_B IS pin is high impedance 011_B IS pin is high impedance 100_B Diagnosis enable of external driver activated (EDD set to “high”) 101_B IS pin is high impedance 110_B IS pin is high impedance 111_B Stand-by mode (IS pin is high impedance) **Set Multiplexer Configuration in ON-state** 000_B Current sense of channel 1 is routed to IS pin 001_B Current sense of channel 2 is routed to IS pin 010_B Current sense of channel 3 is routed to IS pin 011_B Current sense of channel 4 is routed to IS pin 100_B Diagnosis enable of external driver activated (EDD set to “high”) 101_B IS pin is high impedance 110_B IS pin is high impedance 111_B Stand-by mode (IS pin is high impedance))

1) In Limp Home Mode (LHI pin set to “high”) the combinatorial logic is switched to OR-mode.

2) The switch bypass monitor compares the threshold $V_{DS(SB)}$ with the voltage V_{DS} across the power transistor of that channel which is selected by the current sense multiplexer (**DCR.MUX**).

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10 Application Description

The following figure describes a typical operating circuit. It shall not be considered as a warranty of a certain functionality, condition or quality of the device. The **Table 16** shows suggested component values and purposes.

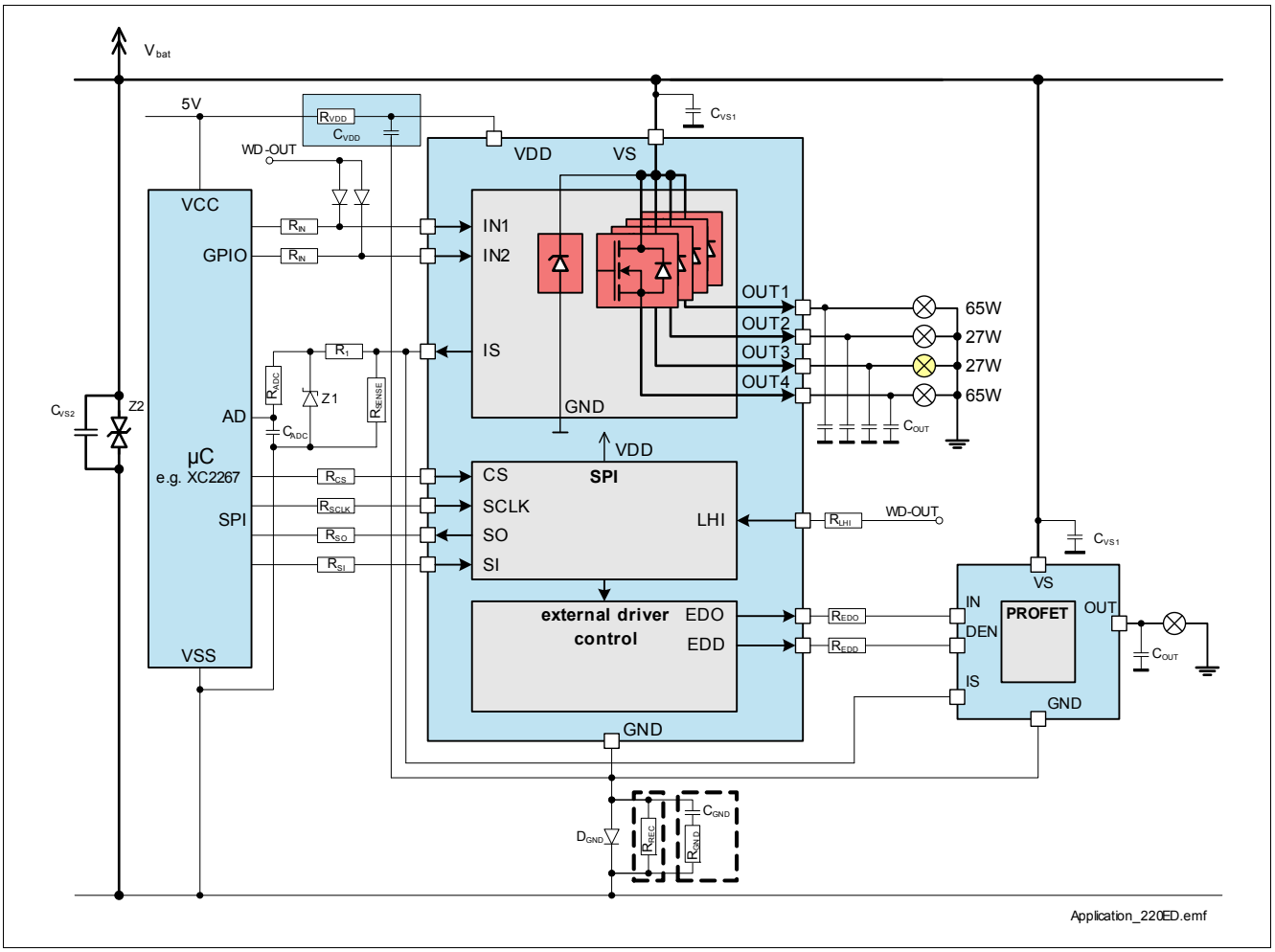


Figure 35 Application Circuit Example

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Table 16 Suggested Component Values

Reference	Value	Purpose
R_{VDD}	500 Ω	Device logic protection (Size 1206 recommended)
R_{IN}	8 kΩ	Protection of the µC during overvoltage, reverse polarity and loss of ground
R_1	4.7 kΩ	Protection resistor for overvoltage, reverse polarity and loss of ground. Value to be tuned with µC specification
R_{IS}	2.7 kΩ	Sense resistor
R_{ADC}	1 kΩ	µC-ADC voltage spikes filtering
R_{CS}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SCLK}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SO}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{SI}	3.9 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{LHI}	8 kΩ	Protection of the µC during overvoltage and reverse polarity
R_{EDO}	8 kΩ	Protection of the device during overvoltage, reverse polarity of external driver
R_{EDD}	8 kΩ	Protection of the device during overvoltage, reverse polarity of external driver
C_{ADC}	1 nF	µC-ADC voltage spikes filtering
C_{VDD}	100 nF	Logic supply voltage spikes filtering
C_{VS1}	68 nF	Battery voltage spikes filtering
C_{VS2}	100 nF	Battery voltage spikes filtering
C_{OUT}	10 nF	For improved electromagnetic compatibility (EMC)
C_{GND}	8.2 nF	Ground voltage spikes filtering (optional for improved robustness against battery voltage transients)
R_{GND}	100 Ω	Ground voltage spikes filtering (optional for improved robustness against battery voltage transients)
R_{REC}	1 kΩ	Ground voltage recycling path (optional for providing a recycle path in case of loss of Battery)
Z_1	7 V	Protection of µC during overvoltage. Zener diode
Z_2	P6SMB30	Protection of device during overvoltage. Zener diode
D_{GND}	BAS70	Protection of device during reverse polarity. Schottky diode

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11 Package Outlines BTS54220-LBE

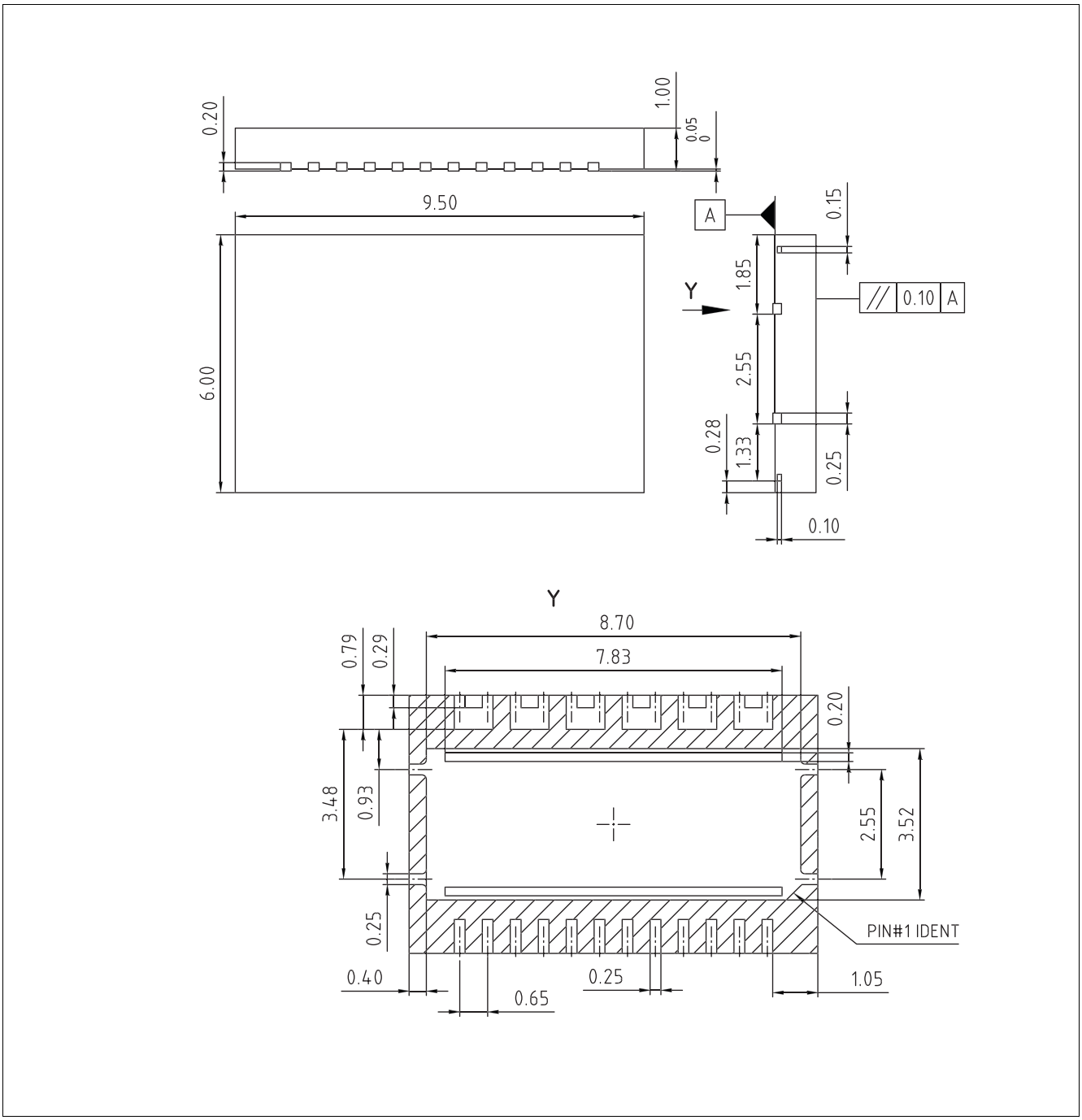


Figure 36 TSON-24-10 Package drawing

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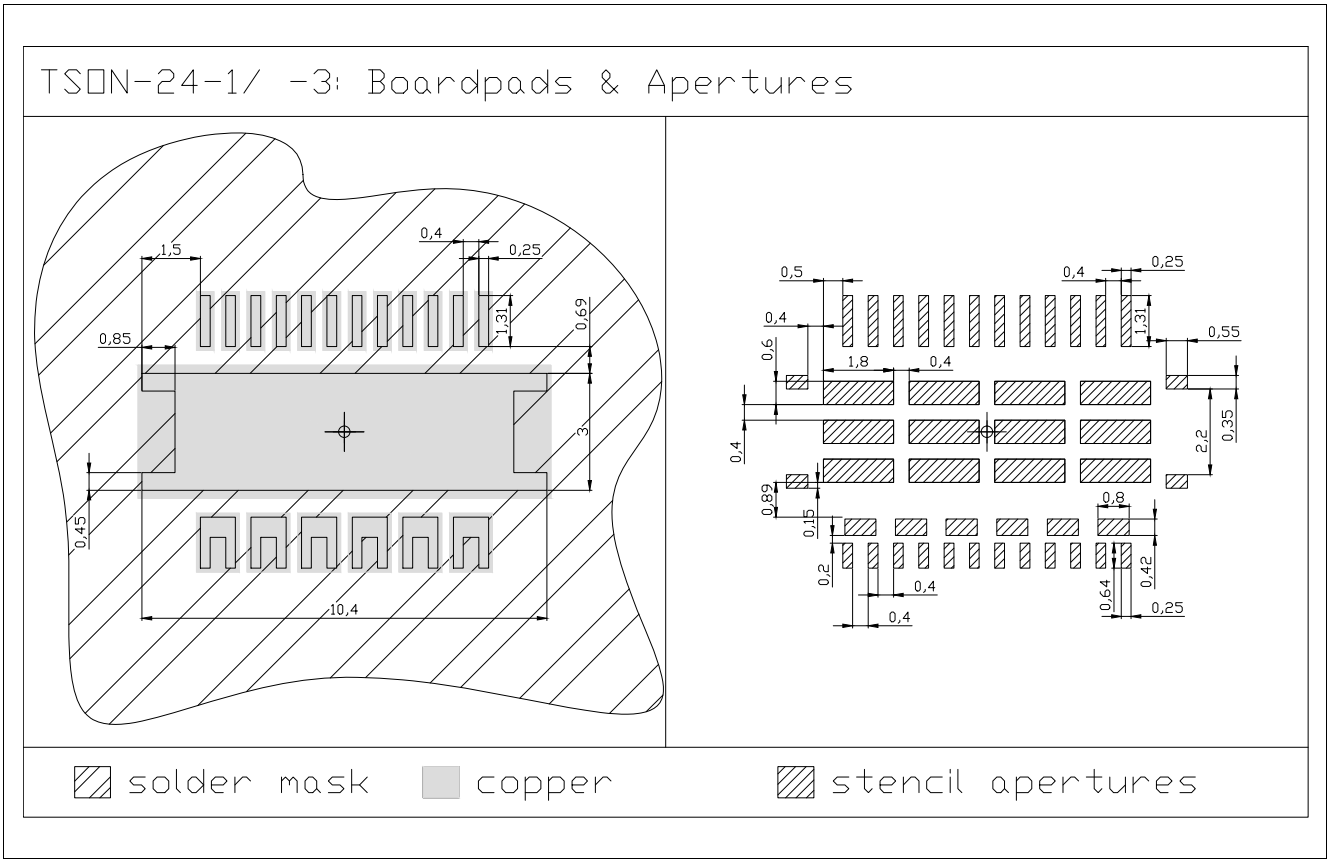


Figure 37 TSON-24 Package pads and stencil

Green Product (RoHS Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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