Radiation Hardened level translating I²C, SMBUS, SPI 16-bit I/O expander

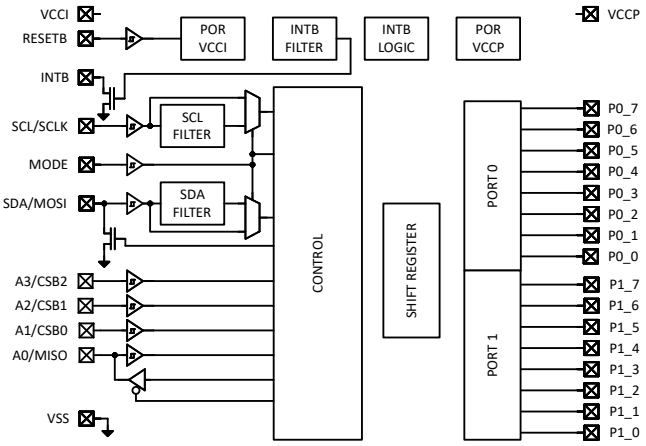
1 GENERAL DESCRIPTION

The **APIO16/AFIO16** is a 16-bit radiation-hardened **level translating I²C, SMBUS, SPI 16-bit I/O expander** designed for harsh environments, such as space and medical applications. It provides voltage-level translation and bi-directional communication over I²C , SMBUS, or SPI interfaces, supporting low-voltage controllers while driving higher voltage peripherals.

The APIO16/AFIO16 features extensive circuit techniques throughout, including triple modular redundancy, self correcting digital circuits and Dual Interlocked storage CEll (DICE) latches to ensure a high level of immunity to single-event transients (SET) and single event upset (SEU) without requiring additional redundant devices.

The APIO16/AFIO16 supports up to 16 I²C addresses configured via dedicated pins, and three SPI chip-select inputs allow multi-device SPI operation with minimal additional decoding logic. The open-drain INTB pin alerts the controller of input changes.

The **APIO16** is the Low Earth Orbit (LEO) variant with 30 krad TID assurance at maximum power supply while the **AFIO16** is the Geosynchronous Earth Orbit (GEO) variant with 300 krad TID assurance at the maximum power supply. These two variants have unique die each architected for its intended mission orbit.



1.1 FEATURES

- 16-bit general purpose parallel I/O expansion
- Supports SMBUS, 1 MHz I²C, and 25 MHz SPI
- Built-in level shifting in voltage range of 1.4 V to 5.5 V
- I²C supports 4 pin configurable address bits allowing up to 16 APIO16/AFIO16 devices (256 I/Os) on single I²C bus
- SEL, SEU, SEFI Immune to LET of 75 MeV-cm2/mg
- SET Immune to LET of 75 MeV-cm2/mg for $V_{CCI} \geq 1.8$ V and $V_{CCP} > 1.8$ V
- Radiation Lot Acceptance at TID 30 krad (Si), LEO
- Radiation Lot Acceptance at TID 300 krad (Si), GEO
- Schmitt triggered inputs on all interface/port pins
- Open drain interrupt output (INTB)
- 25 mA source/sink drive strength
- Cold spareable I/Os with zero power penalty
- Meets NASA's ASTM E595 outgassing specification

DEVICE INFORMATION

PART NUMBER	GRADE	Package
APIO16ANT-R	A-Grade Flight (LEO)	TSSOP-28 Plastic 6.4mm x 9.7mm mass = 95 mg
APIO16BNT-R	B-Grade Flight (LEO)	
APIO16CNT-R	C-Grade Flight (LEO)	
APIO16ENT-R	E-Grade	
AFIO16ANT-R	A-Grade Flight (GEO)	
AFIO16BNT-R	B-Grade Flight (GEO)	
AFIO16CNT-R	C-Grade Flight (GEO)	
AFIO16ENT-R	E-Grade	

1.2 APPLICATIONS

- Bus expansion
- MCU/Processor wake/sleep support
- Power sequencing and domain control
- Dynamic Voltage Scaling (DVS) control
- Phased-array antenna element control
- Telemetry and remote sensing
- Fault containment, signal sensing with remote interrupt
- Basic DACs/ADCs
- Rad-hard data/configuration storage

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge	POR	Power On Reset
RHA	Radiation Hardness Assurance	SEE	Single Event Effects
SEFI	Single Event Functional Interrupt	SEL	Single Event Latchup
SET	Single Event Transient	TID	Total Ionizing Dose
TMR	Triple Modular Redundancy	CDM	Charged-device Model
HBM	Human-body Model		

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3 PIN CONFIGURATION

Figure 1 shows the pin assignments for the TSSOP-28 package APIO16/AFIO16 device.

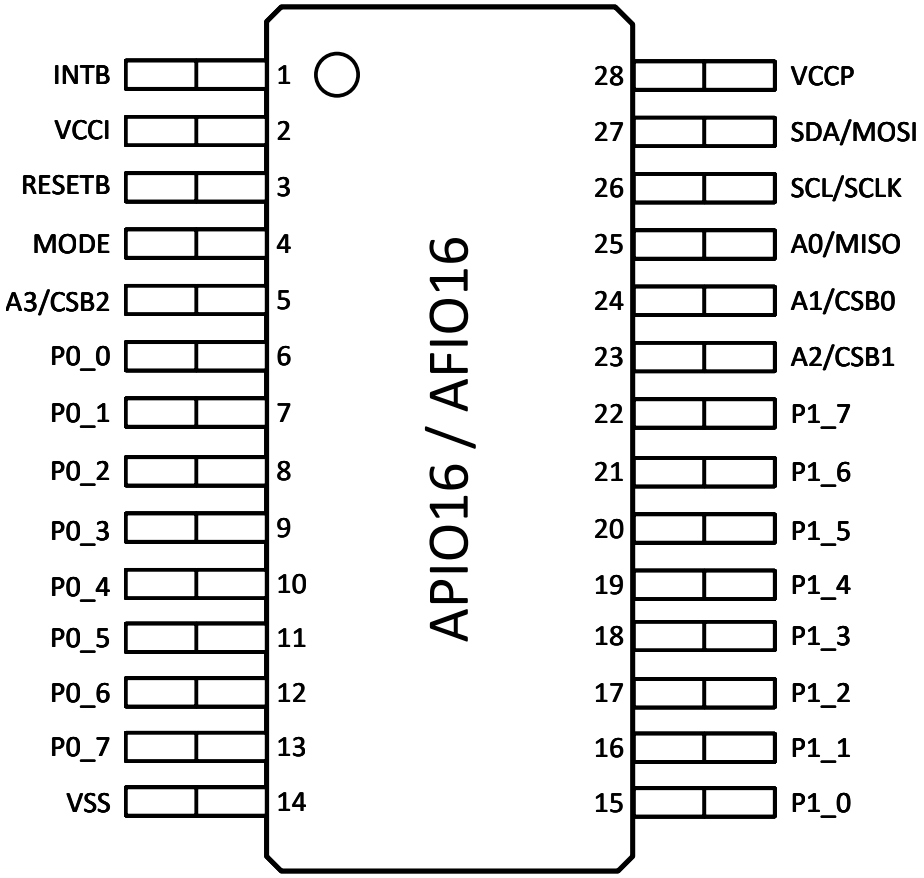

Figure 1: APIO16/AFIO16 device pinout overview

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Table 1: APIO16/AFIO16 device pinout description

PIN NAME(S) & NUMBER(S)		DESCRIPTION	
NAME	**NUMBER**	**MODE = low (I^2C)**	**MODE = high (SPI)**
SDA/MOSI	27	I^2C SDA [(1)]	SPI MOSI input [(1)]
SCL/SCLK	26	I^2C SCL [(1)]	SPI SCLK input [(1)]
A0/MISO	25	Address bit A0 [(1)]	MISO tri-state output [(1)]
A1/CSB0	24	Address bit A1 [(1)]	Active low chip select CSB0 [(1)]
A2/CSB1	23	Address bit A2 [(1)]	Active low chip select CSB1 [(1)]
A3/CSB2	5	Address bit A3 [(1)]	Active low chip select CSB2 [(1)]
INTB	1	Open drain active low interrupt output, pull-up to a 5.5V maximum rail through a pull-up resistor	
RESETB	3	Active low reset input pull-up to V_{CCI} if not required [(1)]	
MODE	4	If low, part operates with an I^2C interface, if high, part operates with an SPI interface. Tie to V_{SS} or V_{CCI} [(1)]	
VCCI	2	Supply voltage for all pins other than ports	
P0_0	6	Port 0 input/output 0 [(2)]	
P0_1	7	Port 0 input/output 1 [(2)]	
P0_2	8	Port 0 input/output 2 [(2)]	
P0_3	9	Port 0 input/output 3 [(2)]	
P0_4	10	Port 0 input/output 4 [(2)]	
P0_5	11	Port 0 input/output 5 [(2)]	
P0_6	12	Port 0 input/output 6 [(2)]	
P0_7	13	Port 0 input/output 7 [(2)]	
VSS	14	Ground	
P1_0	15	Port 1 input/output 0 [(2)]	
P1_1	16	Port 1 input/output 1 [(2)]	
P1_2	17	Port 1 input/output 2 [(2)]	
P1_3	18	Port 1 input/output 3 [(2)]	
P1_4	19	Port 1 input/output 4 [(2)]	
P1_5	20	Port 1 input/output 5 [(2)]	
P1_6	21	Port 1 input/output 6 [(2)]	
P1_7	22	Port 1 input/output 7 [(2)]	
VCCP	28	Supply voltage for ports, tied to V_{CCP}	

[(1)] Referenced to V_{CCI}
[(2)] Referenced to V_{CCP}

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4 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

4.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 2 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 3) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
V_{CCI}, V_{CCP}	Supply voltage		-0.3 to +5.5	V
V_I	INTB, RESETB, MODE, Port pins (P0_x, P1_x), A0/MISO, A1/CSB0, A2/CSB1, A3/CSB2, SCL/SCLK, and SDA/MOSI		-0.3 to +5.5	V
I_{IK}	Maximum current into input pins		-100 to 100	mA
I_O	Maximum current into output pins		-100 to 100	mA
I_{CCI}	Maximum current into V_{CCI} pin		-100 to 100	mA
I_{CCP}	Maximum current into V_{CCP} pin		-100 to 420	mA
I_{VSS}	Maximum current out of V_{SS} pin		-420 to 100	mA
V_{ESD}	ESD Voltage	HBM	$>$ 1000	V
		CDM	$>$ 500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

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4.2 RECOMMENDED OPERATING CONDITIONS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified.

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{CCI}, V_{CCP}	Supply voltages	T_J = -55°C to 125°C	1.65	5.5	V
		T_J = 0°C to 110°C	1.4	5.5	
V_I	INTB, RESETB, MODE, Port pins (P0_x, P1_x), A0/MISO, A1/CSB0, A2/CSB1, A3/CSB2, SCL/SCLK, and SDA/MOSI		0	5.5	V
V_{O_I}	Output voltage on serial interface pins		0	V_{CCI}	V
V_{O_P}	Output voltage on port pins		0	V_{CCP}	V
I_{OL}	LOW level output current per pin: serial interface and port pins		-	25	mA
I_{OH}	HIGH level output current per pin: serial interface and port pins		-	-25	mA
I_{CCP}	Current into V_{CCP} pin		-	410	mA
I_{VSS}	Current out of V_{SS} pin		-	-410	mA

Table 4: Thermal Information

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	V_{CCI},V_{CCP} = 1.65 to 5.5 V	-55	-	+125	°C
		V_{CCI},V_{CCP} = 1.4 to 5.5 V	0	-	+110	
$R_{\theta JA}$	Junction to ambient thermal resistance		-	64	-	°C/W

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4.3 ELECTRICAL CHARACTERISTICS

All recommended parameters below are specified across the entire operating temperature range unless otherwise specified. Note that 1.65V to 5.5V operation is specified over the full temperature range (-55°C to 125°C), while 1.4 to 5.5V operation is specified over a reduced temperature range (0°C to 110°C).

Table 5: Electrical Characteristics: General

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCI_START}	V_{CCI} POR start voltage		-	1.13	1.36	V
V_{CCP_START}	V_{CCP} POR start voltage		-	1.13	1.36	V
V_{CCI_STOP}	V_{CCI} POR stop voltage		0.8	1.08	-	V
V_{CCP_STOP}	V_{CCP} POR stop voltage		0.8	1.08	-	V
V_{CCI_HYST}	V_{CCI} POR hysteresis		20	52	110	mV
V_{CCP_HYST}	V_{CCP} POR hysteresis		20	52	110	mV
V_{T-}	INTB, RESETB, MODE, A0/MISO, A1/CSB0, A2/CSB1, A3/CSB2, SCL/SCLK, and SDA/MOSI Negative-going threshold voltage	V_{CCI} = 5.5 V	1.65	2.6	-	V
		V_{CCI} = 3.0 V	0.9	1.4	-	
		V_{CCI} = 1.65 V	0.495	0.73	-	
		V_{CCI} = 1.4 V, 0°C to 110°C	0.42	0.6	-	
V_{T-}	Port pins (P0_x, P1_x) Negative-going threshold voltage	V_{CCP} = 5.5 V	1.65	2.6	-	V
		V_{CCP} = 3.0 V	0.9	1.4	-	
		V_{CCP} = 1.65 V	0.495	0.73	-	
		V_{CCP} = 1.4 V, 0°C to 110°C	0.42	0.6	-	
V_{T+}	INTB, RESETB, MODE, A0/MISO, A1/CSB0, A2/CSB1, A3/CSB2, SCL/SCLK, and SDA/MOSI Positive-going threshold voltage	V_{CCI} = 5.5 V	-	3.0	3.85	V
		V_{CCI} = 3.0 V	-	1.7	2.1	
		V_{CCI} = 1.65 V	-	1.03	1.15	
		V_{CCI} = 1.4 V, 0°C to 110°C	-	0.88	0.98	
V_{T+}	Port pins (P0_x, P1_x) Positive-going threshold voltage	V_{CCP} = 5.5 V	-	3.0	3.85	V
		V_{CCP} = 3.0 V	-	1.7	2.1	
		V_{CCP} = 1.65 V	-	1.03	1.15	
		V_{CCP} = 1.4 V, 0°C to 110°C	-	0.88	0.98	
ΔV_T	SCL/SCLK, and SDA/MOSI Input hysteresis (V_{T+}-V_{T-})	V_{CCI} = 5.5 V	0.3	0.38	-	V
		V_{CCI} = 3.0 V	0.22	0.32	-	
		V_{CCI} = 1.65 V	0.15	0.29	-	
		V_{CCI} = 1.4 V, 0°C to 110°C	0.15	0.29	-	
ΔV_T	Port pins (P0_x, P1_x) Input hysteresis (V_{T+}-V_{T-})	V_{CCP} = 5.5V	0.3	0.38	-	V
		V_{CCP} = 3.0 V	0.22	0.32	-	
		V_{CCP} = 1.65 V	0.15	0.29	-	
		V_{CCP} = 1.4 V, 0°C to 110°C	0.15	0.29	-	

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Table 6: Electrical Characteristics: General

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH_P}	Port pin output high voltage, all port pins sourcing same current	V_{CCP} = 5.5 V, I_{OH_P} = -25mA	4.55	4.96	-	V
		V_{CCP} = 3.0 V, I_{OH_P} = -25mA	1.8	2.33	-	
		V_{CCP} = 5.5 V, I_{OH_P} = -10mA	5.1	5.27	-	
		V_{CCP} = 3.0 V, I_{OH_P} = -10mA	2.5	2.73	-	
		V_{CCP} = 1.65 V, I_{OH_P} = -10mA	0.9	1.25	-	
		V_{CCP} = 1.4 V, I_{OH_P} = -4mA, 0°C to 110°C	1.05	1.22	-	
V_{OL_P}	Port pin output low voltage, all port pins sinking same current	V_{CCP} = 5.5 V, I_{OL_P} = 25mA	-	0.27	0.43	V
		V_{CCP} = 3.0 V, I_{OL_P} = 25mA	-	0.31	0.57	
		V_{CCP} = 5.5 V, I_{OL_P} = 10mA	-	0.12	0.2	
		V_{CCP} = 3.0 V, I_{OL_P} = 10mA	-	0.13	0.22	
		V_{CCP} = 1.65 V, I_{OL_P} = 10mA	-	0.17	0.34	
		V_{CCP} = 1.4 V, I_{OL_P} = 4mA, 0°C to 110°C	-	0.08	0.16	
V_{OH_I}	MISO pin output high voltage	V_{CCI} = 5.5 V, I_{OH_I} = -25mA	4.9	5.0	-	V
		V_{CCI} = 3.0 V, I_{OH_I} = -25mA	2.15	2.4	-	
		V_{CCI} = 5.5 V, I_{OH_I} = -10mA	5.25	5.3	-	
		V_{CCI} = 3.0 V, I_{OH_I} = -10mA	2.65	2.75	-	
		V_{CCI} = 1.65 V, I_{OH_I} = -10mA	1.05	1.3	-	
		V_{CCI} = 1.4 V, I_{OH_I} = -4mA, 0°C to 110°C	1.16	1.22	-	
V_{OL_I}	INTB, MISO, SDA pins output low voltage	V_{CCI} = 5.5 V, I_{OL_I} = 25mA	-	0.19	0.3	V
		V_{CCI} = 3.0 V, I_{OL_I} = 25mA	-	0.23	0.42	
		V_{CCI} = 5.5 V, I_{OL_I} = 10mA	-	0.08	0.13	
		V_{CCI} = 3.0 V, I_{OL_I} = 10mA	-	0.09	0.18	
		V_{CCI} = 1.65 V, I_{OL_I} = 10mA	-	0.13	0.26	
		V_{CCI} = 1.4 V, I_{OL_I} = 4mA, 0°C to 110°C	-	0.06	0.12	
I_{OH_P}	Port pin output high current	V_{CCP} = 5.5V, V_{OH_P} = 5.1V	-	-21	-13	mA
		V_{CCP} = 3.0 V, V_{OH_P} = 2.6 V	-	-17	-9	
		V_{CCP} = 1.65 V, V_{OH_P} = 1.25 V	-	-11	-4.5	
		V_{CCP} = 1.4 V, V_{OH_P} = 1V, 0°C to 110°C	-	-9	-3	
I_{OL_P}	Port pin output low current	V_{CCP} = 5.5 V, V_{OL_P} = 0.4 V	28	52	-	mA
		V_{CCP} = 3.0 V, V_{OL_P} = 0.4 V	22	43	-	
		V_{CCP} = 1.65 V, V_{OL_P} = 0.4 V	14	28	-	
		V_{CCP} = 1.4 V, V_{OL_P} = 0.4 V, 0°C to 110°C	10	22	-	

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Table 7: Electrical Characteristics: General

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IP}	Input leakage on RESETB, A0-A3, and any port pin configured as an input	V_I = 5.5V or V_{SS} T_j = 25°C	-1	-	1	uA
		V_I = 5.5 V or V_{SS} T_j = 125°C	-18	-	2	
I_{OH_I}	MISO pin output high current	V_{CCI} = 5.5V, V_{OH_I} = 5.1V	-	-21	-13	mA
		V_{CCI} = 3.0 V, V_{OH_I} = 2.6 V	-	-17	-9	
		V_{CCI} = 1.65 V, V_{OH_I} = 1.25 V	-	-11	-4.5	
		V_{CCI} = 1.4 V, V_{OH_I} = 1 V, 0°C to 110°C	-	-9	-3	
I_{OL_I}	INTB, MISO pins, output low current	V_{CCI} = 5.5 V, V_{OL_I} = 0.4 V	28	52	-	mA
		V_{CCI} = 3.0 V, V_{OL_I} = 0.4 V	22	43	-	
		V_{CCI} = 1.65 V, V_{OL_I} = 0.4 V	14	28	-	
		V_{CCI} = 1.4 V, V_{OL_I} = 0.4, 0°C to 110°C	10	22	-	
I_{VCCI_Q}	Quiescent supply current into V_{CCI}	V_{CCI} = 5.5 V, all ports inputs tied to V_{SS} or 5.5 V, no communications, TID = 0 krad T_j = 25°C	-	216	300	uA
		V_{CCI} = 5.5 V, all ports inputs tied to V_{SS} or 5.5 V, no communications, TID = 0 krad T_j = 125°C	-	358	1560	
I_{VCCP_Q}	Quiescent supply current into V_{CCP}	V_{CCP} = 5.5 V, all ports inputs tied to V_{SS} or 5.5 V, no communications, TID = 0 krad T_j = 25°C	-	28	50	uA
		V_{CCP} = 5.5 V, all ports inputs tied to V_{SS} or 5.5 V, no communications, TID = 0 krad T_j = 125°C	-	63	415	
C_{IP}	Port pin capacitance when port configured as input(1)		-	11.5	-	pF
t_{V_INTB}	Time from change on input port to INTB valid		500	-	1500	ns
t_{RESET_W}	Required RESETB pulse width		200	-	-	ns
t_{RESET_R}	Recovery from RESETB		300	-	-	ns
t_{RESET_A}	Time for RESETB to affect ports	-	-	-	200	ns

(1) not tested in production

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Table 8: Electrical Characteristics: I2C/SMBUS operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
The following are from the I²C bus protocol and apply to the host interface						
I_{OL_SDA}	I²C SDA pin low level sink current	V_{SDA} = 0.4V, V_{CCI} = 3.0 V	20	37	-	mA
		V_{SDA} = 0.4 V, V_{CCI} = 1.65 V	8	19	-	
		V_{SDA} = 0.4 V, V_{CCI} = 1.4 V, 0°C to 110°C	6	14	-	
C_I	SCL, SDA input capacitance[1]		-	11.5	-	pF
f_{SCL}	SCL clock frequency	V_{CCI} = 3.0	-	-	1000	kHz
		V_{CCI} = 1.65 V	-	-	400	
		V_{CCI} = 1.4 V, 0°C to 110°C	-	-	100	
t_{SCH}	SCL high time		260	-	-	ns
t_{SCL}	SCL low time		500	-	-	ns
t_{SP}	SCL, SDA maximum width of spike suppressed by input filter		50	-	200	ns
t_{SDS_I2C}	Data setup time	V_{CCI} = 3.0	50	-	-	ns
		V_{CCI} = 1.65	100	-	-	
		V_{CCI} = 1.4 V, 0°C to 110°C	250	-	-	
t_{SDH_I2C}	Data hold time		-	-	0	ns
t_{ICR_I2C}	Input rise time		-	-	120	ns
t_{ICF_I2C}	Input fall time		-	-	120	ns
t_{BUF}	Bus free time between stop and start		500	-	-	ns
t_{STS}	Start or repeated start setup time		260	-	-	ns
t_{STH}	Start or repeated start hold time		260	-	-	ns
t_{SPS}	Stop setup time		260	-	-	ns
t_{VD}	SCL low to valid data		450	-	-	ns
t_{VDACK}	SCL low to valid ACK		450	-	-	ns
The following are device-specific I²C interface specifications for the APIO16/AFIO16						
$t_{RST_INTB_I2C}$	Read of input port to INTB valid		500	-	1550	ns
t_{VQ_I2C}	Write of output port to port valid		70	-	400	ns
t_{SUDP_I2C}	Setup data on port before read		-	-	0	ns
t_{HDP_I2C}	Hold data on port after read		-	-	300	ns

[1] not tested in production

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Table 9: Electrical Characteristics: SPI operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCLK}	SCLK clock frequency	V_{CCI} = 3.0 V	-	-	25	MHz
		V_{CCI} = 1.65 V	-	-	10	
		V_{CCI} = 1.4 V, 0°C to 110°C	-	-	2	
t_{HIGH}	Clock high time	1.65 V $\leq V_{CCI} \leq$ 5.5 V	15	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	50	-	-	
t_{LOW}	Clock low time	1.65 V $\leq V_{CCI} \leq$ 5.5 V	15	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	50	-	-	
t_{SU_CSB}	CSBx setup time before first SCLK rising edge	1.65 V $\leq V_{CCI} \leq$ 5.5 V	50	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	50	-	-	
t_{H_CSB}	CSBx hold time after last SCLK falling edge	1.65 V $\leq V_{CCI} \leq$ 5.5 V	50	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	50	-	-	
$t_{SU_DAT_SPI}$	Data setup time for SPI interface	1.65 V $\leq V_{CCI} \leq$ 5.5 V	25	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	25	-	-	
$t_{HD_DAT_SPI}$	Data hold time for SPI interface	1.65 V $\leq V_{CCI} \leq$ 5.5 V	5	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	5	-	-	
$t_{RST_INTB_SPI}$	Time from read of input port to INTB valid	1.65 V $\leq V_{CCI} \leq$ 5.5 V	500	-	1500	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	500	-	1500	
$t_{V_Q_SPI}$	Time from write of output port to port valid	1.65 V $\leq V_{CCI} \leq$ 5.5 V	-	-	400	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	-	-	400	
$t_{SU_DP_SPI}$	Setup time for data on port before read from port	1.65 V $\leq V_{CCI} \leq$ 5.5 V	100	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	100	-	-	
$t_{H_DP_SPI}$	Hold time for data on port after read from port	1.65 V $\leq V_{CCI} \leq$ 5.5 V	100	-	-	ns
		V_{CCI} = 1.4 V, 0°C to 110°C	100	-	-	
t_{VD_SPI}	Time from falling edge of SCLK to valid data on MISO	3.0 V $\leq V_{CCI} \leq$ 5.5 V	10	-	25	ns
		1.65 V $\leq V_{CCI} <$ 3.0 V	10	-	50	
		V_{CCI} = 1.4V, 0°C to 110°C	20	-	100	
t_{DIS_MISO}	Time from CSBx rising to high impedance on MISO	1.65 V $\leq V_{CCI} \leq$ 5.5 V	-	-	100	ns
		V_{CCI} = 1.4V, 0°C to 110°C	-	-	100	

(1) not tested in production

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5 TYPICAL CHARACTERISTICS

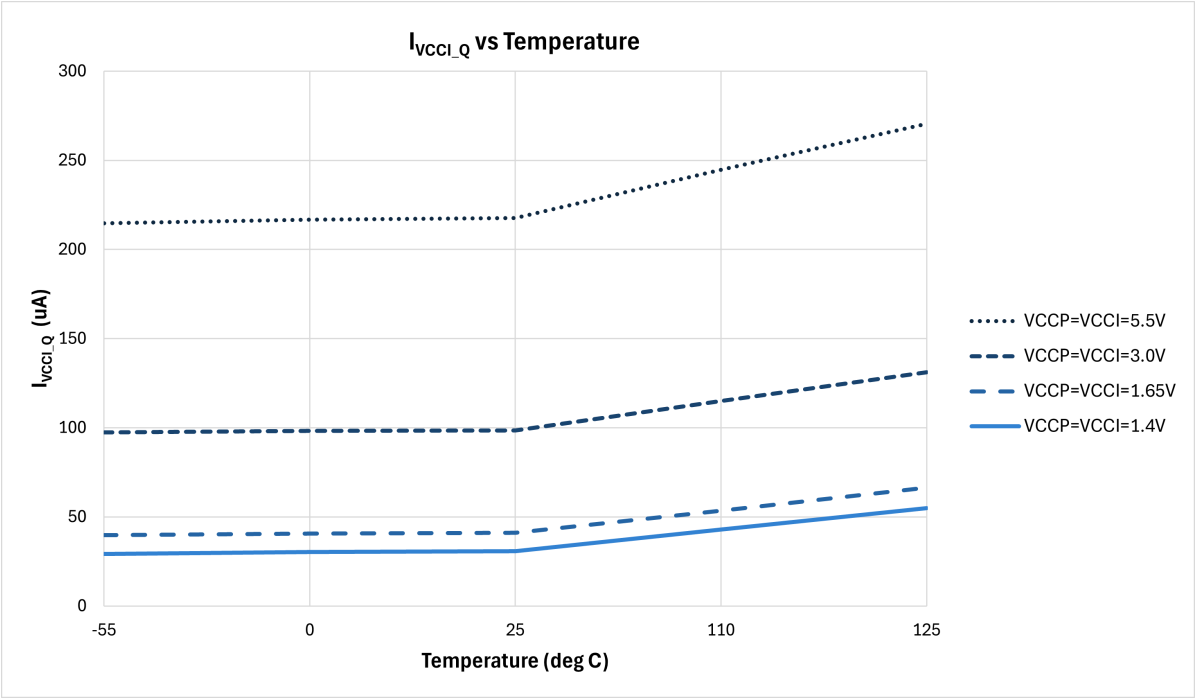

Figure 2: V_{CCI_Q} vs Temperature

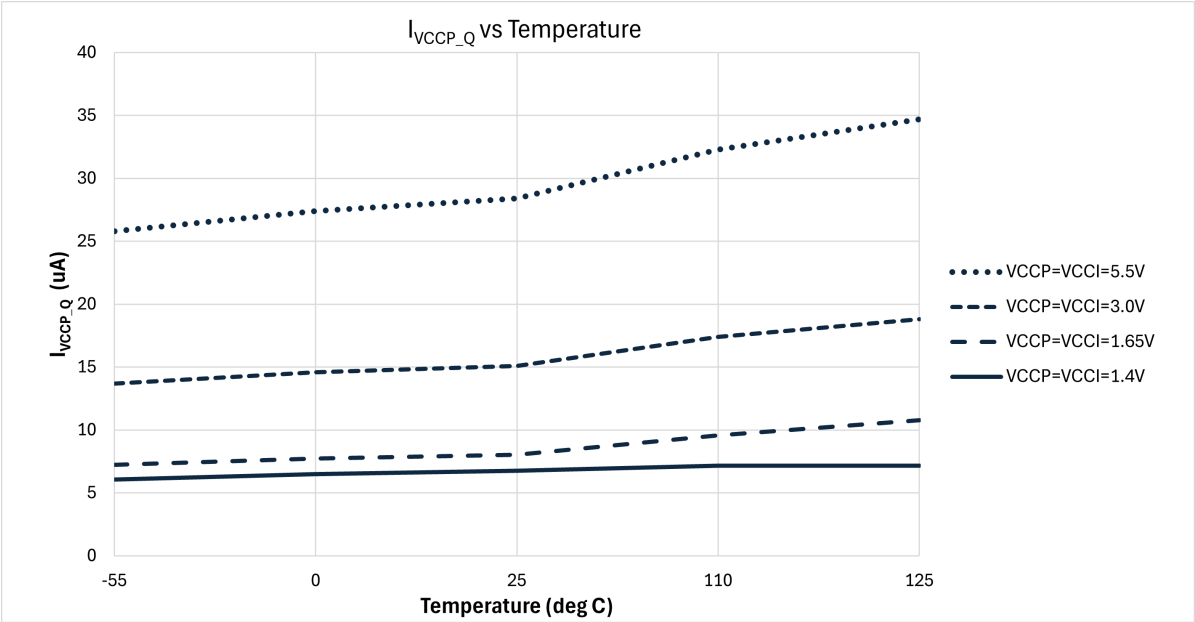

Figure 3: V_{CCP_Q} vs Temperature

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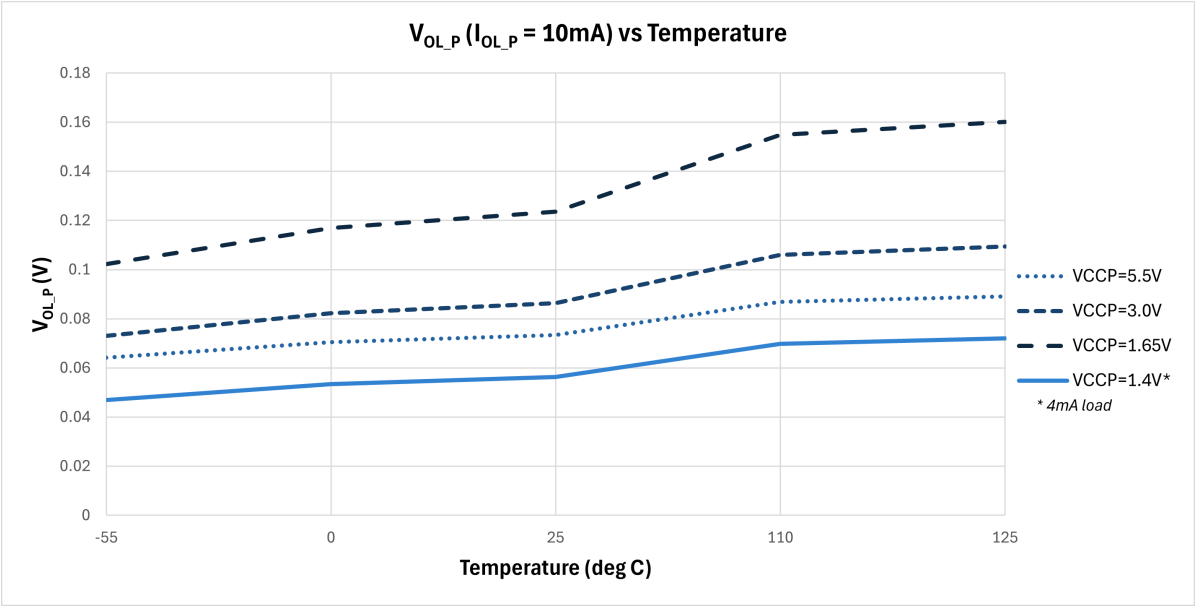

Figure 4: V_{OL_P} vs Temperature

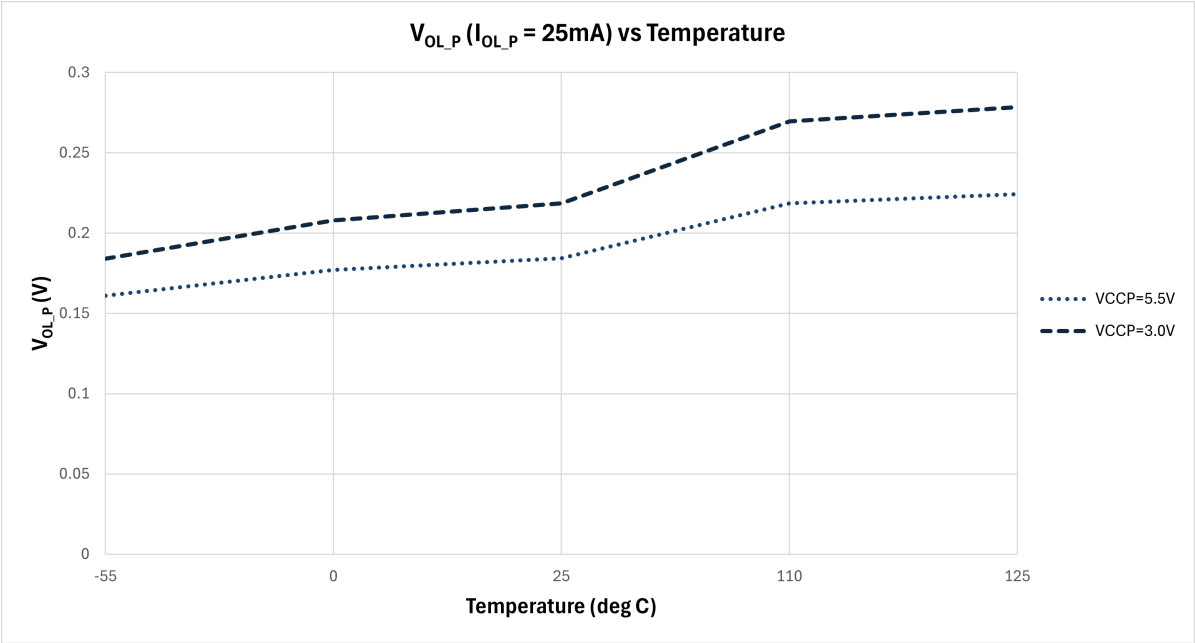

Figure 5: V_{OL_P} vs Temperature

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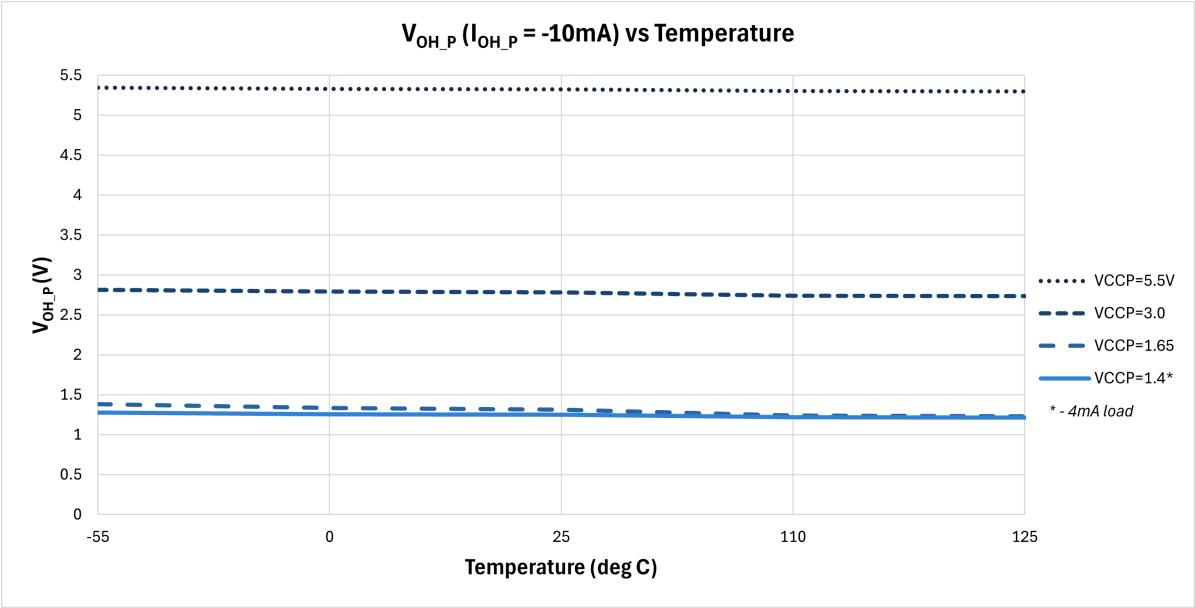

Figure 6: V_{OH_P} vs Temperature

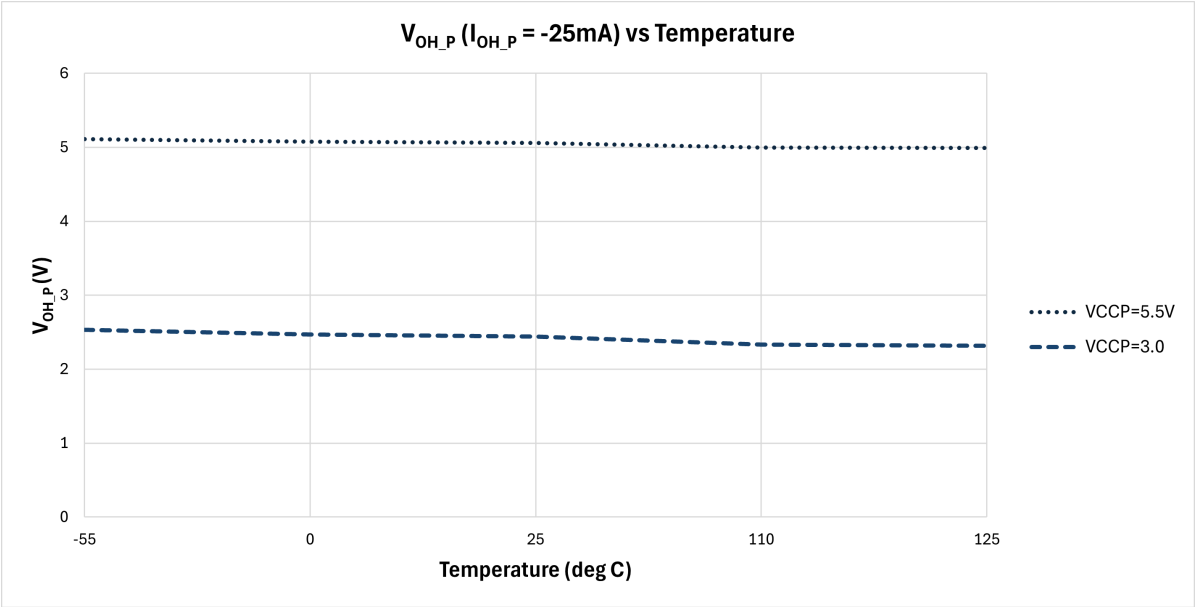

Figure 7: V_{OH_P} vs Temperature

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Figure 8 shows the leakage current expected when an unused port pin is left floating (not pulled high or low).

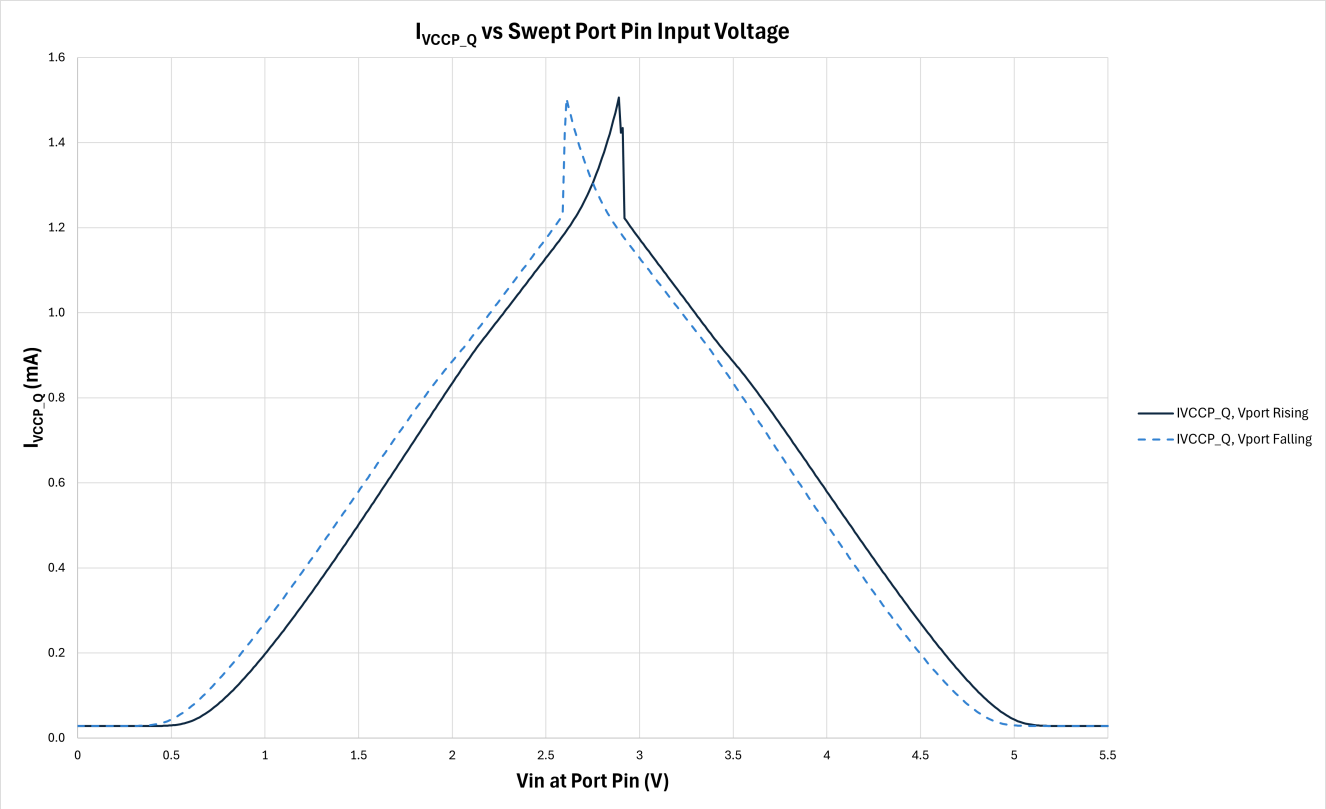

Figure 8: I_{VCCP_Q} vs swept port voltage

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6 DETAILED DESCRIPTION

6.1 OVERVIEW

The APIO16/AFIO16 provides robust and flexible I/O expansion capabilities with voltage level translation, ensuring reliable operation across varying supply voltages. The architecture supports two independent supply rails: V_{CCI} powers the serial interface logic, while V_{CCP} powers the I/O ports. This separation enables seamless interfacing between low-voltage microcontrollers and higher voltage peripherals. The device implements an SMBUS compatible I^2C or SPI based serial bus with two 8-bit ports which can be controlled or read by an external host on the bus.

6.2 FUNCTIONAL BLOCK DIAGRAM

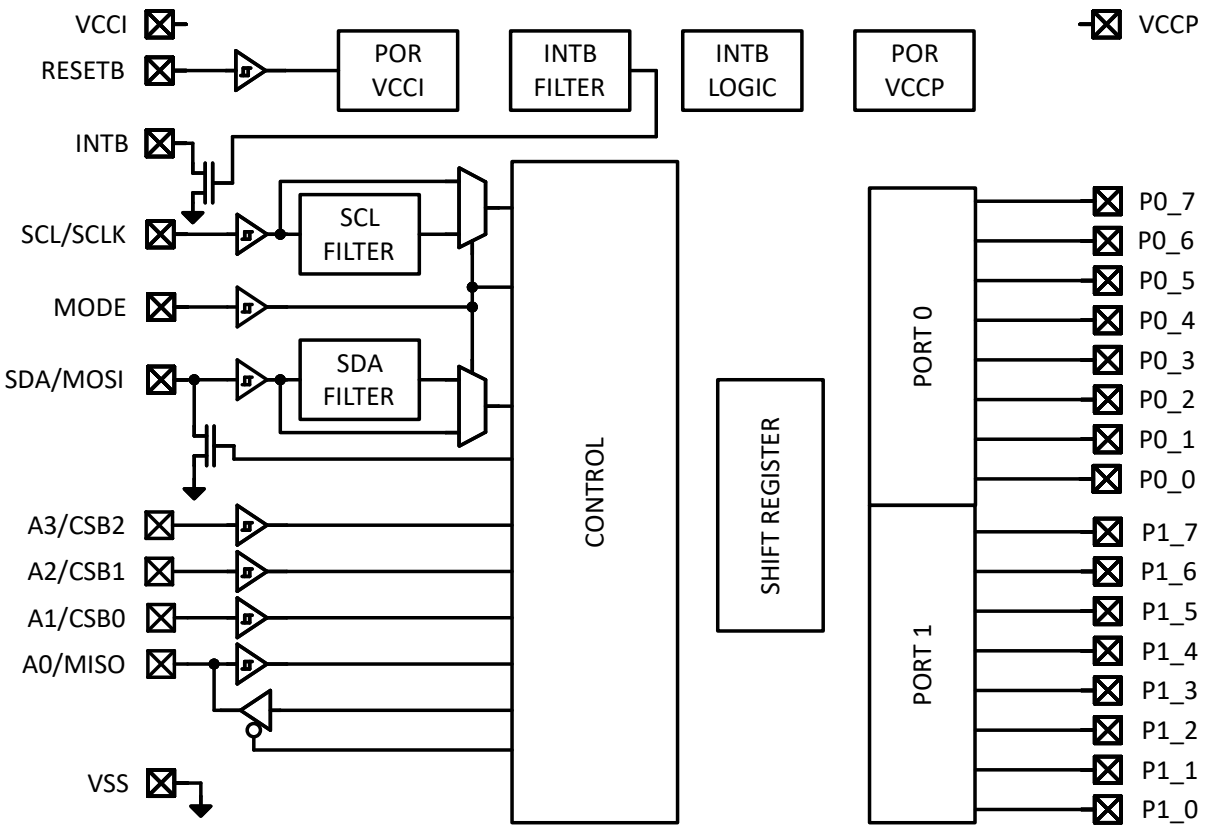

Figure 9: Block diagram

6.3 DETAILED FUNCTIONAL MODES

6.3.1 Power-On Reset (POR) V_{CCI}

The device incorporates independent POR circuits on V_{CCI} and V_{CCP} supplies. If V_{CCI} drops below the threshold V_{CCI_STOP}, all internal registers are reset to default power up states with ports being set to high impedance input mode. With the proprietary cold sparing circuitry on all inputs and outputs the V_{CCI} POR assertion will allow the device to operate in a cold spare configuration presenting high impedance on all serial interface and port pins.

The serial interface cannot be programed until V_{CCI} is above the V_{CCI_START} threshold and RESETB is not asserted.

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6.3.2 Power-On Reset (POR) V_{CCP}

When V_{CCP} is below the V_{CCP_STOP} threshold, the POR is asserted forcing all the ports into a high-impedance state. This enables cold sparing on the output ports independent of V_{CCI} or the serial interface or register settings. If V_{CCI} is in recommended operating range and V_{CCP} POR asserted, the device can be programmed to desired states without impacting port pins during programming. V_{CCP} POR does not clear or reset the serial interface state or internal configuration. Once V_{CCP} is above $\mathbf{V_{CCP_START}}$ threshold, the ports return to the states dictated by the register states.

6.3.3 RESETB

RESETB is an active-low input that resets the device's internal logic and registers. RESETB assertion is identical to V_{CCI} POR assertion with all inputs and outputs in high impedance state. The serial interface is not programmable until both RESETB and V_{CCI} POR are de-asserted. If external control is not needed, RESETB should be tied to V_{CCI} directly, or through pull-up resistor. RESETB provides a software-controlled reset alternative to power cycling.

6.3.4 MODE

The MODE pin selects between I^2C /SMBUS and SPI modes. Tie MODE low for I^2C operation or high for SPI mode. The MODE state should remain constant during operation. Tying MODE pin to V_{CCI} or V_{SS} ensures MODE is in valid state when V_{CCI} POR deasserts.

6.3.5 PORTS

The device features two 8-bit ports: P0 and P1. Both ports are configurable as inputs or outputs via configuration registers on a per-bit basis. Outputs can source or sink up to 25 mA per pin. Schmitt triggers on inputs provide enhanced noise immunity, and a polarity inversion register enables flexible logic level handling by allowing ports to be read with inverted values.

Port pins P0_0 through P0_7 and P1_0 through P1_7 are configurable as inputs or outputs on a per-pin basis. When configured as input, it is recommended that these pins be either actively driven or connected to appropriate pull-up or pull-down resistors to prevent floating inputs and minimize undesirable leakage current as shown in Figure 8. A detailed schematic of the internal circuitry for each port pin is shown in Figure 10.

The ports are 5 V tolerant and can be driven up to 5.5 V when in high-impedance input mode, independent of the V_{CCP} supply voltage.

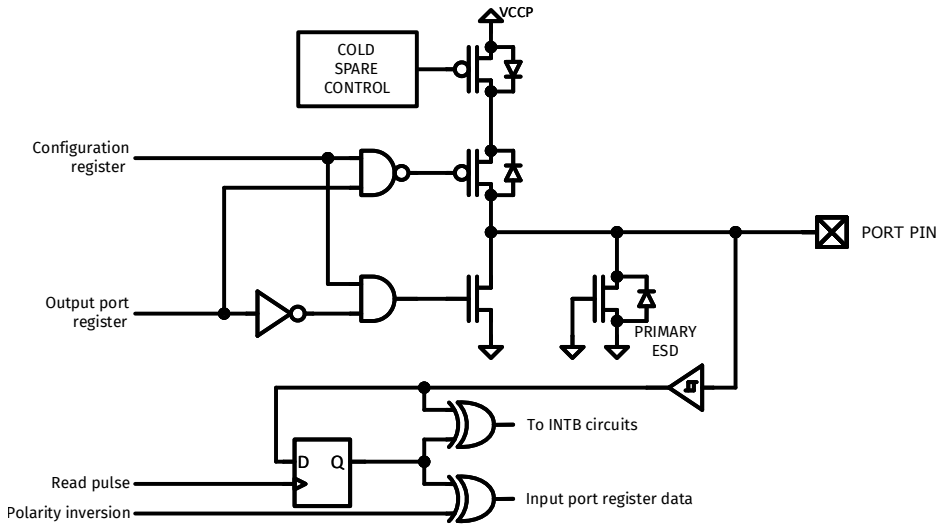

Figure 10: Simplified Port pin schematic

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6.3.6 INTB

INTB is an open-drain output that asserts low when an input state change is detected. After a RESETB or VCCI POR assertion, the port must be read to initialize the port for interrupt detection. The interrupt clears upon reading the affected input port. INTB incorporates an internal 750ns filter to debounce spurious signals. INTB can be used to trigger an interrupt on the host controller to query the port and read new input information. If INTB functionality is not required, it is recommended to tie it to V_{SS} directly, or via a weak pull-down.

6.4 I²C OPERATION

APIO16/AFIO16 operates as a target device in I²C mode. I²C operation is enabled when the MODE pin is pulled to a logic low level. The interface supports 16 unique hard wired I²C addresses via address pins A3/CSB2, A2/CSB1, A1/CSB0 and A0/MISO. These pins set the address bits A3, A2, A1 and A0 respectively. The interface is compliant with I²C Fast-Mode Plus (1 MHz), and SMBUS 3.2. The SCL/SCLK pin functions as the SCL input pin and SDA/MOSI pin functions as the SDA bidirectional pin. Both SCL, and SDA include filters to suppress glitches less than 50ns to ensure reliable operation.

The I²C interface uses a standard START condition followed by the 7-bit device address and a read/write bit (r/wb). On a write operation, the controller then sends the register address and an 8-bit data value. On a read operation, a repeated START condition must be issued (or a STOP followed by a START), followed by the device address with the read bit set. The APIO16/AFIO16 responds with the requested data byte. Reads can be terminated by sending a NACK. During port reads, the input state is latched during the ACK preceding the data transfer, ensuring reliable sampling. See Figures 11 to 14 for detailed timing specifications.

The seven bit I²C device address options are listed in Table 10. Each I²C command contains a 7-bit device address (dad[6:0]). If the address in the I²C command matches the device address selected by the address pins on the device, the device will respond to the I²C command. Otherwise, the device will ignore the command.

Table 10: APIO16/AFIO16 I²C Address

ADDRESS PINS				I²C ADDRESS
A3	A2	A1	A0	(HEX)
L	L	L	L	20
L	L	L	H	21
L	L	H	L	22
L	L	H	H	23
L	H	L	L	24
L	H	L	H	25
L	H	H	L	26
L	H	H	H	27
H	L	L	L	28
H	L	L	H	29
H	L	H	L	2A
H	L	H	H	2B
H	H	L	L	2C
H	H	L	H	2D
H	H	H	L	2E
H	H	H	H	2F

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6.4.1 I²C timing diagrams

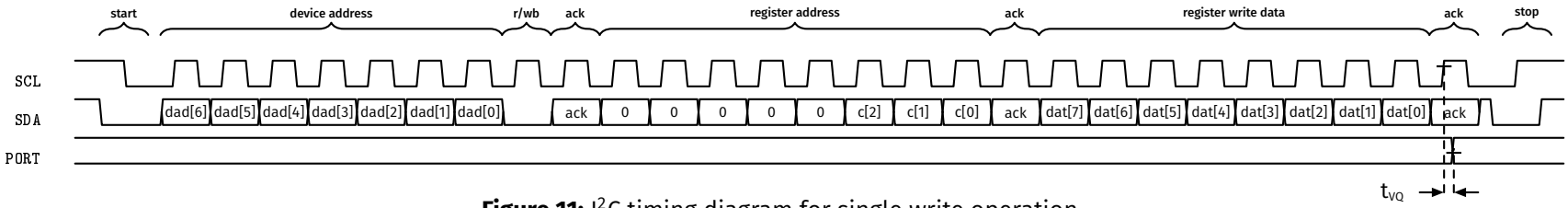

Figure 11: I²C timing diagram for single write operation

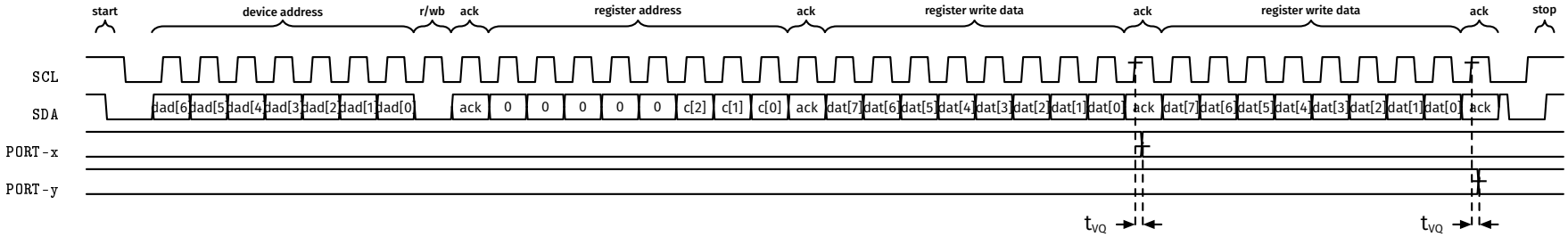

Figure 12: I²C timing diagram for two write operations

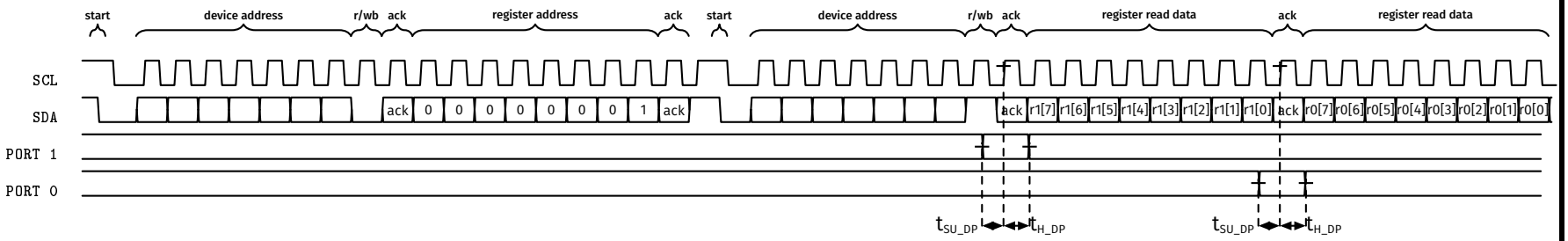

Figure 13: I²C port read timing specifications

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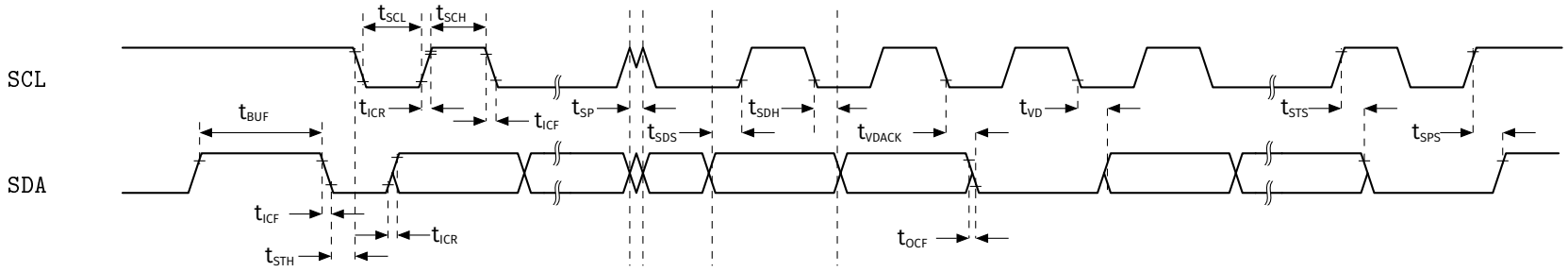

Figure 14: I²C timing specifications

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6.4.2 I²C write

The I²C write operation allows the controller to update the internal registers of the APIO16/AFIO16 device. Communication begins with a START condition, signaling the beginning of a transmission. The controller sends the 7-bit device address with the least significant bit (LSB) set to '0' to indicate a write. The device acknowledges by pulling the SDA line low during the following clock cycle (ACK).

Next, the controller sends the target register address (three bits C2:C0), which the device acknowledges with an ACK. This is followed by the data byte to be written into the selected register. Once the data is transmitted and acknowledged, the controller sends a STOP condition to complete the transaction.

The data becomes active in the addressed register shortly after the STOP condition is received. If additional bytes are sent without a STOP, the device interprets them as sequential register writes. Sequential writes will toggle between the same register function, but for the other port. For example, first write to register 2 (output register port 0), the second write would go to register 3 (output register port 1). The next sequential write would be back to writing to register 2.

Refer to Figure 11 for single I²C write, Figure 12 for sequential I²C writes and Table 11 for APIO16/AFIO16 register definitions.

I²C Write Sequence:

1. START condition
2. 7-bit device address + write bit (0)
3. ACK from APIO16/AFIO16
4. 8-bit Register address (C2:C0 bits) with five MSB bits 0 padded.
5. ACK
6. Data byte
7. ACK
8. STOP condition

6.4.3 I²C read

Reading from the APIO16/AFIO16 involves a two-part sequence: a write phase to specify the register address, followed by a read phase to obtain the data. The controller begins with a START condition and sends the device address with the write bit (0), followed by the target register address. After the device acknowledges, a repeated START is issued.

In the second phase, the controller sends the device address again, this time with the read bit (1). The device responds by placing the register data on the SDA line, which the controller reads. The controller must acknowledge (ACK) each byte it receives or send a NACK after the final byte to indicate the end of the read sequence, followed by a STOP condition.

Data is latched into the device's output buffer just before transmission triggered from the rising edge of SCL of the ACK cycle. Thus, ensuring stability and accurate reads even in noisy environments.

Sequential reads will toggle between the same register function, but for the other port. For example, first read from register 1 (Input register port 1), the second read would return register 0 (Input register port 0). The next sequential read would be back to reading register 1.

Refer to Figures 14 and 13 for I²C read timing diagram, and Table 11 for APIO16/AFIO16 register definitions.

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I^2C Read Sequence:

1. START condition
2. 7-bit device address + write bit (0)
3. ACK from APIO16/AFIO16
4. Register address
5. ACK
6. Repeated START
7. 7-bit device address + read bit (1)
8. ACK
9. Data from APIO16/AFIO16 (MSB first)
10. ACK (for additional bytes) or NACK (to end), followed by STOP

6.5 SPI OPERATION

SPI mode supports 3 chip-select lines A3/CSB2, A2/CSB1, and A1/CSB0 functioning as CSB2, CSB1 and CSB0 respectively for multi-device configurations. It is compatible with SPI clock speeds up to 25 MHz ($V_{CCI} > 3$ V). MISO provides tri-state output, enabling shared bus operation.

6.5.1 SPI Protocol Overview

The SPI interface on the APIO16/AFIO16 device operates in a standard full-duplex configuration, using four signals: SCL/SCLK (clock), SDA/MOSI (controller-to-device data), A0/MISO (device-to-controller data), and CSBx (active-low chip selects). The SPI mode supported is Mode 0 (CPOL = 0, CPHA = 0), where data is sampled on the rising edge of SCLK and output on the falling edge.

Each SPI transaction begins by pulling all of the chip select lines (CSB0-CSB2) low. While the chip select is active, the controller sends a control byte followed by the data byte (for writes) or dummy bits (for reads). Data is shifted MSB first. The device expects an 8-bit control byte consisting of register address bits (C2:C0), read/write indicator, and protocol-specific format padding. After the command byte is received, the data phase begins.

The APIO16/AFIO16 device will ignore data on MOSI unless all three of chip selects (CSB0, CSB1 and CSB2) are low. CSBx is used in the following sections to represent the boolean logical function:

CSBx = (CSB0 OR CSB1 OR CSB2), the statement: "CSBx is low" will be taken to mean that all three of CSB0, CSB1 AND CSB2 are low simultaneously.

The controller must ensure proper SCLK frequency and timing to meet setup and hold times. Once the data phase is complete, deasserting CSBx signals the end of the transaction, and MISO returns to a high-impedance state. Refer to the SPI timing diagram in Figure 15 for an example of SPI write operation.

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6.5.2 SPI timing diagrams

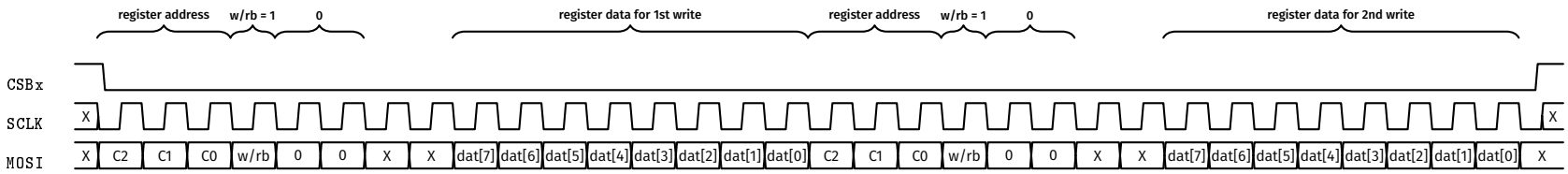

Figure 15: SPI timing specifications

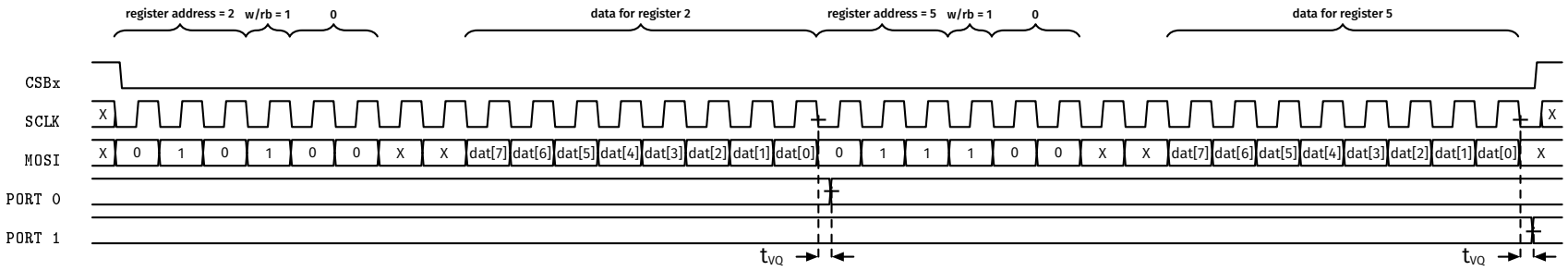

Figure 16: SPI example write register 2 then write register 3

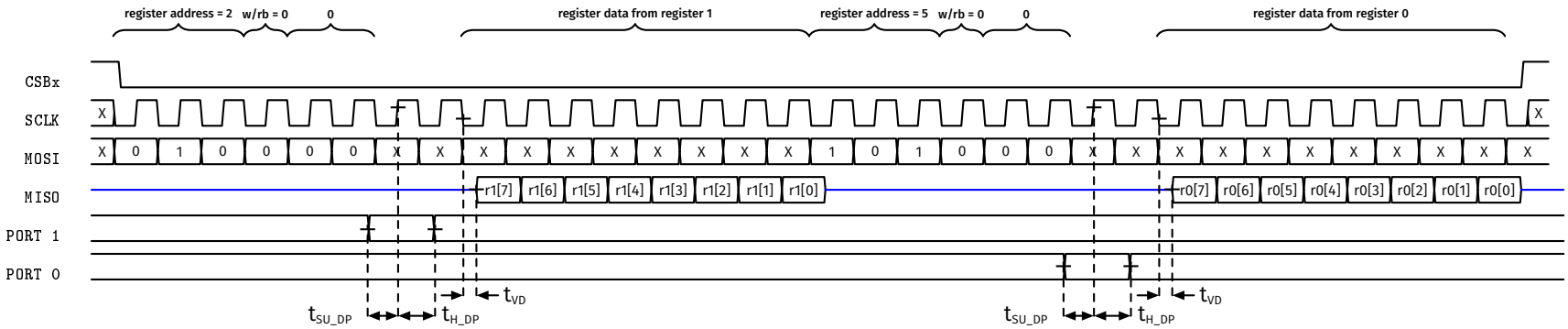

Figure 17: SPI example read register

Note: Blue on MISO represents "High Impedance"

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6.5.3 SPI write

The SPI write operation is initiated by asserting the all of chip-select lines (CSBx) low. Communication occurs on the rising edge of the SPI clock (SCLK), where data is shifted into the APIO16/AFIO16 on the MOSI line. The controller sends a command byte structured as follows: the first bits specify the register address (C2:C0), followed by a write bit (w/rb = 1), two reserved bits which must both be zeros, and two "don't care" bits. This is immediately followed by the 8-bit data payload to be written to the target register. **Note:** that the polarity of the w/rb bit is opposite from the I^2C r/wb bit polarity with a write being a logic high.

The APIO16/AFIO16 latches the data after the final bit is clocked in and commits the new value after a brief setup delay $\mathbf{t_{VQ}}$. The chip-select line must remain low during the entire sequence. For continuous writes, CSBx can stay low across multiple transfers. If CSBx is deasserted between operations, each write sequence must begin with a new command word.

6.5.4 SPI read

To read from the APIO16/AFIO16 via SPI, the controller first pulls the CSBx lines low and transmits an address/control byte on the MOSI line. This byte contains the register address (C2:C0) along with a read bit (w/rb = 0), two reserved bits which must both be zeros, and additional "don't care" bits. Once the address phase is complete, the device outputs the register contents onto the MISO line, aligned with the falling edges of the SPI clock.

MISO remains actively driven during the 8-bit transfer and returns to high impedance once the byte is complete and CSBx is deasserted. The timing requirements ensure the register value is available with sufficient setup and hold times relative to SCLK transitions. SPI reads are single-transaction cycles unless the CSBx remains low and additional registers are addressed in a burst sequence. Refer to SPI read timing diagram in Figure 17 showing a multiple read transaction with a single CSBx assertion.

Note: the polarity of the w/rb used in SPI is the opposite to the polarity used in I^2C

6.5.5 SPI read 4-wire

Multiple **APIO16/AFIO16** devices can be connected to the same MISO line. As long as only ONE **APIO16/AFIO16** device is requested to send back data at a time, there will be no bus conflicts on the MISO line. It is recommended to connect a pull-up or pull-down resistor onto the MISO line, to ensure that it does not float when device is inactive and MISO is not being driven from the device.

6.5.6 SPI read 3-wire

It is also possible to short the MISO and MOSI pins together and connect multiple devices to the same wire, provided both of the following conditions are met:

- Only one **APIO16/AFIO16** device is requested to send back data at a time.
- The controller tri-states its output driving the joined MISO/MOSI line at the appropriate time to ensure the controller and Target are not both driving the same line at the same time.

6.5.7 SPI read from port

In SPI mode, when reading from the port pins, the state of the port pins is latched on the 3rd rising SCLK edge after the w/rb bit is latched. To guarantee correctly latching the expected data on the pins, the data must be stable $\mathbf{t_{SU_DP_SPI}}$ before and remain stable $\mathbf{t_{H_DP_SPI}}$ after that clock edge.

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6.6 REGISTER DESCRIPTIONS

The APIO16/AFIO16 contains eight internal registers that control and monitor the state of its two 8-bit I/O ports. These registers are accessible through both I^2C and SPI interfaces. These registers allow complete control of the bidirectional I/O ports, enabling readback, logical inversion, and dynamic reconfiguration per application needs.

Table 11: APIO16/AFIO16 registers

BIT NAME's			REGISTER	REGISTER	PROTOCOL	RESET
C2	C1	C0	NUMBER	NAME	TYPE	DEFAULT
0	0	0	0	Input port 0	read	xxxx xxxx
0	0	1	1	Input port 1	read	xxxx xxxx
0	1	0	2	Output port 0	read/write	1111 1111
0	1	1	3	Output port 1	read/write	1111 1111
1	0	0	4	Polarity port 0	read/write	0000 0000
1	0	1	5	Polarity port 1	read/write	0000 0000
1	1	0	6	Configuration port 0	read/write	1111 1111
1	1	1	7	Configuration port 1	read/write	1111 1111

6.6.1 Register 0

Reading register 0 returns the state of the pins on port 0. Writing to register 0 has no effect.

Table 12: Input port 0 register (c[2:0] = 0)

Bit	7	6	5	4	3	2	1	0
Pin Name	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0

6.6.2 Register 1

Reading register 1 returns the state of the pins on port 1. Writing to register 1 has no effect.

Table 13: Input port 1 register (c[2:0] = 1)

Bit	7	6	5	4	3	2	1	0
Pin Name	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0

6.6.3 Register 2

Register 2 controls the output drive state of port 0 pins when configured as outputs.

Table 14: Output port 0 register (c[2:0] = 2)

Bit	7	6	5	4	3	2	1	0
Pin Name	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
Default	1	1	1	1	1	1	1	1

6.6.4 Register 3

Register 3 controls the output drive state of port 1 pins when configured as outputs.

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Table 15: Output port 1 register (c[2:0] = 3)

Bit	7	6	5	4	3	2	1	0
Pin Name	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P0_0
Default	1	1	1	1	1	1	1	1

6.6.5 Register 4

Register 4 controls the polarity inversion settings for port 0. When this register has a bit is set to "1", the APIO16/AFIO16 will invert the bit value reported when a register 0 read is performed.

Table 16: Polarity port 0 register (c[2:0] = 4)

Bit	7	6	5	4	3	2	1	0
Pin Name	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
Default	0	0	0	0	0	0	0	0

6.6.6 Register 5

Register 5 controls the polarity inversion settings for port 1. When this register has a bit is set to "1", the APIO16/AFIO16 will invert the bit value reported when a register 1 read is performed.

Table 17: Polarity port 1 register (c[2:0] = 5)

Bit	7	6	5	4	3	2	1	0
Pin Name	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
Default	0	0	0	0	0	0	0	0

6.6.7 Register 6

Register 6 is the configuration register for port 0 and determines if each output is enabled. The output is enabled when a bit in this register is set to "0", then the port pin will drive the corresponding value in port 0's output register 2. With a bit set to "1", the port pin output is disabled and it will present a high impedance.

Table 18: Configuration port 0 register (c[2:0] = 6)

Bit	7	6	5	4	3	2	1	0
Pin Name	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
Default	1	1	1	1	1	1	1	1

6.6.8 Register 7

Register 7 is the configuration register for port 1 and determines if each output is enabled. The output is enabled when a bit in this register is set to "0", then the port pin will drive the corresponding value in port 1's output register 3. With a bit set to "1", the port pin output is disabled and it will present a high impedance.

Table 19: Configuration port 1 register (c[2:0] = 7)

Bit	7	6	5	4	3	2	1	0
Pin Name	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
Default	1	1	1	1	1	1	1	1

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6.7 APPLICATION CIRCUITS

Decoupling capacitors of at least 10 nF should be placed within 25 mm of the IC for both V_{CCI} and V_{CCP} supplies .

It is recommended that the INTB pin be properly pulled up or pulled down even when interrupt functionality is not used. This can be achieved by connecting INTB to a pull-up or pull-down resistor, tying it directly to V_{SS}, or connecting it to a pull-up resistor tied to a higher voltage rail than V_{CCI} (within the maximum allowable voltage limits for the INTB pin).

6.7.1 Basic I²C operation

Please see Figure 18. For basic I²C operation, all that is necessary is to tie the A0, A1, A2, A3 (pins A0-A3) high or low to program the desired target device address.

Ensure that SDA and SCL are connected to the I²C bus and have appropriately sized pull-up resistors somewhere on those lines. Decoupling capacitors of at least 10 nF should be within 25 mm of the IC.

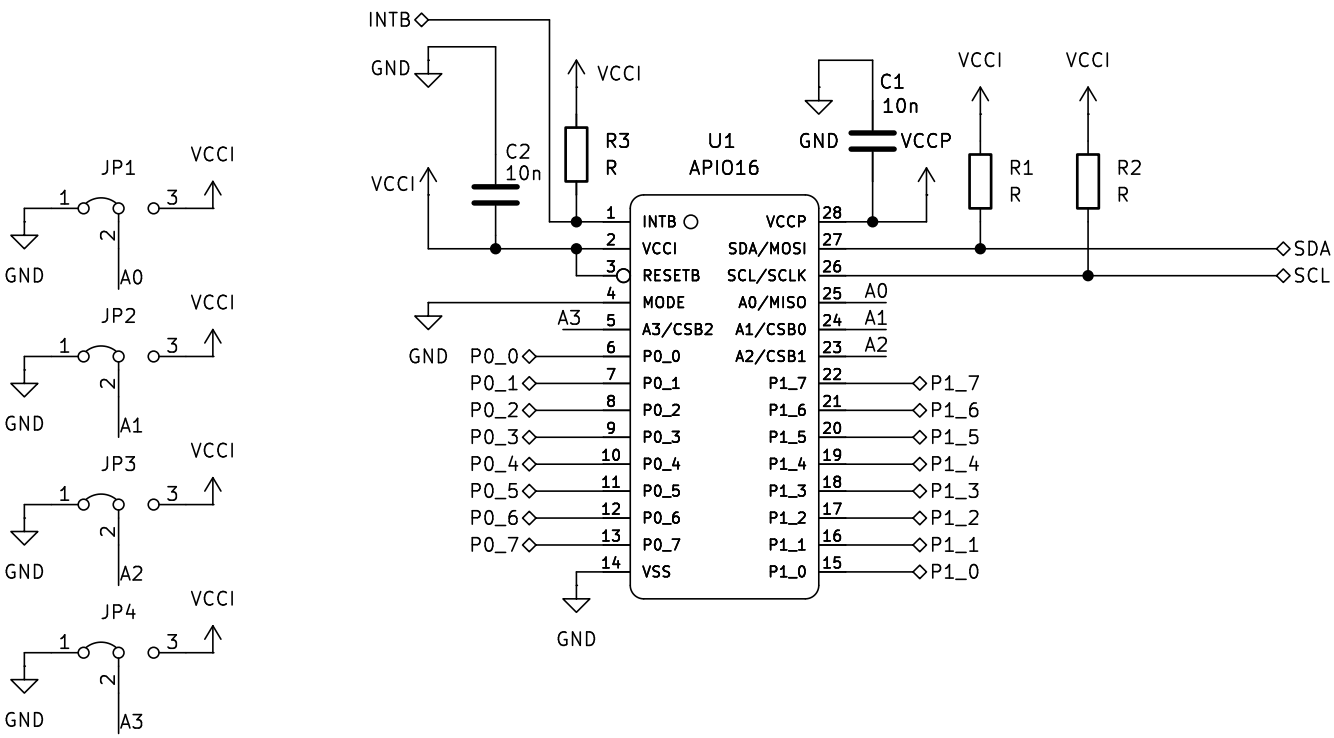

Figure 18: Basic I²C application

6.7.2 I²C connection to FPGA low voltage bank

Typically, modern FPGA I/Os are grouped in banks, each bank can be tied to a different power supply. It is often the case that not all pins on a low voltage bank are used. In this case there can be available IO resources that are un-used. Since the **APIO16/AFIO16** device has level translation built in, it is possible to use these pins to control the device. If the device is used in I²C mode, the SDA and SCL pins would be pulled up to the low voltage VCCI rail. **Note:** that INTB can be pulled up to a different, higher voltage if needed since it is an open drain output. The device can reliably support operation on V_{CCI} and/or V_{CCP} down to 1.4V.

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6.7.3 Sizing the pull-up resistors for SDA and SCLK for I²C

If the part is used in I²C mode, pull-up resistors are required on the SCL and SDA lines. The resistors must be small enough to meet the required speed of operation and large enough that all the components connected to the I²C bus can pull the lines down to a sufficiently low voltage.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of the pull-up resistors due to the maximum allowable rise time for the chosen speed of operation of the bus. Note that **APIO16/AFIO16** does not have a minimum operating speed. The controller may operate the bus at any speed slower than the maximum. Table 20 details the maximum allowable rise time for SDA and SCL to support certain standard bus speeds.

Table 20: Standard I²C bus speed requirements

SYMBOL	PARAMETER	STANDARD MODE	FAST MODE	FAST MODE PLUS	UNIT
$t_{r(max)}$	rise time of SDA and SCL (30% to 70% of VDDI)	1000	300	120	ns

Given that the $t_{r(max)}$ is specified for thresholds of 30% to 70%, the maximum pull-up resistance required can be calculated from the following equation:

$$\mathbf{R_{p(max)} = \frac{t_{r(max)}}{0.8473 \times C_b}} \tag{1}$$

The minimum pull-up resistance is limited due to the limited sink current of the devices on the bus, it can be calculated using:

$$\mathbf{R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}}} \tag{2}$$

Where V_{CC} represents the supply that the I²C pull-up resistors are connected to.

Once the maximum and minimum allowable value of R_P has been calculated, the designer is free to select a value between these two limits: towards the high end if low current consumption is required, towards the lower end if higher noise immunity is desired.

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6.7.4 Basic SPI operation

Please see Figure 19. For basic SPI operation, V_{CCI} is to be connected to the same power supply rail used by the controller driving the SPI bus. Only one CSBx pin is needed. In this example CSB0 is used from controller with CSB1 and CSB2 tied to V_{SS} .

If read-back via MISO is not required, the MISO pin can be left disconnected. It is recommended to tie the pin to V_{SS} or V_{CCI} with a pull up or pull down resistor in the range of 1 k to 10 k to prevent floating inputs.

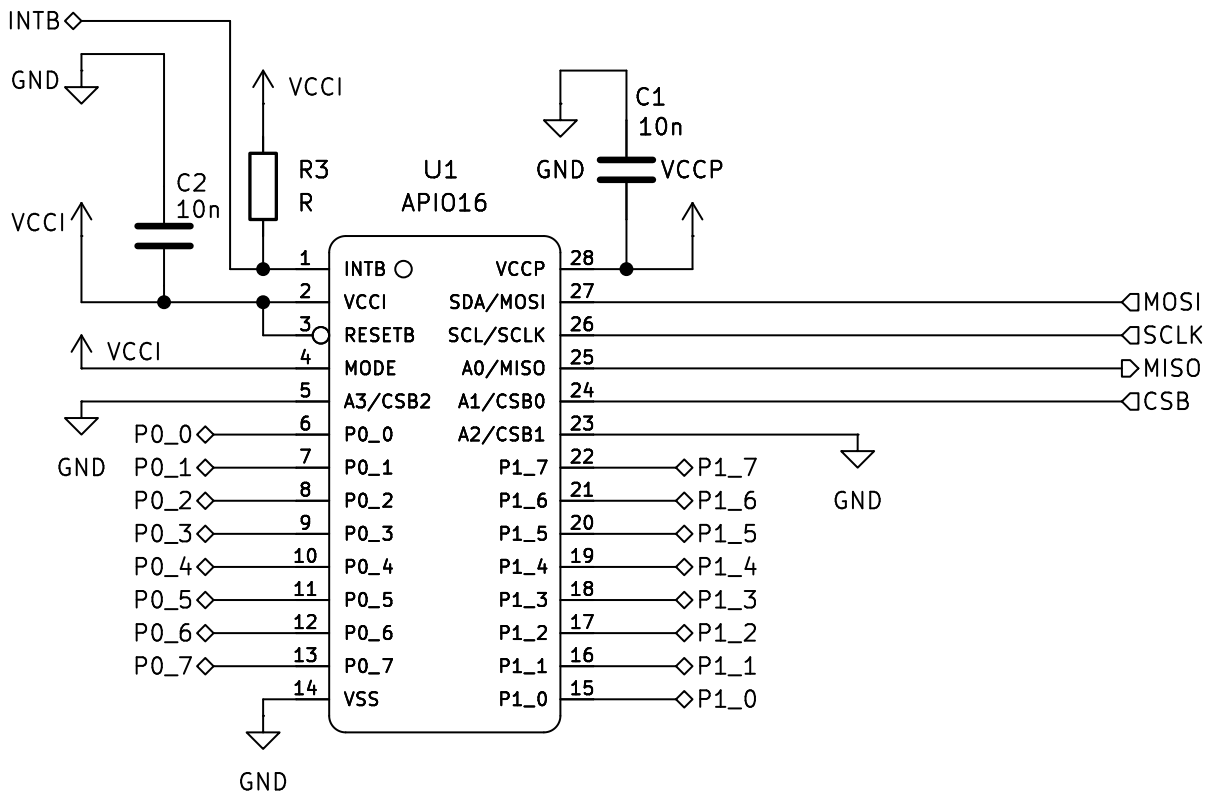

Figure 19: Basic SPI application

6.7.5 Using CSB0, CSB1, CSB2 to multiplex many devices in SPI mode

In SPI mode, the CSBx = CSB0 OR CSB1 OR CSB2: all the CSBx pins must be LOW to select the device. As a result, the extra CSBx pins can be used to enable selection of multiple **APIO16/AFIO16** devices with a minimum number of select lines and minimal external decoding. The Application Note Leveraging the APIO16: Practical Applications in Control, Sensing, and Power Management provides detailed application examples for the APIO16/AFIO16.

6.8 LAYOUT GUIDELINES

A decoupling capacitor of 10 nF to 100 nF should be connected between V_{CCI} and V_{SS} . This capacitor should be located within 25 mm of the IC. A similar capacitor should be placed between V_{CCP} and V_{SS}.

If the port pins are going to source large currents, it may be necessary to add additional capacitance from V_{CCP} to V_{SS} to minimize transients on power supply.

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6.9 ERROR HANDLING

In a high radiation environment, it is possible that the I^2C or SPI commands could become corrupted. The following section defines how the **APIO16/AFIO16** responds to various errors that may be present in the transactions.

6.9.1 I^2C illegal command

A valid command is an 8 bit word with the first five bits zero, the last three bits are the command itself. If any of the first five bits are not zeros, this will be detected as an illegal command. The device will ignore the command and wait until it detects a restart or a stop followed by a start or the device is reset by RESETB or a V_{CCI} POR.

6.9.2 I^2C controller acknowledge fail

If the controller does not acknowledge a read byte, the device will stop sending data back on SDA and waits until it detects a restart or a stop followed by a start or the device is reset by RESETB or a V_{CCI} POR.

6.9.3 I^2C target acknowledge fail

If the target ack fails to reach the controller because the bus is being held high by some bus fault condition, the target does not detect this. The target will wait for the controller to send the next address. The controller should detect the bus fault and issue a reset.

6.9.4 I^2C target data send to controller fail

The target does not monitor the data sent back to the controller. If some other device on the bus corrupts the data, the target will not detect this.

6.9.5 I^2C stop detect

If the target detects a stop at any time, it will stop whatever it is doing and wait for a start command.

6.9.6 I^2C start detect

If the target detects a start at any time, it will stop whatever it is doing and treat the start as a new start command.

6.9.7 SPI illegal command

A valid command is an 8 bit word. The first three bits are the command itself, followed by the w/rb bit then one zero and three "don't care" bits. If the zero after the w/rb bit is not present, this will be detected as an illegal command. The device will ignore the command and wait until it detects CSBx high then low or a RESETB pulled low or a V_{CCI} POR.

6.9.8 SPI loss of synchrony

SPI has the capability to accept data words continually without pulling CSBx high then low. This can be used to stream data rapidly, however, there is a risk that a single event could corrupt the SCLK or SDAT and the device will lose its place in the data stream. Without CSBx pulling high then low, there is no way for the device to know when to resynchronize. It is therefore recommended that the user pull CSBx high then low to resynchronize all data words. If fast burst data is required, omit CSBx transitions for only as long as necessary, then resume CSBx transitions.

6.9.9 Extremely long transactions

All transactions should terminate with CSBx high (for SPI) or with a STOP in I^2C. If a transaction is paused without these terminating events, there is a very small risk of a combination of multiple single events over an extended period causing faulty operation. Note that this vulnerability would have a very small cross section due to the internal modular redundancy in the device. This small cross section failure mode is eliminated as long as each transaction terminates correctly in a timely manner.

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7 PACKAGING INFORMATION

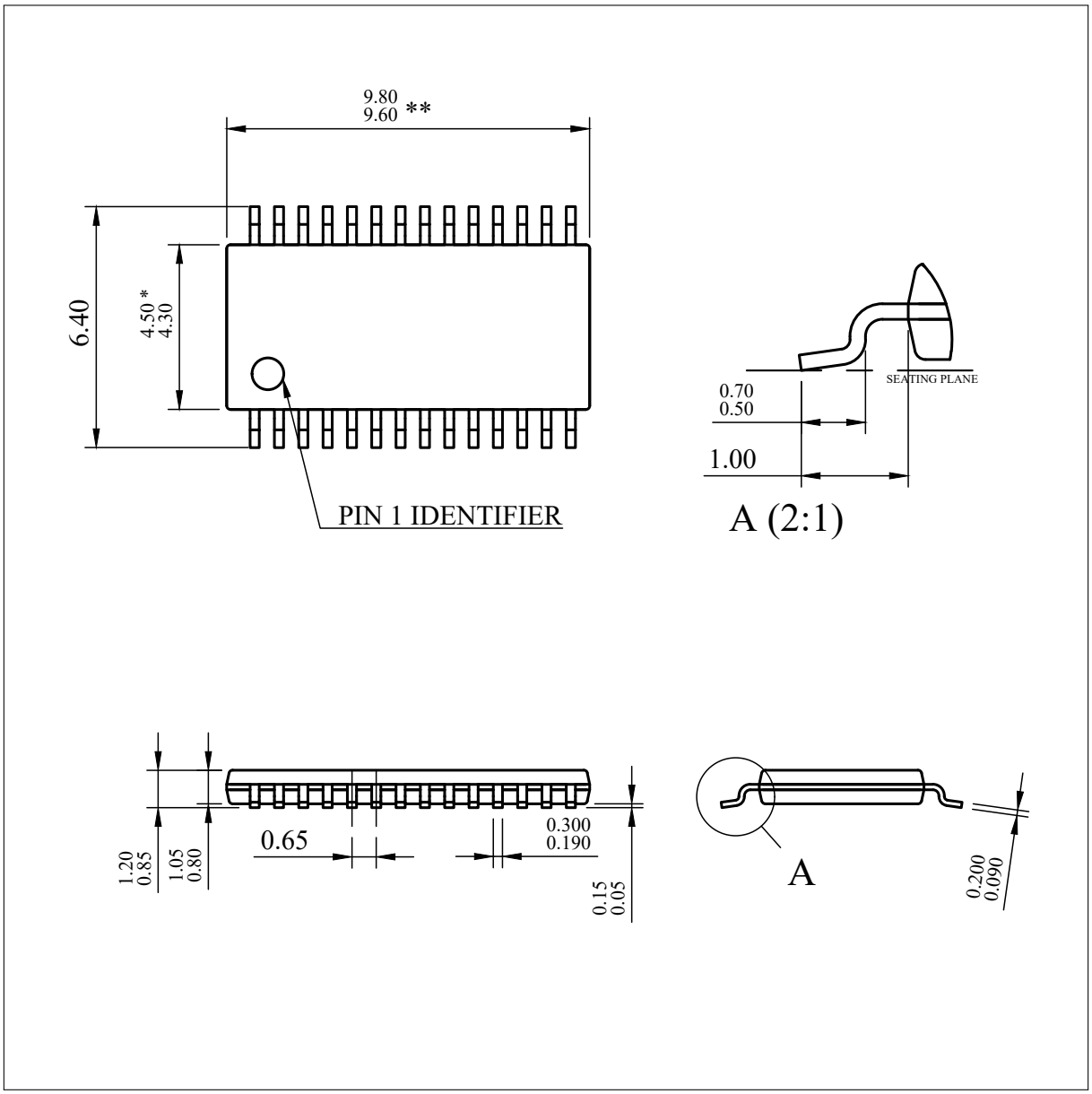

Figure 20: 28-NT - Package Mechanical Detail (NiPdAu)

Notes:

1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

∗ Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25mm each side.

∗∗ Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

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8 ORDERING INFORMATION

Example part numbers for the APIO16/AFIO16 are listed in Table 21. The full list of options for this part can be found in Figure 21. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 21: APIO16/AFIO16 Ordering Information

DEVICE	DESCRIPTION	PACKAGE	LEAD FINISH	PACKAGE DIAGRAM	PACKAGE MASS
APIO16ANT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16ANT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16BNT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16BNT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16CNT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16CNT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (30 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16ENT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (for evaluation only)	TSSOP-28	NiPdAu	28-NT	95 mg
APIO16ENT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (for evaluation only)	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16ANT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (300 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16ANT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (300 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16BNT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (300 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16BNT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (300 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16CNT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (300 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16CNT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (300 krad (Si))	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16ENT-R	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (for evaluation only)	TSSOP-28	NiPdAu	28-NT	95 mg
AFIO16ENT-J[1]	Radiation Hardened level translating I^2C, SMBUS, SPI 16-bit I/O expander (for evaluation only)	TSSOP-28	NiPdAu	28-NT	95 mg

[1] Available through distributors only.

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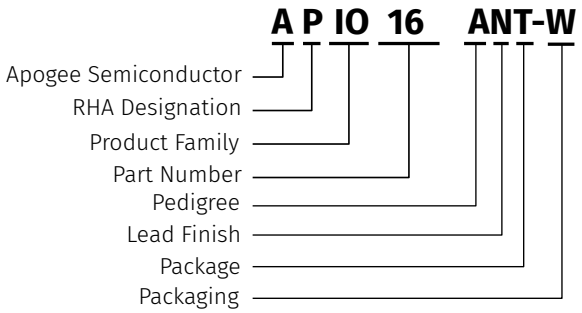

Figure 21: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Product Family
   - **I/O expander**
3. Part Number
   - **16 number of bits**
4. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
5. Lead Finish
   - **N** Nickel Palladium Gold (NiPdAu)
6. Package
   - **T** Thin Shrink Small Outline Package (TSSOP)
7. Packaging
   - **W** Waffle Pack or Pillow Stat Box
   - **R** Tape and Reel[1]
   - **J** JEDEC Tray

[1] Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

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9 REVISION HISTORY

REVISION	DESCRIPTION	DATE
C00	Initial Public Production Release	October 2, 2025
C01	Reduced Temperature range for 1.4V operation	November 4, 2025

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