LM98555 CCD Driver

Check for Samples: LM98555

FEATURES

- **All CCD Drivers Integrated into One Package**
- **High Strength Drivers Designed Specifically for CCD Loads**
- **Ability to Scale Clock Driver Strength**
- **Skew Specifications Ensured**
- **Separate Input and Output Power Supplies**
- **CMOS Process Technology**
- **64-Pin HTSSOP Package with Extended Power Handling Capability**

KEY SPECIFICATIONS

- **Supply Voltage**
  - **Inputs 3.0 to 5.5V**
  - **Drivers 4.5 to 5.8V**
- **Maximum Output Skew Between P1A and P2A Outputs 0.5 ns**
- **Maximum Power Handling 2.0W**

DESCRIPTION

The LM98555 is a highly integrated driver circuit intended for CCD driving applications. It combines 25 drivers of varying drive strengths into one chip to provide a complete CCD driving solution. Due to this one-chip integration, optimal skew control is achieved for this demanding application.

Functional Description

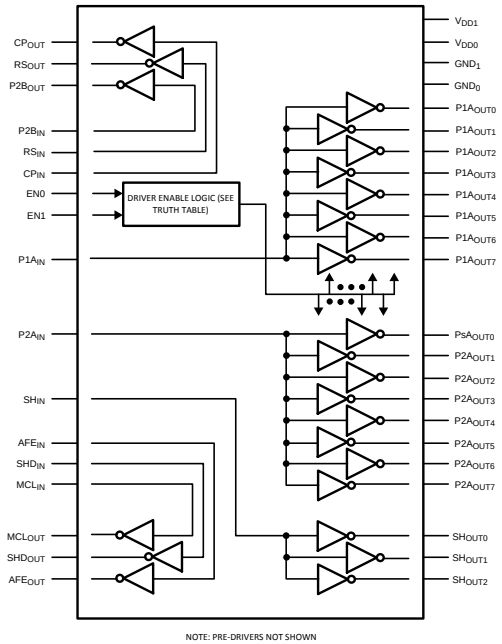


Figure 1. Functional Block Diagram

Connection Diagram

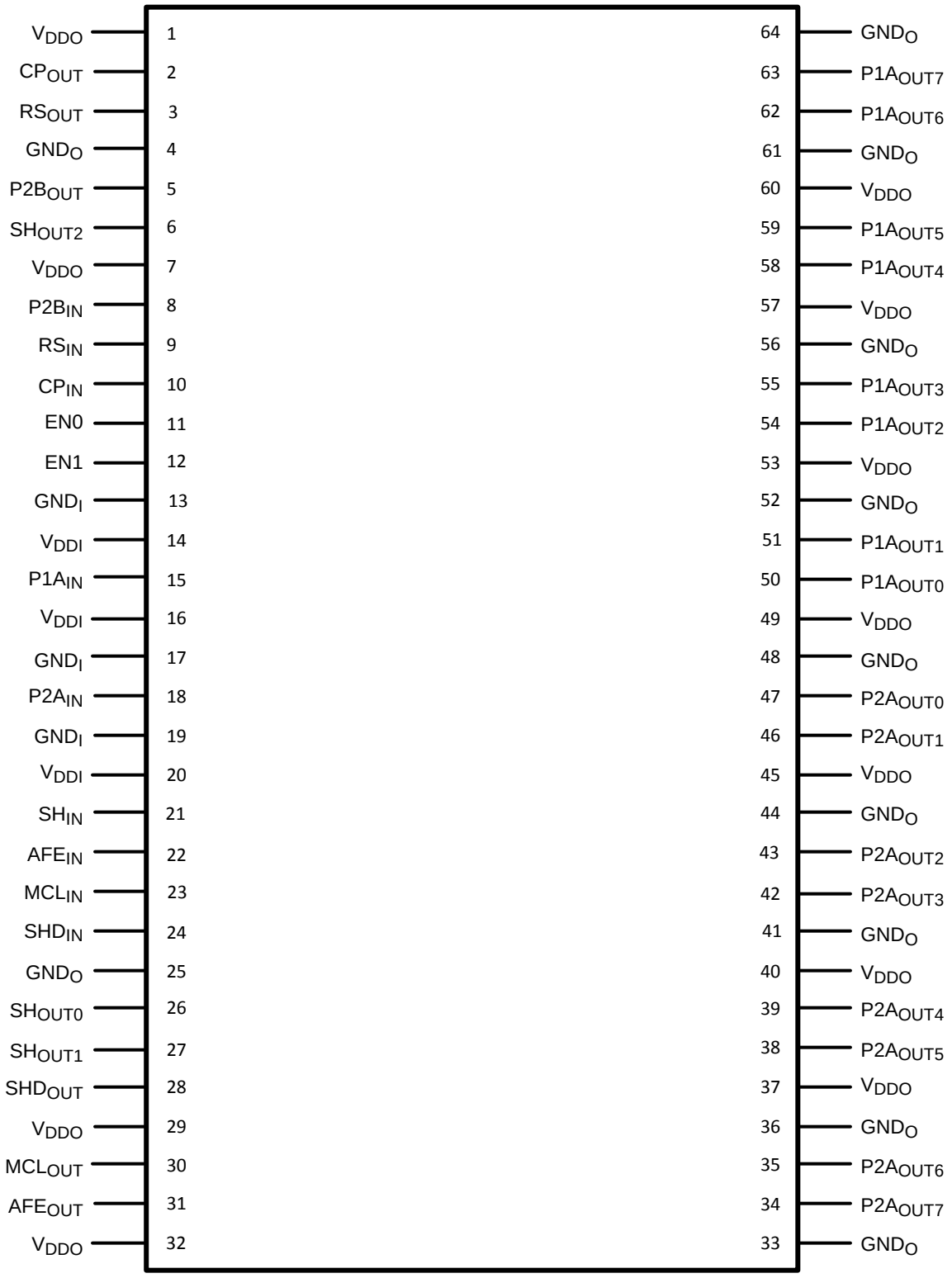


Figure 2. HTSSOP Package
See Package Number DCA0064A

Pin Descriptions

Pin Name	Pin No.	Type	Description
Driver inputs			
$P2B_{IN}$	8	Input	CMOS logic input for the P2B driver.
RS_{IN}	9	Input	CMOS logic input for the RS driver.
CP_{IN}	10	Input	CMOS logic input for the CP driver.
$P1A_{IN}$	15	Input	CMOS logic input for the P1A ganged (8) driver set.
$P2A_{IN}$	18	Input	CMOS logic input for the P2A ganged (8) driver set.
SH_{IN}	21	Input	CMOS logic input for the SH ganged (3) driver set.
AFE_{IN}	22	Input	CMOS logic input for the AFE driver.
MCL_{IN}	23	Input	CMOS logic input for the MCL driver.
SHD_{IN}	24	Input	CMOS logic input for the SHD driver.
Driver Outputs			
SHD_{OUT}	28	Output; Low-Strength	Driver output for the SHD_{IN} input signal.
MCL_{OUT}	30	Output; Low-Strength	Driver output for the MCL_{IN} input signal.
AFE_{OUT}	31	Output; Low-Strength	Driver output for the AFE_{IN} input signal.
CP_{OUT}	2	Output; Low-Strength	Driver output for the CP_{IN} input signal. Typically used to drive the Clamp Gate input of the CCD.
RS_{OUT}	3	Output; Low-Strength	Driver output for the RS_{IN} input signal. Typically used to drive the Reset Gate input of the CCD.
$P2B_{OUT}$	5	Output; Low-Strength	Driver output for the $P2B_{IN}$ input signal.
$P2A_{OUT0}$	47	Output; TRI-STATE; High-Strength	Ganged driver outputs for the $P2A_{IN}$ input. Typically the user may join together these outputs to drive the φ2 clock input of the CCD. Some of these outputs may be disabled using the EN(1:0) inputs - see Application Information.
$P2A_{OUT1}$	46		
$P2A_{OUT2}$	43		
$P2A_{OUT3}$	42		
$P2A_{OUT4}$	39		
$P2A_{OUT5}$	38		
$P2A_{OUT6}$	35		
$P2A_{OUT7}$	34		
$P1A_{OUT0}$	50	Output; TRI-STATE; High-Strength	Ganged driver outputs for the $P1A_{IN}$ input. Typically the user may join together these outputs to drive the φ1 clock input of the CCD. Some of these outputs may be disabled using the EN(1:0) inputs - see Application Information.
$P1A_{OUT1}$	51		
$P1A_{OUT2}$	54		
$P1A_{OUT3}$	55		
$P1A_{OUT4}$	58		
$P1A_{OUT5}$	59		
$P1A_{OUT6}$	62		
$P1A_{OUT7}$	63		
SH_{OUT0}	26	Output; Low-Strength	Ganged driver outputs for the SH_{IN} input signal. Typically used to drive the Shift Gate input of the CCD.
SH_{OUT1}	27		
SH_{OUT2}	6		
Logic Inputs			
EN0	11	Input	Driver enable control. Some of the P1A and P2A drivers can be disabled using these inputs. See Application Information.
EN1	12		
Power & Ground Pins			
V_{DDI}	14 16 20	Power	V_{DD} for pre-drivers.

Pin Descriptions (continued)

Pin Name	Pin No.	Type	Description
V_{DDO}	1 7 29 32 37 40 45 49 53 57 60	Power	V_{DD} for final-stage driver.
GND_I	13 17 19	Ground	Ground connection for all circuitry other than the Final-Stage Drivers.
GND_O	4 25 33 36 41 44 48 52 56 61 64	Ground	Ground connection for the Final-Stage Drivers.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		−0.5V to 6.2V
Package Power Rating at 25°C(3)		2.0 Watts
Voltage on Any Input or Output Pin		−0.5V to V_{DD}+0.5V
DC Input Current at Any Pin		25 mA
DC Package Input Current		50 mA
Storage Temperature		−65°C to +150°C
Lead temperature (Soldering, 10 sec.)		300°C
ESD Susceptibility	Human Body Model	2000V
	Machine Model	200V

(1) Absolute maximum ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Package power rating assumes the exposed thermal pad is soldered to the printed circuit board as recommended, with significant heat spreading provided by vias to internal or bottom heat dissipation planes or pad. If this is not the case, then the package power rating should be reduced. See THERMAL GUIDELINES in Application Information for more information.

Operating Conditions

Supply Voltage	V_{DDI}	+3.0V to +5.5V
Supply Voltage	V_{DDO}	+4.5V to +5.8V
Supply Sequencing(1)		V_{DDI} < V_{DDO}+0.2V
Ambient Temperature (T_A)		0 to 70°C
Operating Frequency		30 MHz
Power Dissipation(2)		2.0W

(1) When powering up and down, transient voltage levels on V_{DDI} must be lower than (V_{DDO} + 0.2V)
(2) This is the power dissipated on-chip due to all currents flowing through the device - both DC and AC. This operating condition will be violated if all driver outputs are fully loaded and operating at the same time at the rated F_{MAX}. The system design must constrain the chip's operating conditions (loads, power supply, number of parallel drivers enabled, frequency of operation) to make certain that this limit is never exceeded.

Package Thermal Resistances

Package	θ_{J-A} (1)	θ_{J-PAD} (Thermal Pad)
64-Lead HTSSOP	36.8°C / W	6.2°C / W

(1) Package thermal resistance for junction to ambient is based on a 5.5 inch by 3 inch, 4 layer printed circuit board, with thermal vias connecting the heat sinking pad to a full internal ground plane. Tests were done in still air, with a power dissipation of 2.0 W, at an ambient temperature of 22°C.

DC Electrical Characteristics

The following specifications apply for GND = 0V, V_{DDI} = 3.3V, V_{DDO} = 5.0V, unless noted otherwise. **Boldface limits apply for T_A= T_{MIN} to T_{MAX};** all other limits T_A= 25°C

Parameter		Test Conditions	Min	Typical	Max	Units
I_I	Logic 1 Input Current	V_I = V_{DDI}	**-1**	0.004	**1**	µA
	Logic 0 Input Current	V_I = GND_I	**-1**	0.006	**1**	µA
V_{IT}	Input Threshold	V_{DDI} = 3.3V	**1.41**	1.57	**1.75**	V
	Input Threshold	V_{DDI} = 5.0V		2.48		V
	Input Threshold Hysteresis	V_{DDI} = 3.3V	**-72**	11	**100**	mV
ΔV_{IT}	Input Threshold Variation	Between P1A, P2A inputs	-100		100	mV

DC Electrical Characteristics (continued)

The following specifications apply for GND = 0V, V_{DDI} = 3.3V, V_{DDO} = 5.0V, unless noted otherwise. **Boldface limits apply for T_A= T_{MIN} to T_{MAX};** all other limits T_A= 25°C

Parameter		Test Conditions	Min	Typical	Max	Units
R_O	Output Impedance P1A and P2A Outputs	I_{LOAD} = 525 mA $R_O = (V_{DDO} - V_O)/I_{OH}$ or $R_O = V_O/I_{OL}$		6.1	**9.9**	Ω
R_O	Output Impedance All Other Outputs	I_{LOAD} = 280 mA $R_O = (V_{DDO} - V_O)/I_{OH}$ or $R_O = V_O/I_{OL}$		10.2	**17.4**	Ω

AC Electrical Characteristics

The following specifications apply for GND = 0V, V_{DDI} = 3.3V, V_{DDO} = 5.0V, unless noted otherwise. **Boldface limits apply for T_A= T_{MIN} to T_{MAX};** all other limits T_A= 25°C

Parameter		Test Conditions	Min	Typical	Max	Units
t_{PHL}	Prop Delay: High-to-Low P1A and P2A Outputs	C_L = 220 pF, R_L = 10Ω (1)	**3.06**	4.6	**6.55**	ns
t_{PHL}	Prop Delay: High-to-Low CP, RS, P2B Outputs	C_L = 82 pF, R_L = 10Ω (1) (2)		4.1		ns
t_{PLH}	Prop Delay: Low-to-High P1A and P2A Outputs	C_L = 220 pF, R_L = 10Ω (3)	**3.38**	4.9	**6.68**	ns
t_{PLH}	Prop Delay: Low-to-High CP, RS, P2B Outputs	C_L = 82 pF, R_L = 10Ω (3) (2)		4.2		ns
t_{SKEW}	Prop Delay Skew High-to-Low	Between any P1A or P2A Outputs on a Single Unit C_L = 220 pF, R_L = 10Ω		109	**387**	ps
	Prop Delay Skew Low-to-High			157	**490**	

(1) Propagation Delay High-to-Low with output low trigger voltage at V_{DDO}*0.75.
(2) Typical values determined from characterization testing only. Not production tested or ensured.
(3) Propagation Delay Low-to-High with output high trigger voltage at V_{DDO}*0.25.

Test Conditions

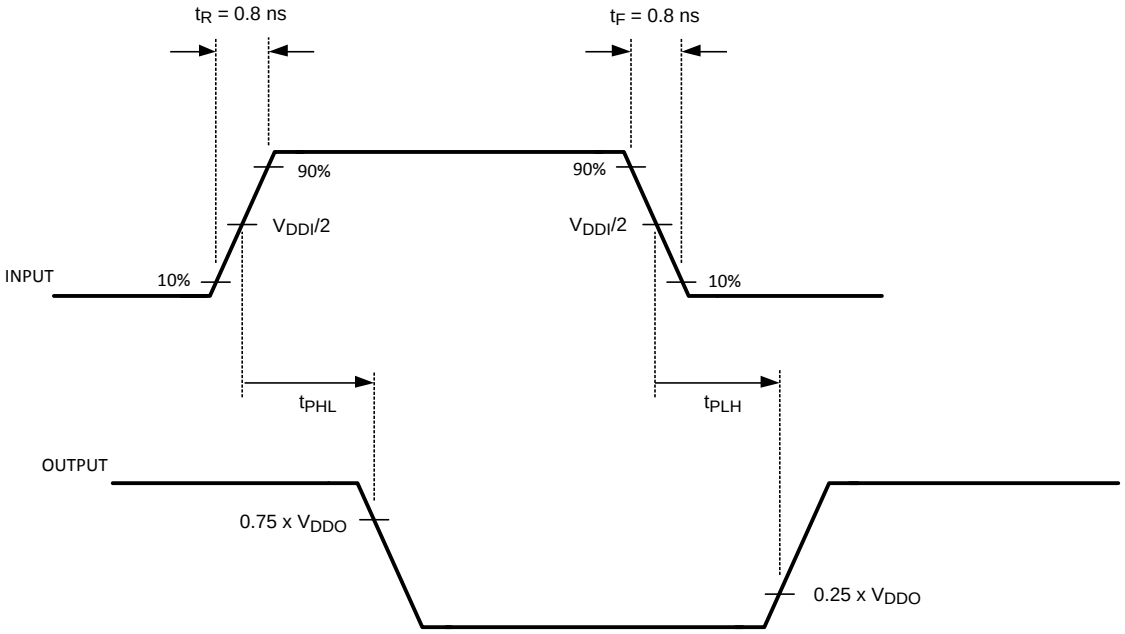


Figure 3. AC Test Conditions

APPLICATION INFORMATION

The LM98555 is a fully integrated clock driver/buffer for high speed CCD applications. It provides high performance low impedance drivers, with optimized low skew performance of the P1 and P2 outputs. Enable inputs allow use of two, four, six, or all eight P1 and P2 drivers to optimize the amount of drive for the application. The 64 pin thermally enhanced HTSSOP provides excellent power handling through the use of an exposed heat transfer pad on the underside of the package.

THERMAL GUIDELINES

The LM98555's maximum power dissipation limit, shown in Operating Conditions, must be strictly adhered to. The product's multiple high-strength drivers, with their ability to drive a wide-range of loads, make it possible to be within spec on each output and yet violate the aggregate maximum power dissipation limit for the total product. Special caution must be paid to this by limiting the chip's operating conditions (loads, power supply, number of parallel drivers enabled, frequency of operation) to make certain that the maximum power dissipation limit is never exceeded.

Thermal characterization of the device has been done to provide reference points under specific conditions. θ junction to ambient was measured using a 5.5 inch by 3 inch, 4 layer PCB. The thermal contact pad on the board was connected using vias to a full ground plane on one of the internal layers. The recommended thermal pad is shown in Figure 4.

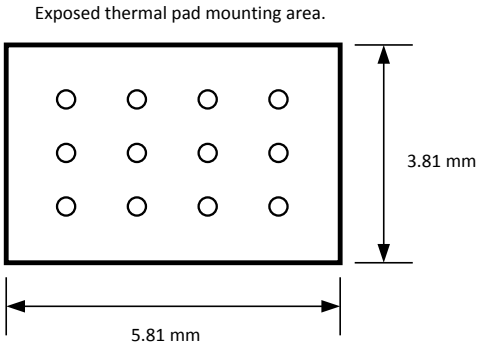


Figure 4. Exposed Pad Land Pattern

The vias shown provide a path for heat to flow from the pad to a heat sinking or dissipating area of the printed circuit board. The following figures show several typical examples of how this can be done, and illustrate how heat is conducted away from the IC to larger areas where it is dissipated.

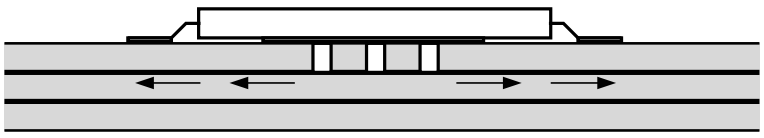


Figure 5. 4 Layer PCB - Example 1

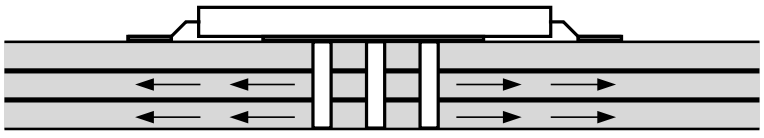
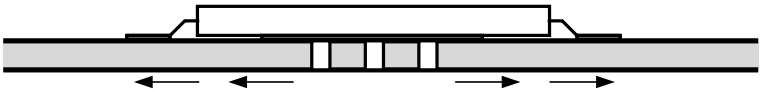


Figure 6. 4 Layer PCB - Example 2



Vias couple thermal energy to copper plane on bottom layer to transfer heat away from package.

Figure 7. 2 Layer PCB

In multi-layer board applications, one or more internal planes are usually dedicated as a ground plane. Connecting the thermal pad to this ground plane with vias will usually provide adequate heat management. In 2 layer boards, it is important to provide a large heat spreading pad on the opposite side of the board. The vias will provide a good thermal connection between the pad under the IC, and the heat spreading pad on the bottom of the board. Thermal modelling can be done using the θ junction to pad information provided, to calculate the required area of copper based on the ambient temperature of the system, and the calculated amount of thermal dissipation in the LM98555.

POWER DISSIPATION

The amount of power dissipated in the device can be determined by considering the following factors:

- Power dissipated delivering energy to the load capacitance
- Power dissipated delivering energy to parasitic capacitance
- Power dissipated due to leakage in the IC

The amount of power dissipated due to leakage is very small in this CMOS device. Most of the power will be due to the load capacitance being switched, with a small additional amount caused by the parasitic capacitance of the output circuitry, output pins, and PCB traces. A typical parasitic capacitance would be on the order of 5 pF. Since the load capacitance will be on the order of 100 pF or more, this usually dominates the power dissipation calculation. The following equation can be used to calculate the power dissipation due to capacitive switching of the loads:

P = Sum[Output Frequency x Load Capacitance x Output Voltage Squared] (summed for all outputs)

INPUT SIGNALS

Care should be taken to match the trace lengths between timing signals that require low skew. Usually, the P1A and P2A signals will be the most critical. In some applications, the timing of P2B with respect to P1A and P2A can also be important, and that input trace should also be carefully designed.

Trace shape and width should also be carefully controlled. The trace geometry will determine the characteristic impedance of each trace. The impedance should be set to give reasonable immunity to noise coupling into the trace. With a known trace impedance, the signals can be terminated using a series resistor at the source that is equal to the characteristic impedance. This will provide a signal with minimum overshoot and ringing, and will contribute to better performance of the final signal reaching the CCD.

OUTPUT CONNECTIONS AND LOADING EXAMPLES

The LM98555 can be used with a wide variety of different CCD sensors. The P1Aoutx and P2Aoutx outputs can be selectively enabled to provide 2, 4, 6, or 8 drivers. This allows the available drive strength to be optimized for the sensor and application. Connecting multiple outputs together in parallel as shown in the typical application circuit provides lower drive impedance as needed to suit the load being driven. When driving smaller loads, lower switching noise will be generated if the minimum necessary outputs are enabled and used.

The output signal traces should also be designed for a known impedance. Source terminating resistors should be used in series with each output to provide good matching to the trace characteristic impedance. The resistors should be located as close as possible to each output pin. If multiple outputs will be combined to drive a single load pin, the output signals should be combined after the termination resistors. This will provide the best summing of adjacent outputs. The combined signal should then pass through an EMI type ferrite bead. This component can be selected to change the bandwidth or shape of the clocking signal to achieve the best CCD transfer efficiency.

Several other techniques will also help maintain signal quality, and minimize timing differences between critical signals. Vias should not be used for critical timing signals. These can add impedance discontinuities that will affect the waveform quality. Traces should have gradual bends and avoid sharp changes in direction that can also introduce impedance discontinuities.

SELECTIVE DRIVER ENABLING

With the Enable pins, the user has the capability to enable only the drivers that are required for the application, thus eliminating unnecessary outputs switching. The following table shows the details.

EN1	EN0	Driver-set State
0	0	P1Aout(1:0) and P2Aout(1:0) are enabled; all others disabled.
0	1	P1Aout(3:0) and P2Aout(3:0) are enabled; all others disabled.
1	0	P1Aout(5:0) and P2Aout(5:0) are enabled; all others disabled.
1	1	All P1Aout and P2Aout drivers are enabled.
Note: The disabled drivers' outputs are in TRI-STATE.		

POWER SUPPLY SEQUENCING

During device power-up and power-down, V_{DDI} must be maintained less than (V_{DDO} + 0.2V) to prevent excessive current flow through the internal ESD protection circuitry. Since most applications will involve 3V on V_{DDI} and 5V on V_{DDO}, this can be easily met. If this voltage relationship cannot be met, then the DC pin and package limits for input current must be maintained by controlling the source impedance of the V_{DDI} supply.

POWER AND GROUND - PLANES VERSUS BUSES

The best performance will be achieved by using planes rather than traces for power and ground. Planes provide lower electrical and thermal impedance. Ground bounce and ringing are reduced, electromagnetic emissions are minimized and the best thermal performance will be realized.

A single common ground plane should be used for all power and signal domains.

Another circuit board layer can be used to provide power to the various circuitry. Different power buses can be provided by isolated planes within this layer of the circuit board.

EMI MANAGEMENT

Good EMI control will be achieved by addressing the following items:

- Provide proper source termination of output signals
- Limit length of output traces
- Ensure adequate power supply decoupling
- Provide power and ground planes as much as possible
- Provide common ground plane for all signals, especially between LM98555 outputs and load CCD
- Enable and use the minimum number of outputs needed

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM98555CCMH/NOPB	ACTIVE	HTSSOP	DCA	64	28	RoHS & Green	NIPDAU | SN	Level-4-260C-72 HR	0 to 70	LM98555 CCMH	Samples
LM98555CCMHX/NOPB	ACTIVE	HTSSOP	DCA	64	1000	RoHS & Green	NIPDAU | SN	Level-4-260C-72 HR	0 to 70	LM98555 CCMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

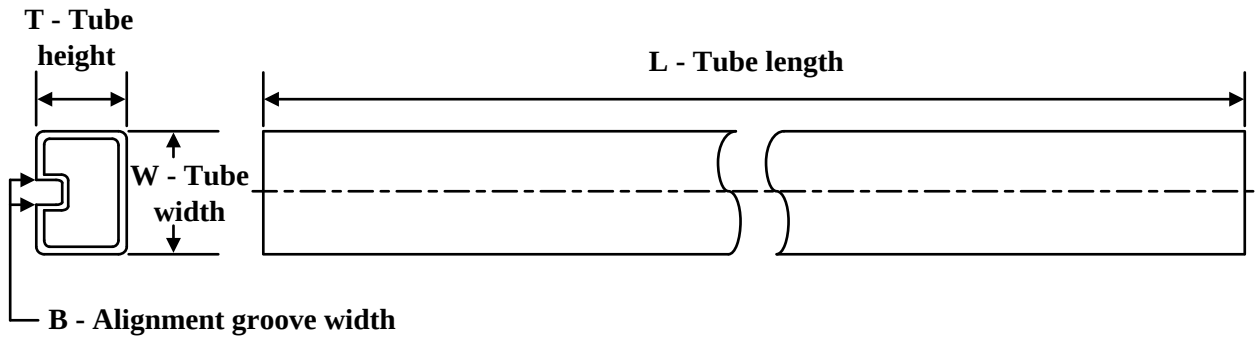
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM98555CCMH/NOPB	DCA	HTSSOP	64	28	495	10	2540	5.79

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