The documentation and process conversion measures necessary to comply with this document shall be completed by 22 October 2016.

INCH-POUND

MIL-PRF-19500/253M
22 July 2016
SUPERSEDING
MIL-PRF-19500/253L
7 April 2011

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, LOW-POWER,
TYPES 2N930 JAN, JANTX, JANTXV, JANS, JANHC, JANKC

MIL-PRF-19500/253 is inactive for new design after 3 June 2004.
For new design use MIL-PRF-19500/376.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1 SCOPE

1.1 Scope. This specification covers the performance requirements for an NPN, silicon, low-power transistors. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500, and two levels of product assurance are provided for each unencapsulated device. Radiation hardness assurance (RHA) level designators “M”, “D”, “P“, “L” “R”, “F’, “G”, and “H” are appended to the device prefix to identify devices which have passed RHA requirements.

* 1.2 Physical dimensions. The device packages for the encapsulated device types are as follows: (2N930) (TO-18) in accordance with figure 1, (UB, surface mount) in accordance with figure 2. The dimensions and topography for JANHC and JANKC unencapsulated die is as follows: The A version die in accordance with figure 3. The B version die in accordance with figure 4. The C version die in accordance with figure 5.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_J and T_{STG}
V dc	V dc	V dc	mA dc	°C
60	45	6	30	-65 to +200

Types	P_T (1) T_A = +25°C	P_T (1) T_C = +25°C	P_T (1) T_{SP} = +25°C	$R_{\theta JA}$ (2)	$R_{\theta JC}$ (2)	$R_{\theta JSP(IS)}$ (2)
	mW	mW	mW	°C/W	°C/W	°C/W
2N930	360	360	N/A	485	150	N/A
2N930UB	N/A	N/A	360	325 (3)	N/A	95

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C. Continued.

(1) For derating, see figures 6, 7, 8, and 9.
(2) For thermal impedance curves see figures 10, 11, and 12.
(3) Mounted on FR-4 base material PCB (1 ounce copper) with contacts 20 mils larger than package pads.

1.4 Primary electrical characteristics.

Limits	h_{FE1} (1)	h_{FE2} (1)	C_{obo}	$\|h_{fe}\|$	$V_{BE(SAT)}$ (1)	$V_{CE(SAT)}$ (1)
	V_{CE} = 5 V dc I_C = 10 µA dc	V_{CE} = 5 V dc I_C = 500 µA dc	V_{CB} = 5 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	V_{CE} = 5 V dc I_C = 500 µA dc f = 30 MHz	I_C = 10 mA dc I_B = 0.5 mA dc	I_C = 10 mA dc I_B = 0.5 mA dc
			pF		V dc	V dc
Min	100	150		1.5	0.6	
Max	300		8.0	6.0	1.0	1.0

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level.

* 1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

* 1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "M", "D", "P", "L", "R", "F", "G", and "H").

* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follow: "930".

* 1.5.4 Suffix symbols. The following suffix letters are incorporated in the PIN in the order listed in the table as applicable:

	A blank first suffix symbol indicates a through-hole mount package similar to a TO-18 metal can (see figure 1) TO-18
UB	Indicates a 4 pad surface mount package. The metal lid is connected to pad 4 (see figure 2)

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

* 1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A", “B”, and ”C”.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

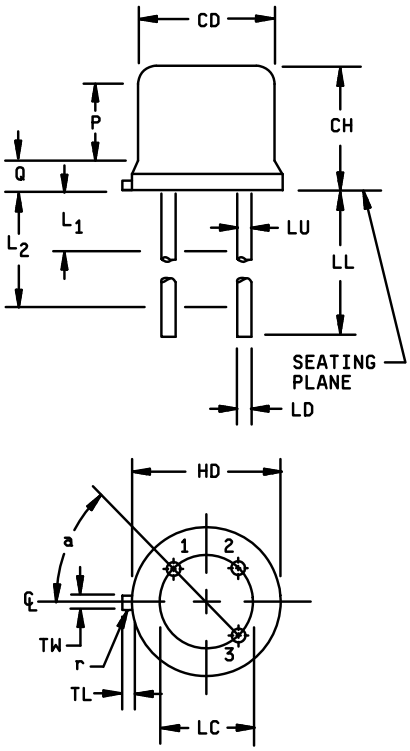
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil.

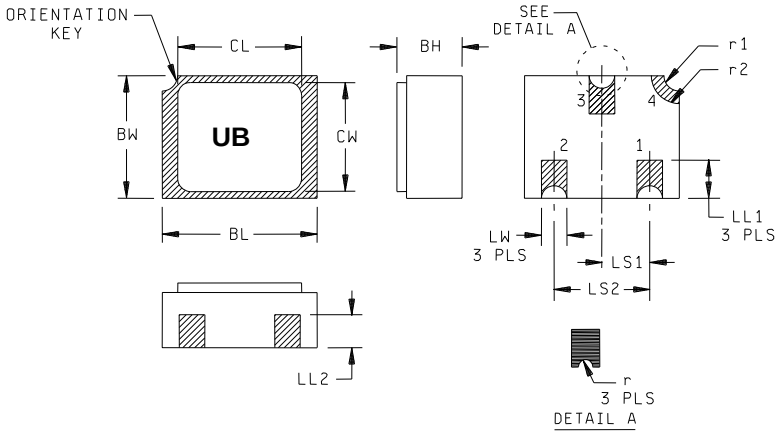
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

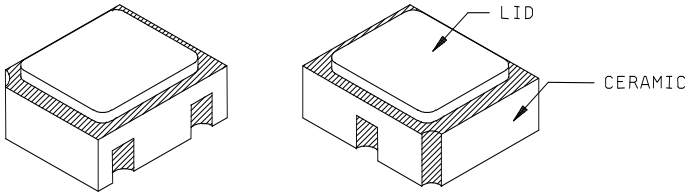
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6



NOTES:
1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with AMSE Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions (similar to TO-18).



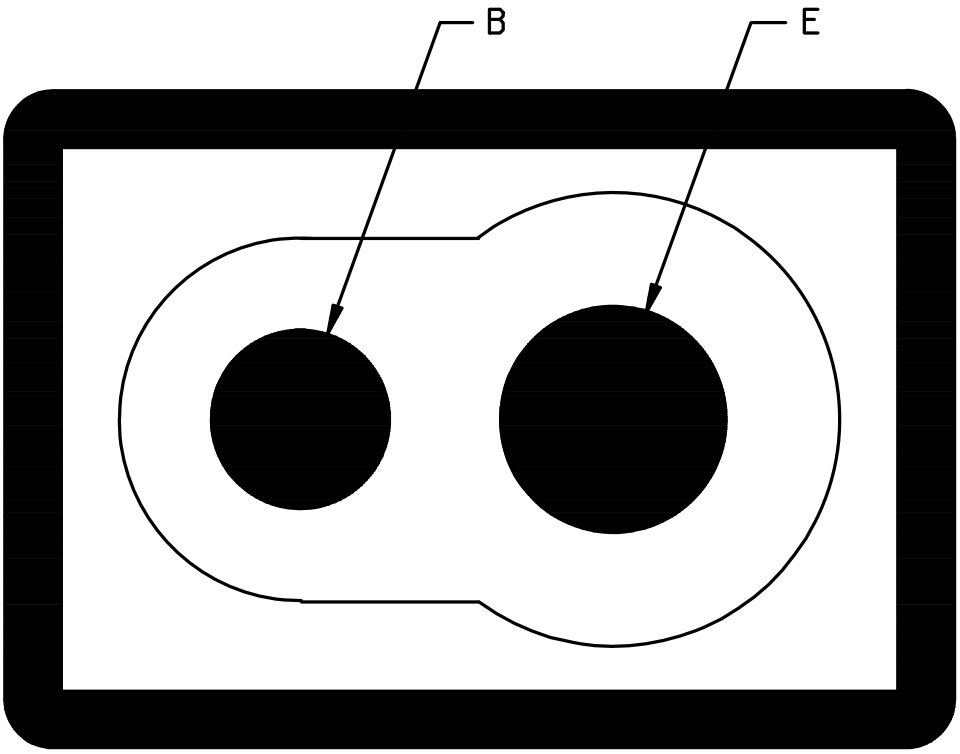


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.9	
LL2	.017	.035	0.43	0.89	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.

3. Hatched areas on package denote metallized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, surface mount (2N930UB).

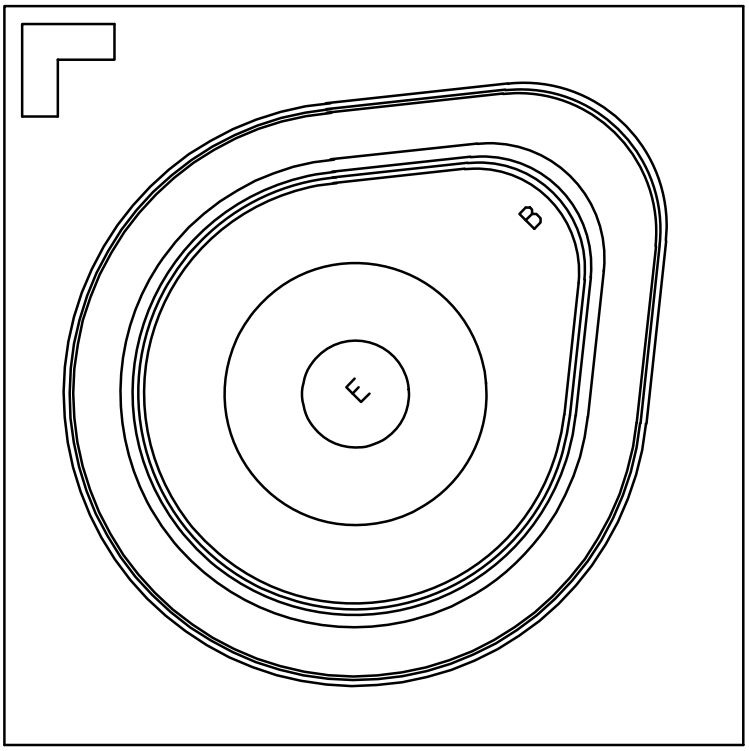


A- version

NOTES:

1.	Chip size	.015 x .019 inch ±.001 inch. (0.381 X 0.483 ±0.0254 mm)
2.	Chip thickness	.010 ±.0015 inch. (0.254 ±0.038 mm).
3.	Top metal	Aluminum 15,000Å minimum, 18,000Å nominal.
4.	Back metal	A. Gold 3,500 Å minimum, 5,000 Å nominal.
5.	Backside	Collector.
6.	Bonding pad	B = .003 inch (0.076 mm), E = .004 inch (0.101 mm) diameter.
7.	Passivation	Si_3N_4 (Silicon Nitride) 5,600 Å min, 8,000 Å nom.

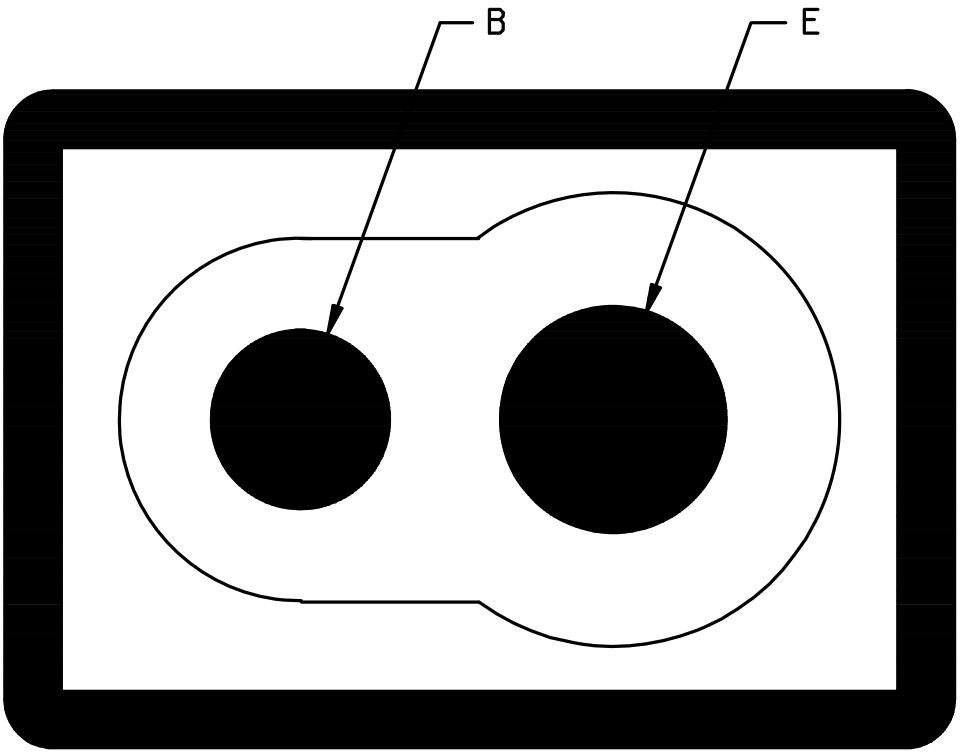
FIGURE 3. Physical dimensions, JANHCA die.



B-version

Die size:	.018 x .018 inch (0.4572 x 0.4572 mm).
Die thickness:	.008 ±.0016 inch (0.2032 ±0.04064 mm).
Base pad:	.0025 inch (0.0635 mm) diameter.
Emitter pad:	.003 inch (0.0762 mm) diameter.
Back metal:	Gold, 6,500 ±1,950 Å.
Top metal:	Aluminum, 19,500 ±2,500 Å.
Back side:	Collector.
Glassivation:	SiO_2, 7,500 ±1,500 Å.

FIGURE 4. Physical dimensions, JANHCB and JANKCB die.



C- version

NOTES:

1.	Chip size	.015 x .019 inch ±.001 inch. (0.381 X 0.483 ±0.0254 mm)
2.	Chip thickness	.010 ±.0015 inch. (0.254 ±0.038 mm).
3.	Top metal	Aluminum 10,000Å minimum, 12,000Å nominal.
4.	Back metal	A. Gold 3,500Å minimum, 5,000Å nominal.
5.	Backside	Collector.
6.	Bonding pad	B = .003 inch (0.076 mm), E = .004 inch (0.101 mm) diameter.
7.	Passivation	SiO_2 (Silicon Oxide) 6,300 Å min, 9,000 Å nom.

FIGURE 5. Physical dimensions, JANKCC die.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP(IS)}$	Thermal resistance junction to solder pads (infinite sink mount to PCB).
UB	Surface mount case outlines (see figure 2).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-18), figure 2 (UB, surface mount), and figure 3, figure 4, and figure 5 (die).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. Electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I, table II, table III, and table IV).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement	Measurement
	JANS levels	JANTX and JANTXV levels
3c	Thermal impedance, method 3131 of MIL-STD-750, see 4.3.3.	Thermal impedance, method 3131 of MIL-STD-750, see 4.3.3.
9	I_{CBO2}, h_{FE2}.	Not applicable.
10	48 hours minimum.	48 hours minimum.
11	I_{CBO2}, h_{FE2} ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE2} = ±25 percent.	I_{CBO2}, h_{FE2}
12	See 4.3.1.	See 4.3.1.
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE2} = ±25 percent.	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE2} = ±25 percent.

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. P_D = 100 percent of P_T maximum, T_A ambient rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. This option is limited to plants who are at least transitional (QML) approved or have an approved technical review board (TRB).

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.3 Thermal impedance (measurements). The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit used in 4.3, screen 3c and the subgroup 2 of table I shall comply with the thermal impedance graph in figure 9, figure 10, and figure 11 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131 of MIL-STD-750.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspections only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with group A, subgroup 2 and table IV herein: delta requirements only apply to subgroups B4, and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with group A, subgroup 2 and table IV herein.

* 4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

	Subgroup	Method	Condition
*	B4	1037	V_{CB} = 10 - 30 V dc.
*	B5	1027	V_{CB} = 10- 30 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIa, adjust T_A to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A to achieve a T_J = +225°C minimum.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI, conformance inspection, shall be analyzed to the extent possible to identify root cause and corrective action.

	Step	Method	Condition
*	1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 - 30 V dc, power shall be applied and ambient temperature adjusted to achieve T_J = +150°C minimum using a minimum of P_D = 100 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
	2	1048	Blocking life: T_A = +150°C, V_{CB} = 80 percent rated voltage. 48 hours minimum. n = 45 devices, c = 0.
	3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANJ, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with group A, subgroup 2 and table IV herein; delta requirements only apply to subgroup C6.

* 4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

	Subgroup	Method	Condition
	C2	2036	Test condition E; (not applicable for UB devices).
	C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
*	C6	1026	1,000 hours at V_{CB} = 10 - 30 V dc; power shall be applied and ambient temperature shall be adjusted to achieve T_J = +150°C minimum and a minimum of P_D = 100 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The ample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3).
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2.e herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurement shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, and t_H. Measurement delay time t_{MD} = 70 μs maximum.

* TABLE I. Group A inspection.

	Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
	Subgroup 1 2/						
	Visual and mechanical examination 3/	2071					
	Solderability 3/ 4/	2026	n = 15 leads, c = 0				
	Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
*	Salt atmosphere (corrosion) 4/	1041	n = 6 devices, c = 0, (For laser marked devices only. Not required for non-corrosive base metals)				
*	Temperature cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
	Hermetic seal 4/ 6/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
	Electrical measurements		Table I, subgroup 2				
	Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = 300°C at t = 2 hrs n = 11 wires, c = 0				
	Decap internal visual (design verification) 4/	2075	n = 4 device, c = 0				
	Subgroup 2						
	Thermal impedance 7/	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
	Collector to base cutoff current	3036	Bias condition D, V_{CB} = 60 V dc	I_{CBO1}		10	µA dc
	Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 6 V dc	I_{EBO1}		10	µA dc
	Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	45		V dc
	Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V dc	I_{CES1}		2.0	nA dc
*	Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 5 V dc	I_{CEO}		2.0	nA dc
	Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO2}		5	nA dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - continued.						
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO2}		10	nA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 µA dc; Pulsed (see 4.5.1)	h_{FE1}	100	300	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 µA dc; Pulsed (see 4.5.1)	h_{FE2}	150		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 mA dc	h_{FE3}		600	
Collector-emitter saturation voltage	3071	I_C = 10 mA dc; I_B = 0.5 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)}$		1.0	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 10 mA dc; I_B = 0.5 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$	0.6	1.0	V dc
Subgroup 3						
High temperature operation		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition C;V_{CE} = 45 V dc; pulsed (see 4.5.1)	I_{CES2}		10	µA dc
Low temperature operation		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 10 µA dc	h_{FE4}	20		
Subgroup 4						
Small-signal short-circuit forward current transfer ratio	3206	V_{CE} = 5 V dc; I_C = 1 mA dc; f = 1 kHz	hfe	150	600	
Magnitude of small-signal short- circuit forward current transfer ratio	3306	V_{CE} = 5 V dc; I_C = 500 µA dc; f = 30 MHz	| hfe |	1.5	6.0	
Open circuit output capacitance	3236	V_{CB} = 5 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		8	pF

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - continued.						
Noise figure	3246	V_{CE} = 5 V dc; I_C = 10 μA dc; R_g = 10 kΩ	NF			
Test 1 Test 2 Test 3		f = 100Hz f = 1 kHz f = 10 kHz			5 3 3	dB dB dB
Small-signal open-circuit output admittance	3216	V_{CB} = 5 V dc; I_E = 1.0 mA dc; f = 1 kHz	h_{ob}	0	1.0	mhos
Small-signal open-circuit reverse voltage transfer ratio	3211	V_{CB} = 5 V dc; I_E = 1.0 mA dc; f = 1 kHz	h_{rb}		6×10^{-4}	
Small-signal short-circuit input impedance	3201	V_{CB} = 5 V dc; I_E = 1.0 mA dc; f = 1 kHz	h_{ib}	25	32	Ω
Subgroups 5 and 6						
Not applicable						

1/ For sampling plan, unless otherwise specified, see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.
7/ This test required for the following end-point measurements only:
Group B, subgroup 3, 4, and 5 (JANS).
Group B, step 1 (TX and TXV).
Group C, subgroup 2 and 6.

* TABLE II. Group D inspection and end-point limits.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0 V				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6.0 V dc	I_{EBO1}		20	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	45		V dc
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V	I_{CES1}		4.0	ηA dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 5 V	I_{CEO}		4.0	ηA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5.0 V dc	I_{EBO2}		10	ηA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO2}		20	ηA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 10 µA dc; pulsed (see 4.5.1)	[h_{FE1}] 5/	[50]	300	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 500 µA dc; pulsed (see 4.5.1)	[h_{FE2}] 5/	[75]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 10 mA dc	h_{FE3}		600	
Collector-emitter saturation voltage	3071	I_C = 10 mA dc; I_B = 0.5 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)}$		1.15	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 10 mA dc; I_B = 0.5 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$	0.6	1.15	V dc

See footnotes at end of table.

* TABLE II. Group D inspection and end-point limits - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2						
Steady-state total dose irradiation	1019	Gamma exposure V_{CES} = 36 V				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6.0 V dc	I_{EBO1}		20	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	45		V dc
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 45 V	I_{CES1}		4.0	ηA dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 5 V	I_{CEO}		4.0	ηA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5.0 V dc	I_{EBO2}		10	ηA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 45 V dc	I_{CBO2}		20	ηA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 10 µA dc; pulsed (see 4.5.1)	$[h_{FE1}]$ 5/	[50]	300	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 500 µA dc; pulsed (see 4.5.1)	$[h_{FE2}]$ 5/	[75]		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 10 mA dc	h_{FE3}		600	
Collector-emitter saturation voltage	3071	I_C = 10 mA dc; I_B = 0.5 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)}$		1.15	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 10 mA dc; I_B = 0.5 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$	0.6	1.15	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to the corresponding AL, UA, UB, and UBC suffix versions unless otherwise noted.
4/ See 6.2.e herein.
5/ See method 1019, of MIL-STD-750, for how to determine $[h_{FE}]$ by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE}. Notice the $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

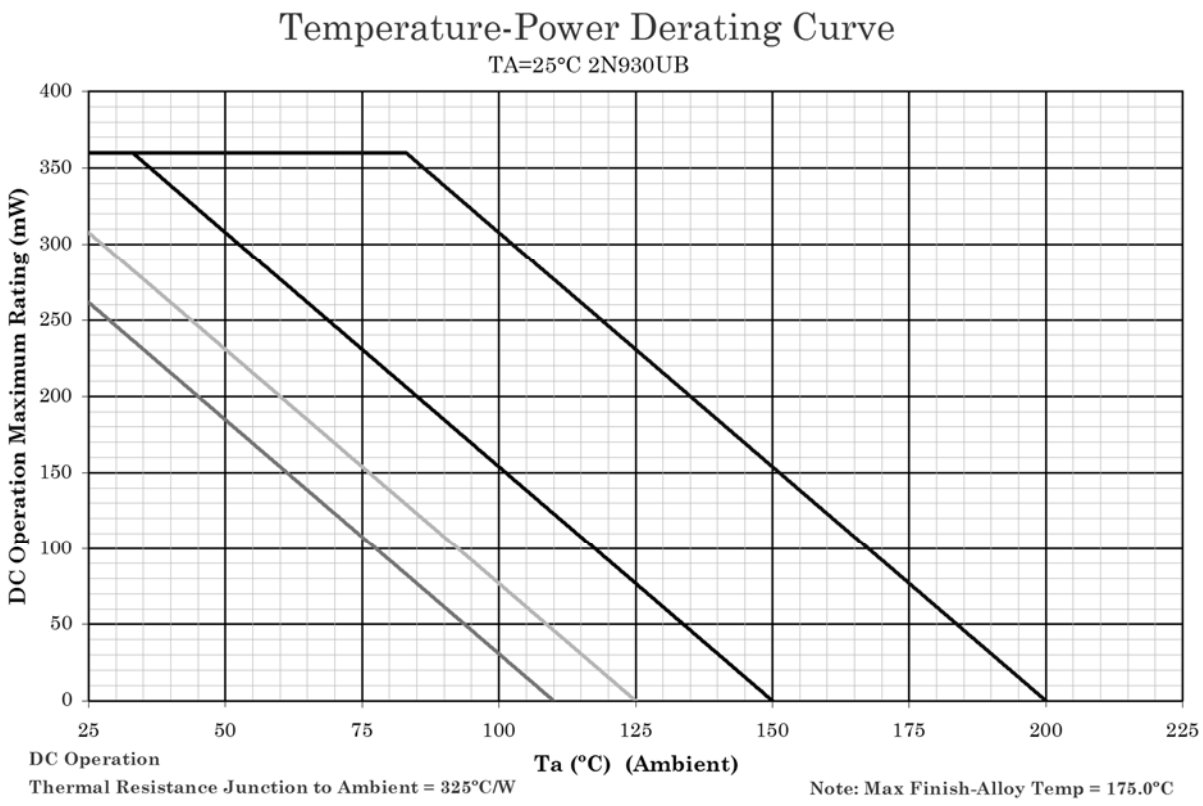
TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and table IV herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and table IV herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500, table E-IX, group E, subgroup 4.	
Subgroup 5			
Not applicable			
Subgroup 6			11 devices c = 0
Electrostatic discharge (ESD)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	

TABLE IV. Groups B, C, and E delta measurements.

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 45 V dc	ΔI_{CB02} 1/	100 percent of initial value or 5 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 500 μA dc; pulsed see 4.5.1.	Δh_{FE2} 1/	±25 percent change from initial reading.	

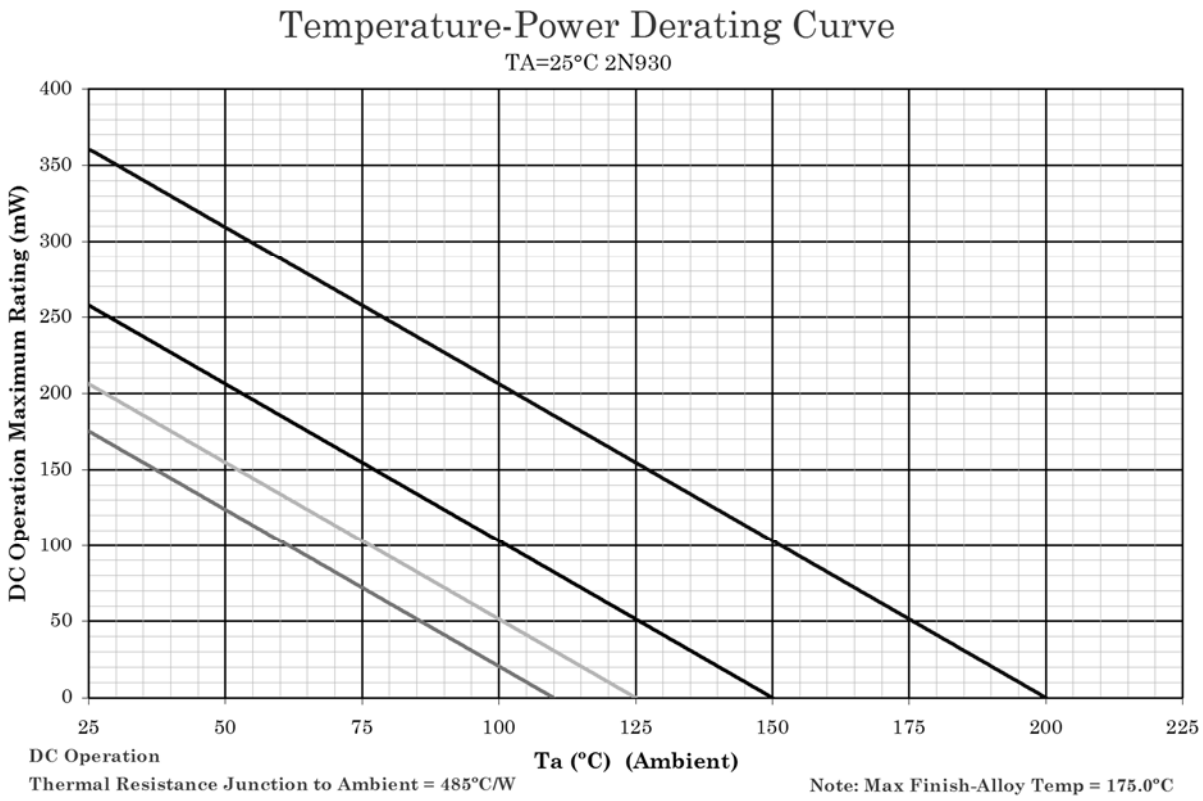
1/ Devices which exceed the table I limits for this test shall not be accepted.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

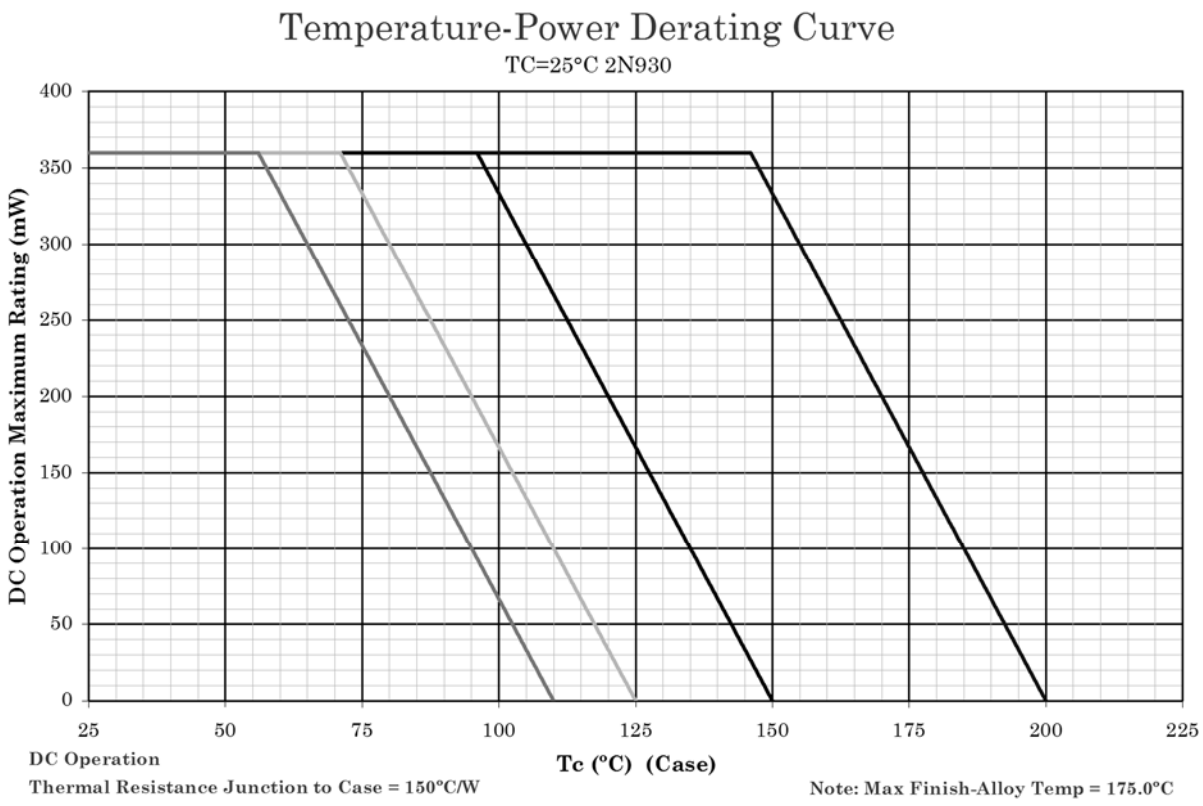
FIGURE 6. Temperature-power derating for 2N930 (UB package).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

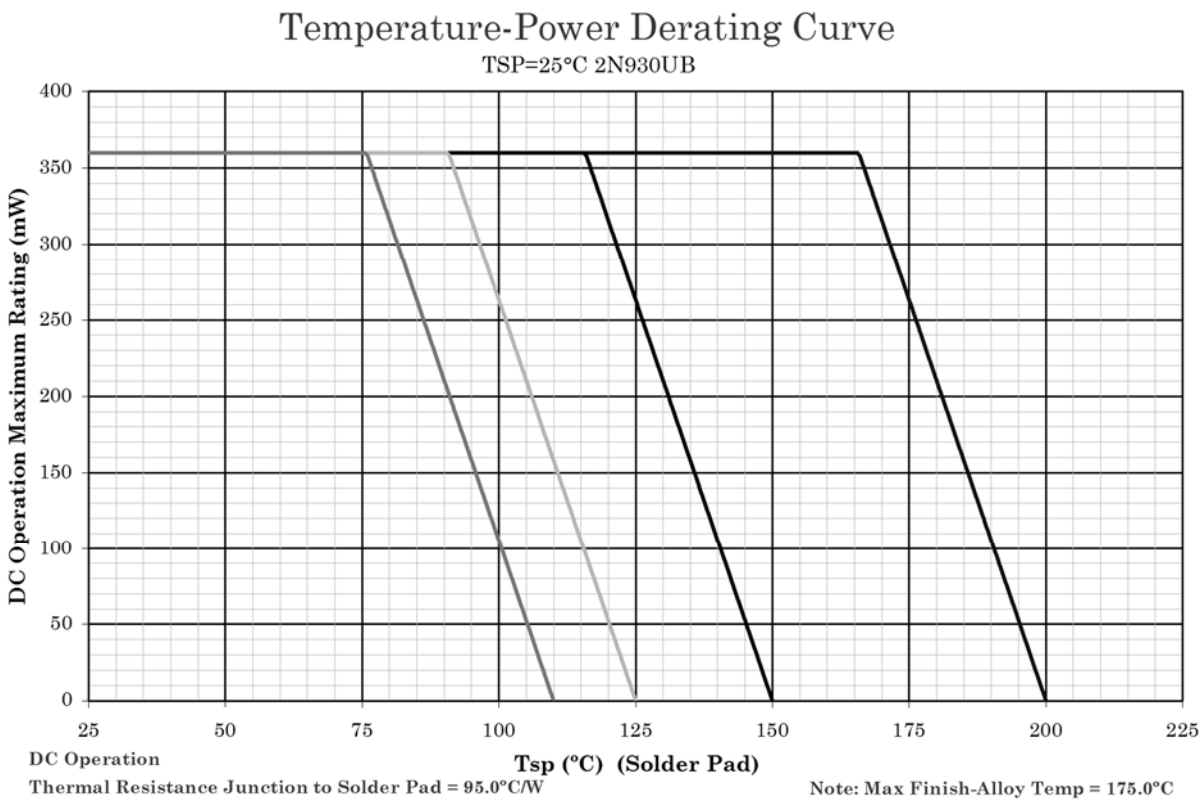
FIGURE 7. Temperature-power derating for 2N930 (TO-18 package).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Temperature-power derating for 2N930 (TO-18 package case base mounted).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 9. Temperature-power derating for 2N930UB (UB).

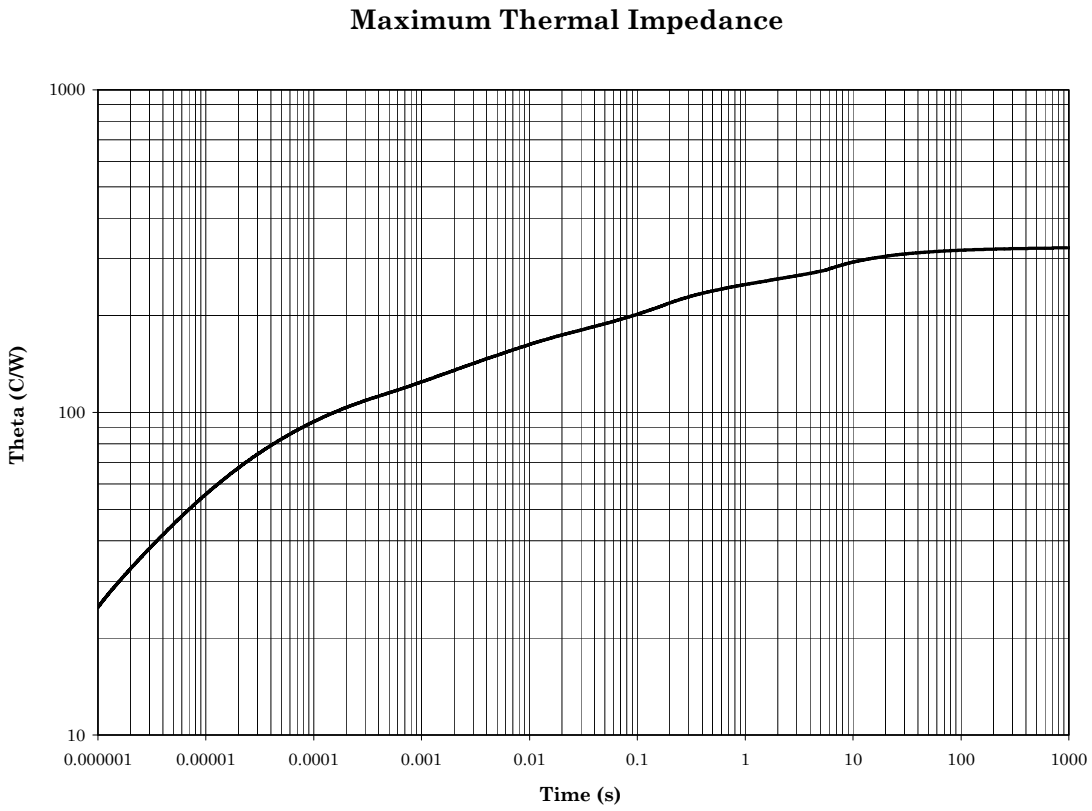


FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N930UB (UB).

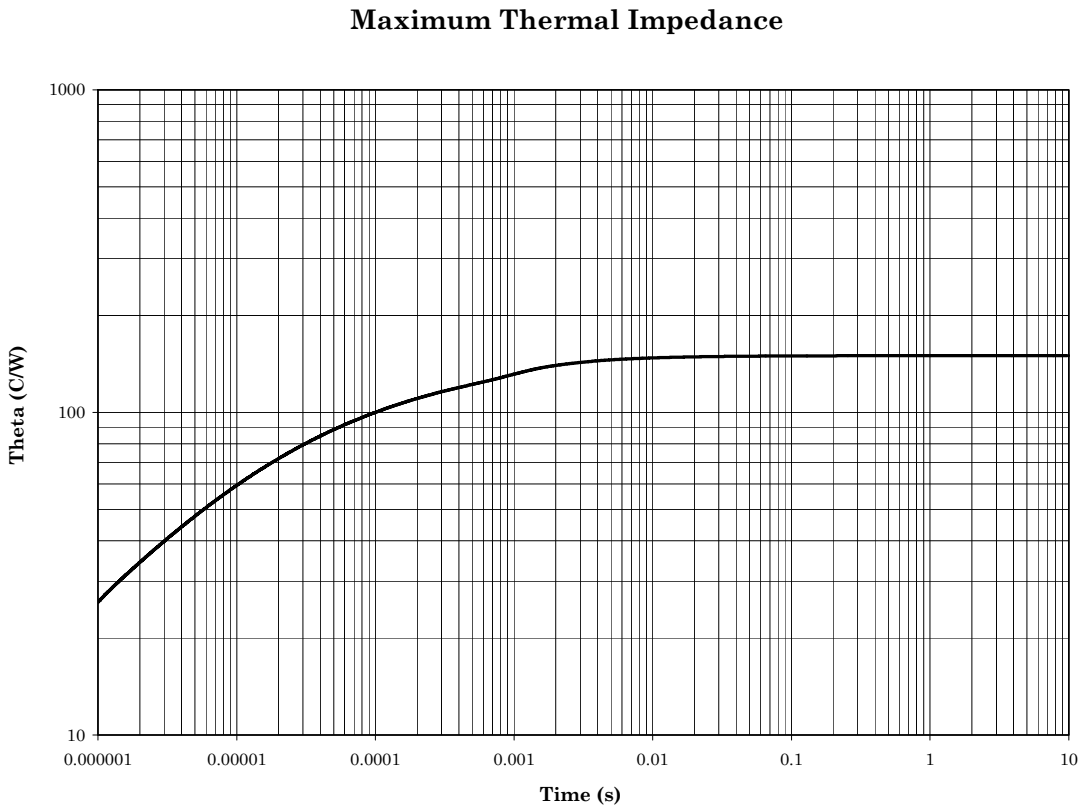


FIGURE 11. Thermal impedance graph ($R_{\theta JC}$) for 2N930 (TO-18 package case base mounted).

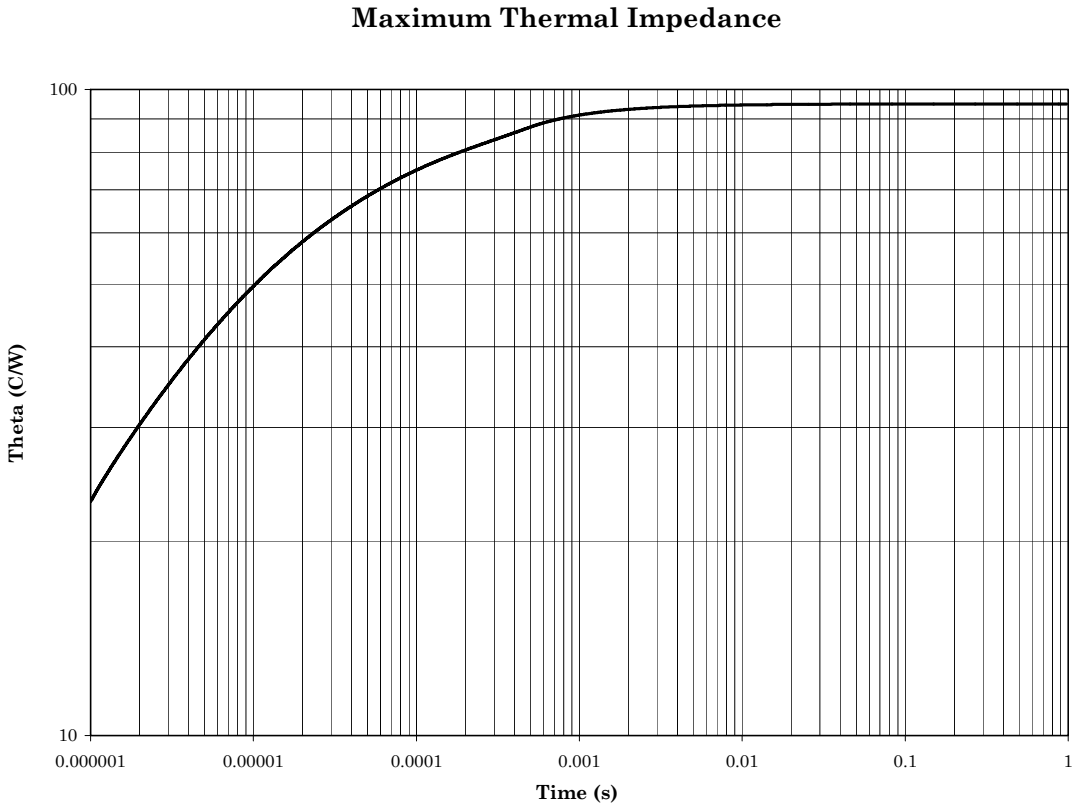


FIGURE 12. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N930UB (UB).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete Part or Identifying Number (PIN), see 1.5.

* e. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

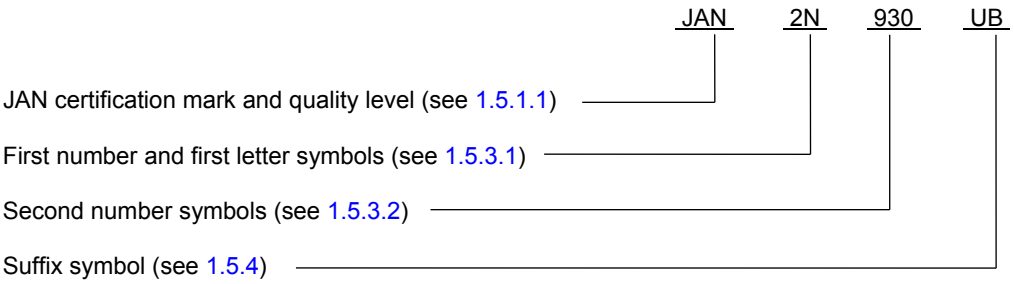
* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

* 6.4 Suppliers of JANHC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N930) will be identified on the QML.

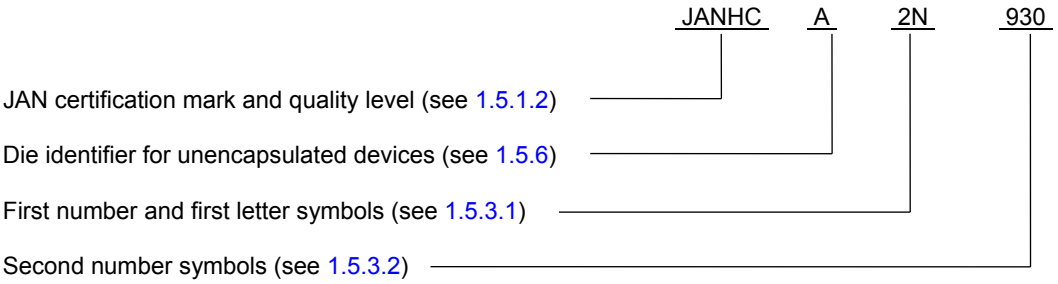
JANC ordering information			
PIN	Manufacturer		
	43611	34156	43611
2N930	JANHCA2N930 JANKCC2N930	JANHCB2N930 JANKCB2N930	JANHCC2N930 JANKCC2N930

* 6.5 PIN construction example.

* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

Encapsulated PINs for type 2N930			
JAN2N930	JANTX2N930	JANTXV2N930	JANS#2N930
JAN2N930UB	JANTX2N930UB	JANTXV2N930UB	JANS#2N930UB

Unencapsulated PINs for type 2N930			
JANHCA#2N930	JANKCA#2N930	JANHCA2N930	JANKCA#2N930
JANHCC2N930	JANKCC#2N930		

* (1) The number sign (#) represent one of eight RHA designators available (M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - AR, AV, MI, SM
Navy - AS
Air Force - 71, 99

Preparing activity:
DLA - CC

(Project 5961-2016-069)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.