

PerFET™ Power Transistor

FEATURES

- Ultra-low On-resistance
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

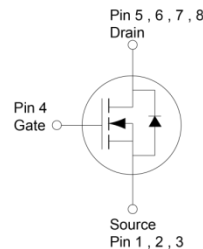
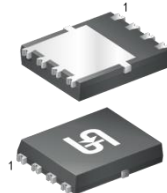
PRODUCT SUMMARY			
PARAMETER		VALUE	UNIT
V_{DS}		40	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	5.6	mΩ
	$V_{GS} = 7V$	6.7	
Q_g	$V_{GS} = 10V$	27.3	nC

APPLICATIONS

- DC-DC Converters
- Solenoid and Motor Drivers
- Load Switch



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$	I_D	90	A
Continuous Drain Current ^(Note 1)	$T_C = 25^\circ\text{C}$	I_D	54	A
	$T_C = 100^\circ\text{C}$		54	
	$T_A = 25^\circ\text{C}$		17	
Pulsed Drain Current		I_{DM}	216	A
Single Pulse Avalanche Current ^(Note 2)		I_{AS}	21.6	A
Single Pulse Avalanche Energy ^(Note 2)		E_{AS}	69.8	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	78.9	W
	$T_C = 125^\circ\text{C}$		26.3	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1.9	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 1mA	BV _{DSS}	40	--	--	V
Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	V _{GS(TH)}	2.4	3	3.6	V
Gate-Source Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 40V	I _{DSS}	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 40V T _J = 125°C		--	--	100	
	Drain-Source On-State Resistance (Note 3)		V _{GS} = 10V, I _D = 27A	R _{DS(on)}	--	
	V _{GS} = 7V, I _D = 27A	--	5		6.7	
Forward Transconductance (Note 3)	V _{DS} = 10V, I _D = 10A	g _{fs}	--	105	--	S
Dynamic						
Total Gate Charge	V _{GS} = 7V, V _{DS} = 20V, I _D = 17A	Q _g	--	19.4	--	nC
Total Gate Charge	V _{GS} = 10V, V _{DS} = 20V, I _D = 17A	Q _g	--	27.3	--	
Gate-Source Charge		Q _{gs}	--	8.4	--	
Gate-Drain Charge		Q _{gd}	--	4.8	--	
Input Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	C _{iss}	--	1942	--	pF
Output Capacitance		C _{oss}	--	350	--	
Reverse Transfer Capacitance		C _{rss}	--	37	--	
Gate Resistance	f = 1.0MHz	R _g	--	1.5	--	Ω
Switching (Note 4)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 20V, I _D = 17A, R _G = 1.5Ω	t _{d(on)}	--	10.1	--	nS
Rise Time		t _r	--	55.7	--	
Turn-Off Delay Time		t _{d(off)}	--	20.3	--	
Fall Time		t _f	--	5.7	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V _{GS} = 0V, I _S = 27A	V _{SD}	--	--	1.1	V
Reverse Recovery Time	I _S = 17A,	t _{rr}	--	32	--	nS
Reverse Recovery Charge	di/dt = 100A/μs	Q _{rr}	--	22	--	nC

Notes:

- Package current limit.
- $L = 0.3mH, V_{GS} = 10V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

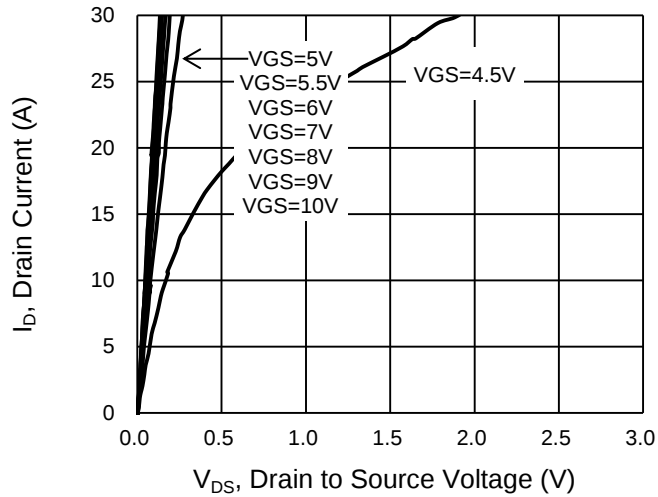
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM056NH04CR RLG	PDFN56U	2,500pcs / 13" Reel

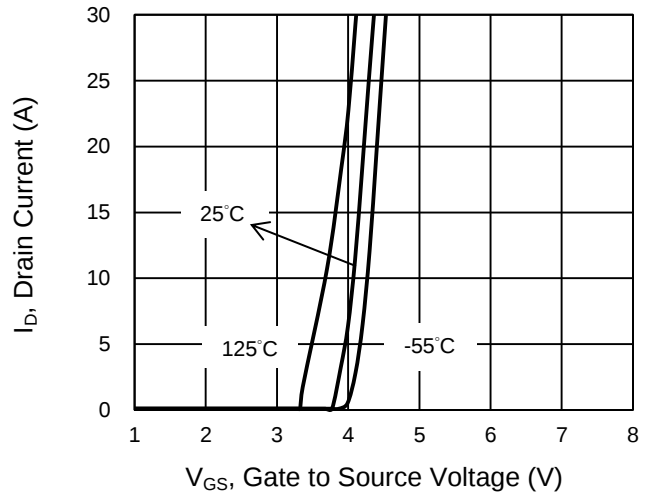
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

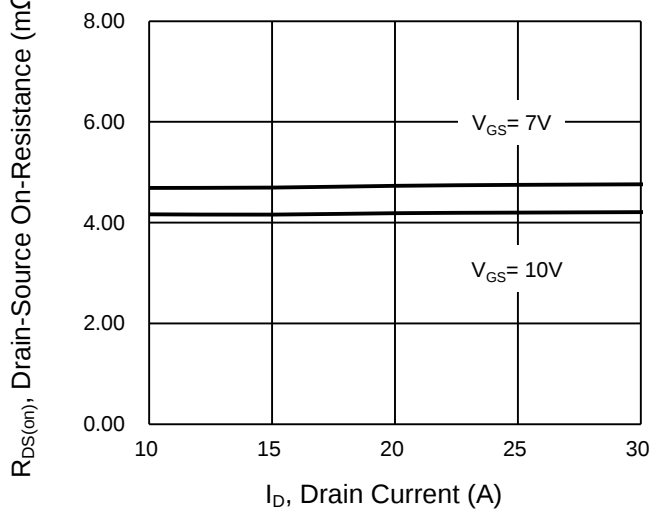
Output Characteristics



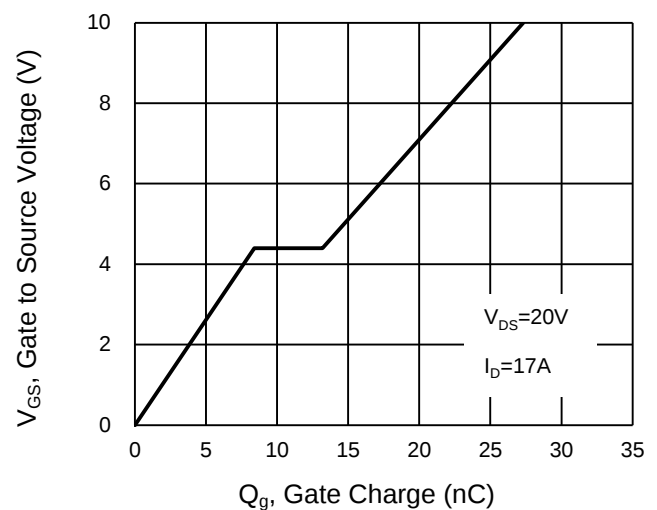
Transfer Characteristics



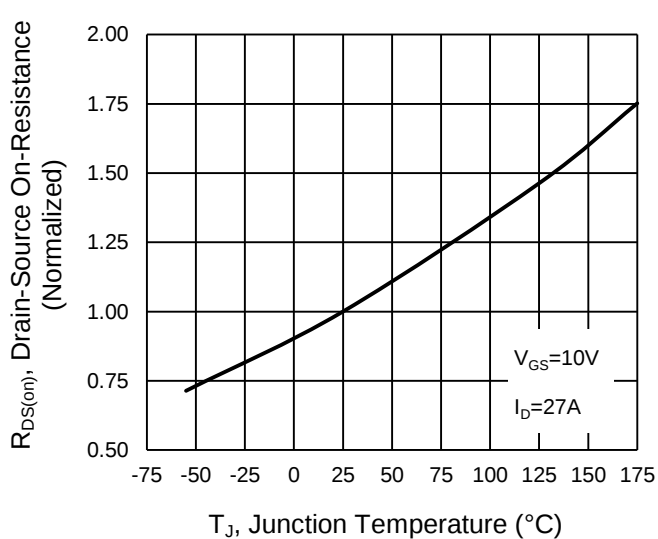
On-Resistance vs. Drain Current



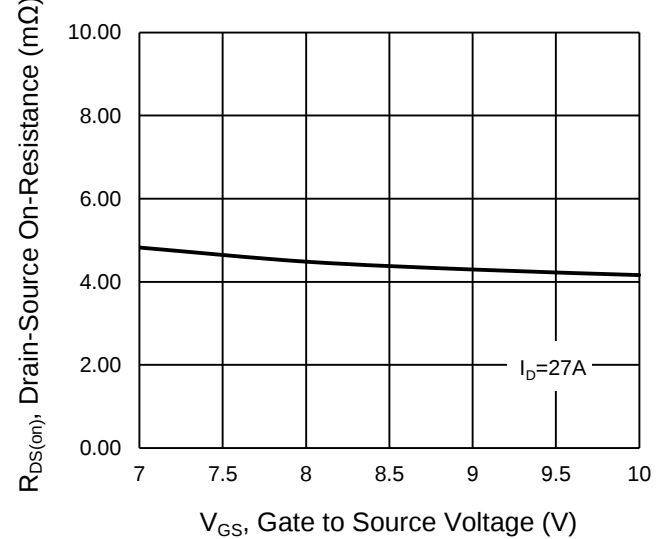
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



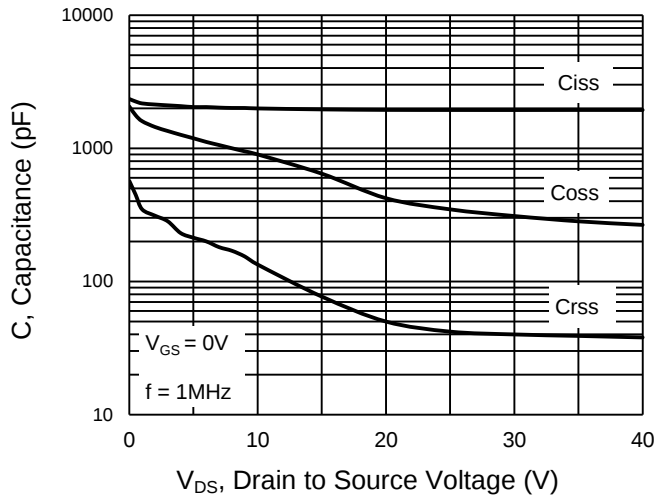
On-Resistance vs. Gate-Source Voltage



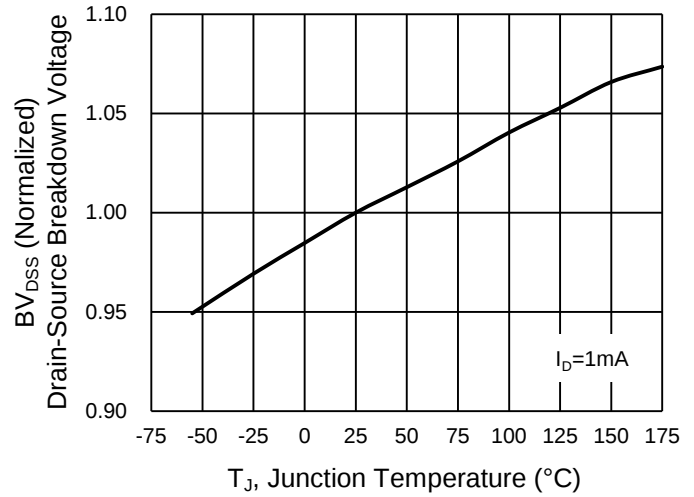
CHARACTERISTICS CURVES

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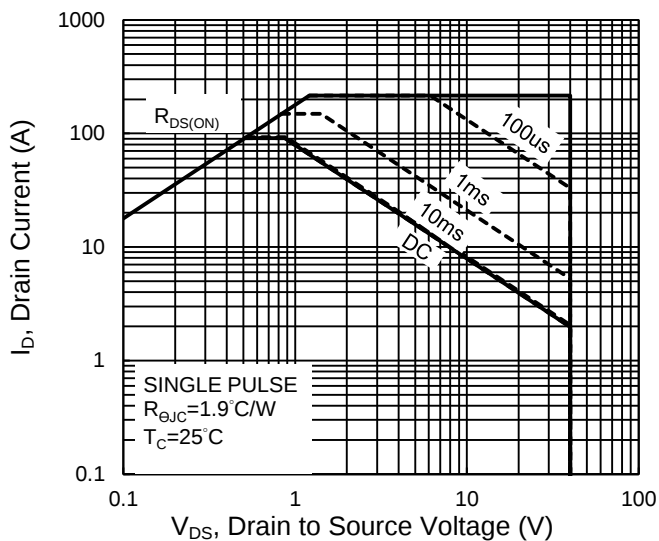
Capacitance vs. Drain-Source Voltage



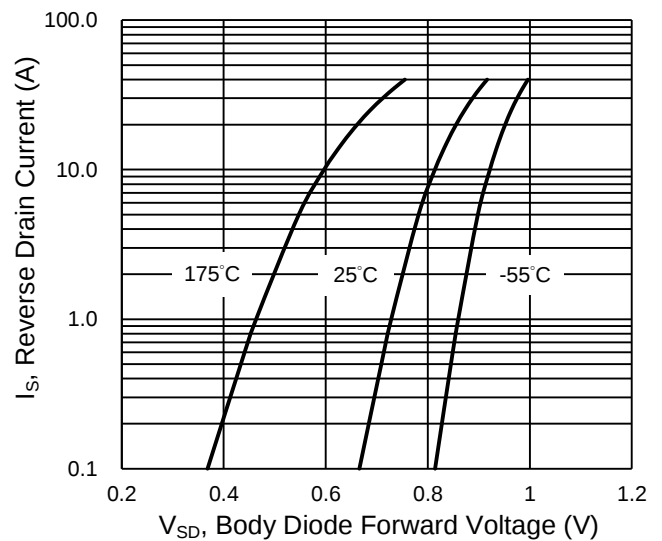
BV_{DSS} vs. Junction Temperature



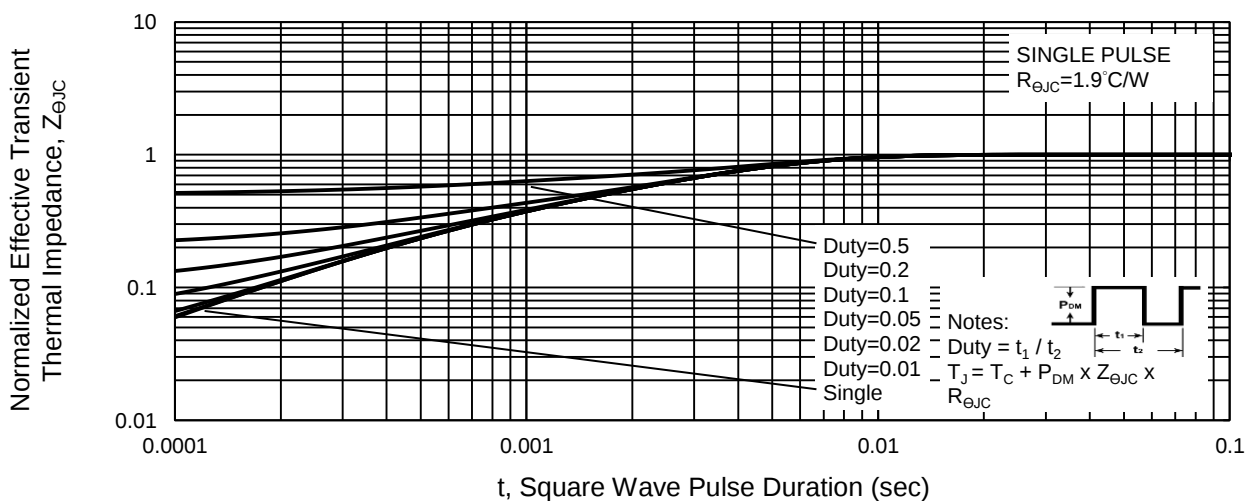
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

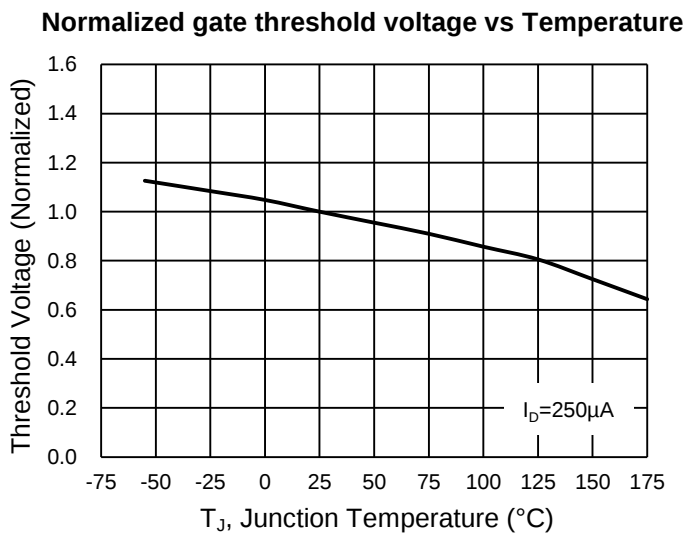
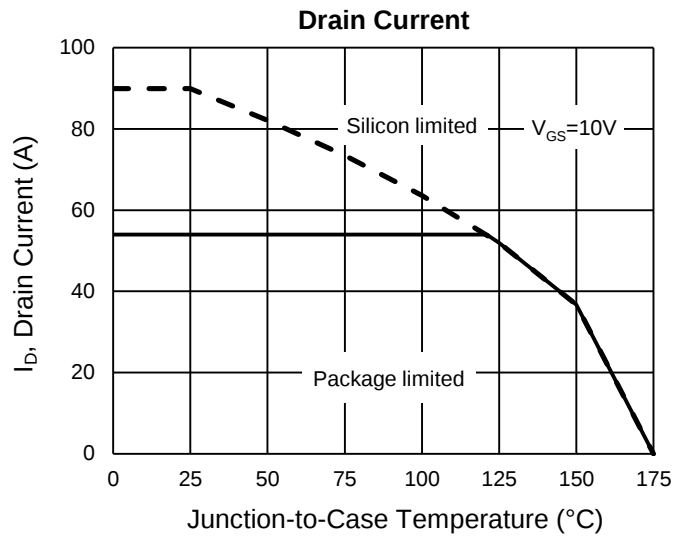
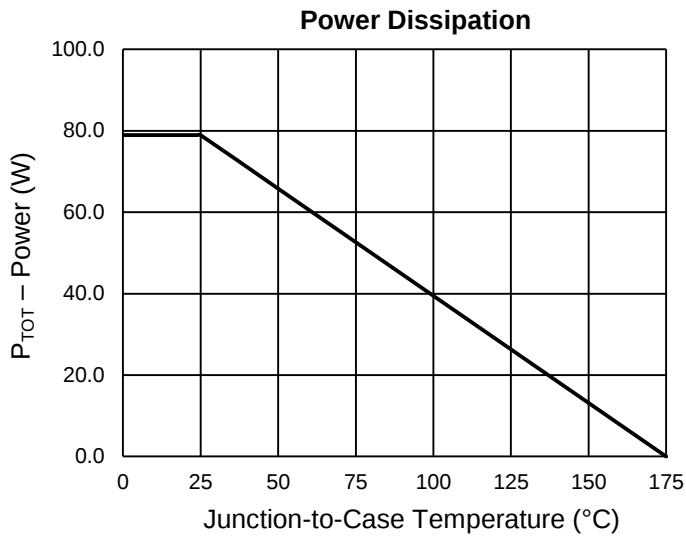


Normalized Thermal Transient Impedance, Junction-to-Case



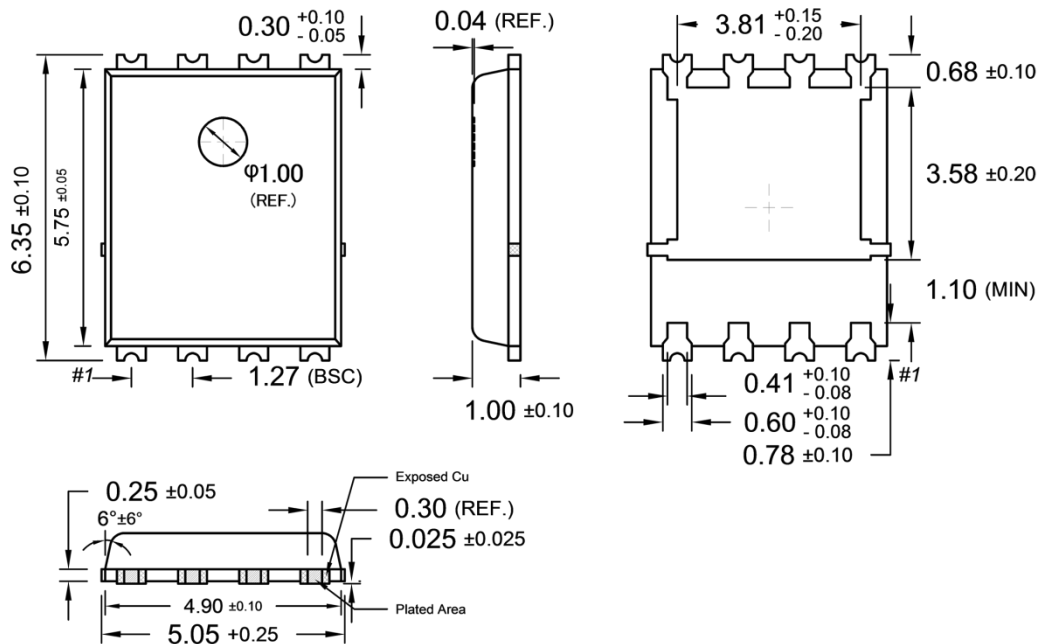
CHARACTERISTICS CURVES

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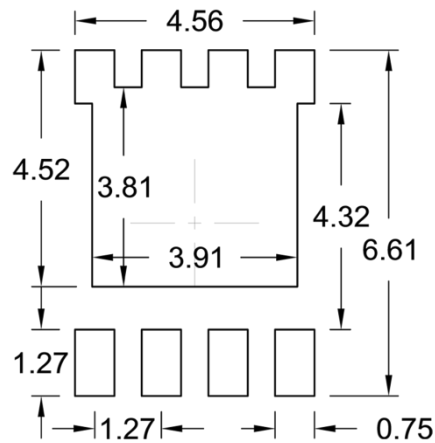


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

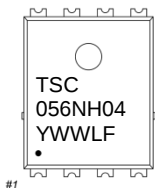
PDFN56U



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9, A~Z)
- F** = Factory Code

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