SMD Wraparound Ultra Low Value Thin Film Resistors

LINKS TO ADDITIONAL RESOURCES

3D Models

With extremely low resistance and high power capabilities, these ultra low value resistors are available with solderable or weldable terminations.

FEATURES

- NiCr + Ta_2O_5 resistive layer
- Pre-soldered or gold terminations
- No inductance for high frequency applications
- Alumina substrates for high power handling capability
- Resistance range: 0.1 Ω to 9.99 Ω
- TCR down to 50 ppm/°C
- Power rating: up to 2 W at +70 °C
- Withstand AEC-Q200 humidity test
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS* Available

HALOGEN FREE Available

GREEN (5-2008) Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER $P_{70\,°C}$ W	LIMITING ELEMENT VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
L0603	0603	0.1 to 9.99	0.125	50	1, 2, 3, 5, 10	50, 100, 200, 300
L0805	0805	0.1 to 9.99	0.2	50	1, 2, 3, 5, 10	50, 100, 200, 300
L1206	1206	0.1 to 9.99	0.33	50	1, 2, 3, 5, 10	50, 100, 200, 300
L1505	1505	0.1 to 9.99	0.5	50	1, 2, 3, 5, 10	50, 100, 200, 300
L2010	2010	0.1 to 9.99	1.0	50	1, 2, 3, 5, 10	50, 100, 200, 300
L2512	2512	0.1 to 9.99	2.0 (1)	50	1, 2, 3, 5, 10	50, 100, 200, 300

Note

(1) With special assembly care

CLIMATIC SPECIFICATIONS

Operating temperature range	-55 °C; +155 °C

MECHANICAL SPECIFICATIONS

Substrate	Alumina
Technology	NiCr + Ta_2O_5
Coating	Silicone
Terminations	Solderable **B type:** SnPb over nickel barrier **N type:** SnAg over nickel barrier **G type:** Gold over nickel barrier

Note

- Refer to Application Note “Guidelines for Vishay Sfernice Resistive and Inductive Components” (document number: 52029) for recommended reflow profile. Profile #3 applies

TOLERANCE AND TCR VS. OHMIC VALUE

OHMIC VALUE RANGE in Ω	TIGHTEST TOLERANCE (%)	BEST TCR (ppm/°C)	TERMINATIONS
0R1 < 0R25	1	300	N or B
0R25 < 0R5	1	200	N or B
0R5 < 2R5	1	100	N or B
2R5 < 9R99	1	50	N or B
0R1 < 0R25	5	300	G
0R25 < 0R5	5	200	G
0R5 < 1R	5	100	G
1R < 2R5	3	100	G
2R5 to 9R99	3	50	G

For technical questions, contact: sferthinfilm@vishay.com

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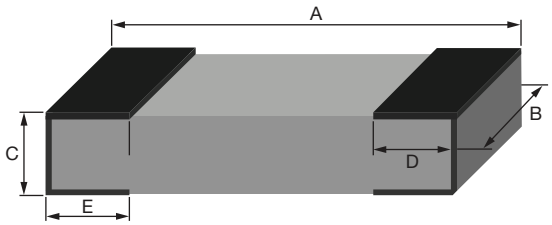
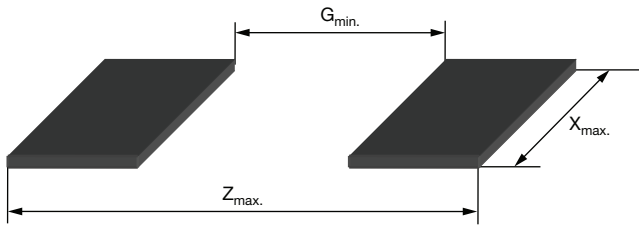
DIMENSIONS in millimeters (inches)



CASE SIZE	A	B	C	D/E
	± 0.152 (± 0.006)	± 0.127 (± 0.005)	± 0.127 (+ 0.005)	± 0.127 (± 0.005)
0603	1.52 (0.060)	0.85 (0.033)	0.5 (0.020)	0.38 (0.015)
0805	1.91 (0.075)	1.27 (0.050)		
1206	3.06 (0.120)	1.60 (0.063)		0.40 (0.016)
1505	3.81 (0.150)	1.32 (0.052)		0.48 (0.019)
2010	5.08 (0.200)	2.54 (0.100)		
2512	6.30 (0.248)	3.30 (0.129)		

SUGGESTED LAND PATTERN in millimeters (inches) (to IPC-7351A)



CASE SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0603	2.37 (0.093)	0.35 (0.014)	0.98 (0.039)
0805	2.76 (0.109)	0.74 (0.029)	1.40 (0.055)
1206	3.91 (0.154)	1.85 (0.073)	1.73 (0.068)
1505	4.66 (0.183)	2.44 (0.096)	1.45 (0.057)
2010	5.93 (0.233)	3.71 (0.146)	2.67 (0.105)
2512	7.15 (0.281)	4.93 (0.194)	3.43 (0.135)

Option: Enlarged Terminations: 0063

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heat sinks (see application note: “Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film)”: www.vishay.com/doc?53048).

For enlarged terminations: Please consult Vishay Sfernice.

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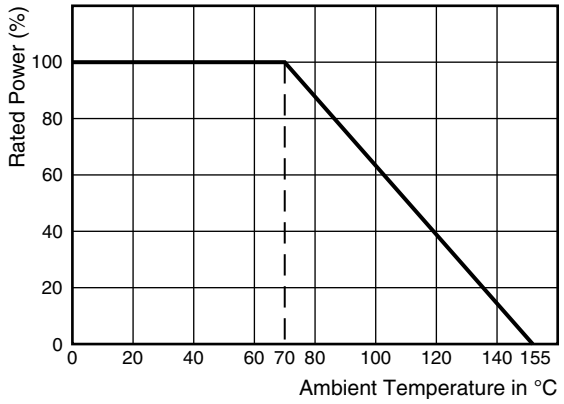
POWER DERATING CURVE



PACKAGING

Several types of packaging are proposed: waffle-pack and tape and reel

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" × 2"	TAPE AND REEL		
			MIN.	MAX.	
0603	100	100	100	5000	8 mm
0805				4000	
1206		140			
1505		60			12 mm
2010				2000	
2512		50			

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover. **To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code**.

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided. **When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code**.

PERFORMANCE

TESTS	CONDITIONS	VALUES AND DRIFT	
		MIL-R-55342 REQUIREMENTS	TYPICAL PERFORMANCES
Thermal shock	MIL-R-55342 C MIL-STD-702, method 107	± 0.25 %	± 0.02 %
Short time overload	MIL-R-55342 C PARA 3.10.4.7.5	± 0.10 %	± 0.01 %
Low temperature operation	MIL-R-55342 C PARA 3.9 and 4.7.4	± 0.25 %	± 0.01 %
Resistance to solder heat	MIL-R-55342 C PARA 3.12, 4.7.7, 4.7.1.2	± 0.25 %	± 0.04 %
Moisture resistance	MIL-R-55342 C PARA 3.13 and 4.7.8 MIL-STD-202, method 106	± 0.40 %	± 0.01 %
	AEC-Q200 85 °C / 85 % RH / 0.1 Pn 1000 h	-	Max. < 0.5 % + 0.05 Ω
High temperature	MIL-R-55342 C PARA 3.11 and 4.7.6	± 0.20 %	± 0.075 %
Load life	MIL-R-55342 C 2000 h Pn at 70 °C MIL-STD-202, method 108	± 0.50 %	± 0.15 %

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GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: L0805K1R00FBT0099

L	0	8	0	5	K	1	R	0	0	F	B	T	0	0	9	9

GLOBAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION (1)	PACKAGING	OPTION
L	**0603** **0805** **1206** **1505** **2010** **2512**	**H** = ± 50 ppm **K** = ± 100 ppm **L** = ± 200 ppm **M** = ± 300 ppm	R designated decimal point For values under 1R Rxxx	**F** = ± 1 % **G** = ± 2 % **H** = ± 3 % **J** = ± 5 % **K** = ± 10 %	**B**: SnPb over nickel barrier **N**: SnAg over nickel barrier **G**: gold over nickel barrier	For more information see Codification of Packaging table	Leave blank if no option

Historical Part Number Example: L 0805 K 1R00 1 % B T R0099

L	0805	K	1R00	1 %	B	T	R0099
MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION

Note

(1) **B**: lead bearing version
N and **G**: lead (Pb)-free / RoHS version

CODIFICATION OF PACKAGING

CODE 18	PACKAGING
WAFFLE PACK	
W	100 min., 1 mult.
WA	100 min., 100 mult. (available only in size 1206)
PLASTIC TAPE (Standard for all sizes)	
T	100 min., 1 mult.
TA	100 min., 100 mult.
TB	250 min., 250 mult.
TC	500 min., 500 mult.
TD	1000 min., 1000 mult.
TE	2500 min., 2500 mult.
TF	Full tape (quantity depending on size of chips)
PAPER TAPE (Available for 0603, 0805, and 1206. Please consult Vishay Sfernice for other sizes)	
PT	100 min., 1 mult.
PA	100 min., 100 mult.
PB	250 min., 250 mult.
PC	500 min., 500 mult.
PD	1000 min., 1000 mult.
PE	2500 min., 2500 mult.
PF	Full tape (quantity depending on size of chips)

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