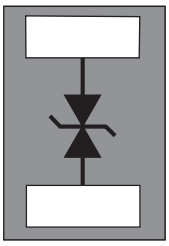
ESDZV5HS-1BF4

Datasheet

Ultra-low clamping single line bidirectional ESD protection

0201 WLCSP package



Features

- Ultra-low clamping voltage:
  - 10 V (IEC 61000-4-2 contact discharge 8 kV at 30 ns / 16 A TLP)
- Bidirectional and symmetrical device
- High holding voltage for DC line protection
- 0201 WLCSP package
- Complies with the following standards: IEC 61000-4-2 level 4
  - ±15 kV (air discharge)
  - ±10 kV (contact discharge)
- ECOPACK®2 compliant component

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablet and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status link
ESDZV5HS-1BF4

Description

The ESDZV5HS-1BF4 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

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1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	±10 ±15	kV
P_{pp}	Peak pulse power (8/20 µs)		40	W
I_{pp}	Peak pulse current (8/20 µs)		4	A
T_j	Operating junction temperature range		-55 to +150	°C
T_{stg}	Storage junction temperature range		-65 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics (definitions)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
V_H	Holding voltage
I_{RM}	Leakage current at V_{RM}
I_{PP}	Peak pulse current
V_{Trig}	Triggering voltage
C_{line}	Input capacitance per line
R_D	Dynamic resistance

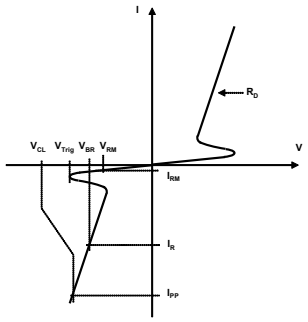

Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{trig}			10	12	13.5	V
V_H			6.5	7		V
I_{RM}	Leakage current	V_{RM} = 5.5 V			100	nA
V_{CL}	Clamping voltage	IEC 61000-4-2, 8 kV contact discharge measured after 30 ns		10		V
R_D	Dynamic resistance, pulse duration 100 ns			0.18		Ω
C_{LINE}	Line capacitance	V_{LINE} = 0 V, F = 1 MHz, V_{OSC} = 30 mV		4	4.5	pF

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1.1 Characteristics (curves)

Figure 2. Variation of leakage current versus junction temperature (typical values)

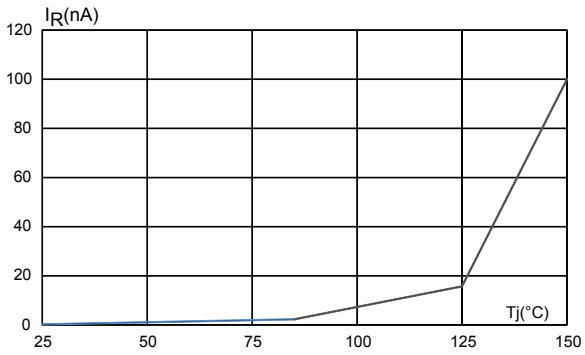


Figure 3. Junction capacitance versus frequency

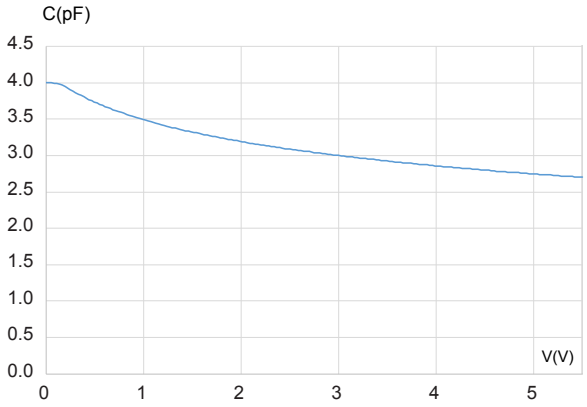


Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

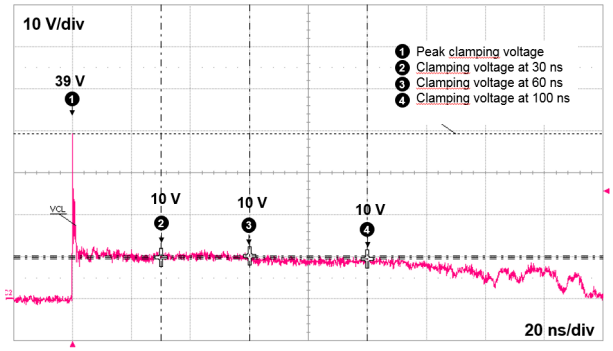


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

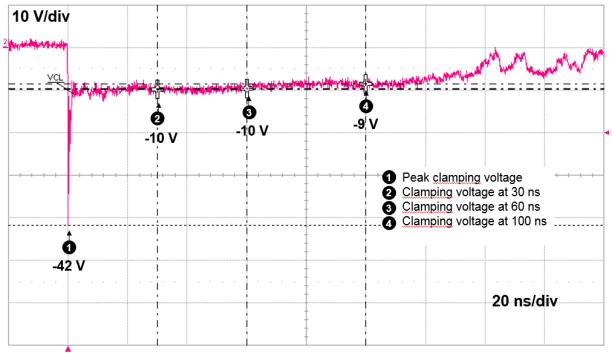


Figure 6. TLP

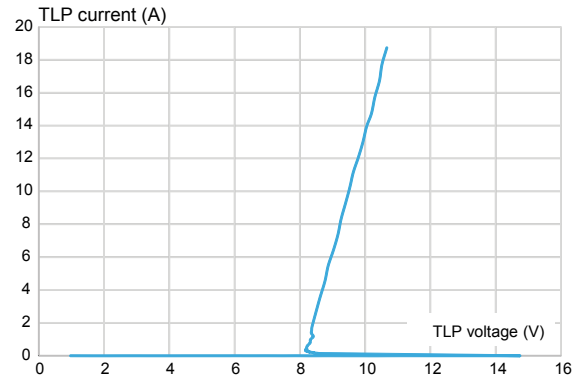
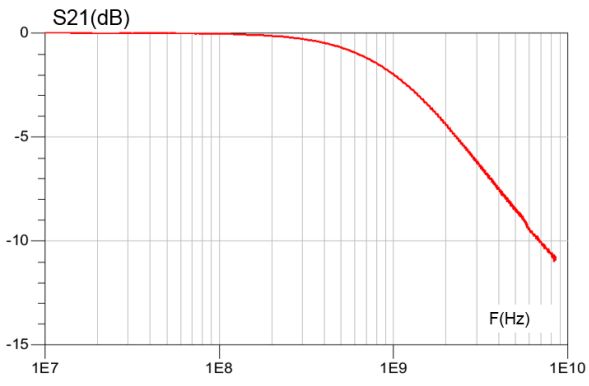


Figure 7. S21 attenuation



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2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 0201 WLCSP package information

Figure 8. 0201 WLCSP package outline

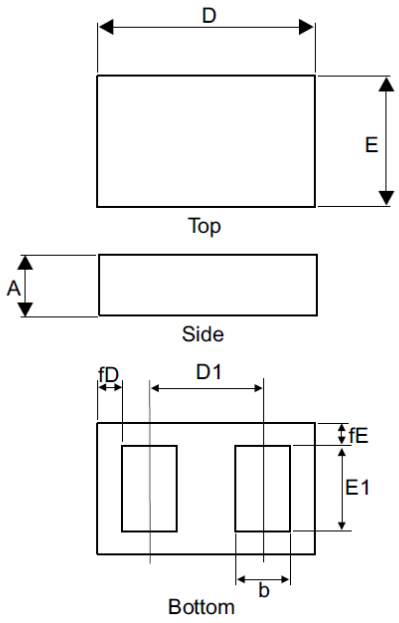

Table 3. 0201 WLCSP package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.270	0.300	0.330
b	0.1675	0.1875	0.2075
D	0.560	0.580	0.600
D1		0.3375	
E	0.260	0.280	0.300
E1	0.205	0.225	0.245
fD	0.0175	0.0275	0.0375
fE	0.0175	0.0275	0.070

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Figure 9. **Marking**

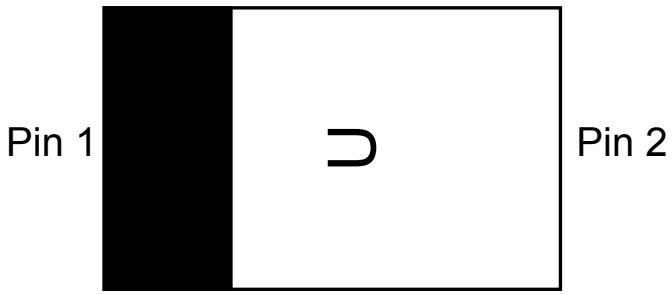
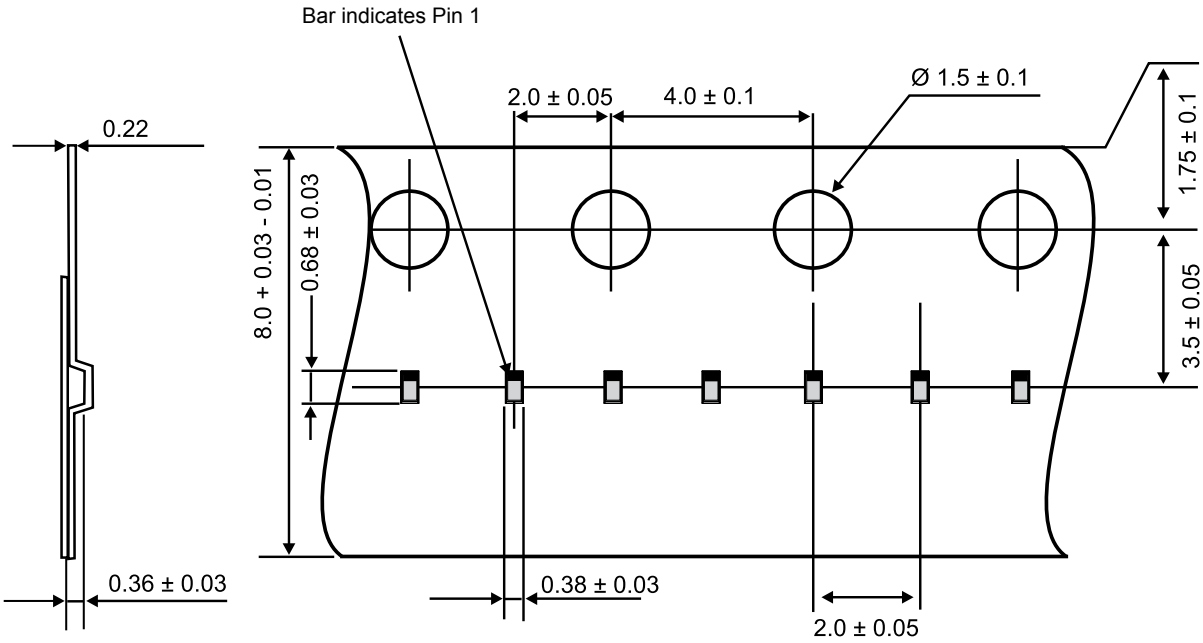


Figure 10. **Tape and reel specification**



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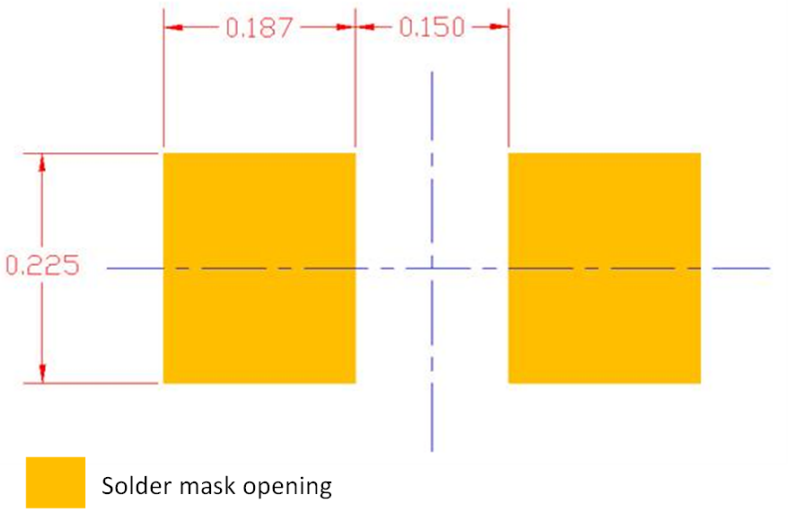
3 Recommendation on PCB assembly

3.1 Footprint

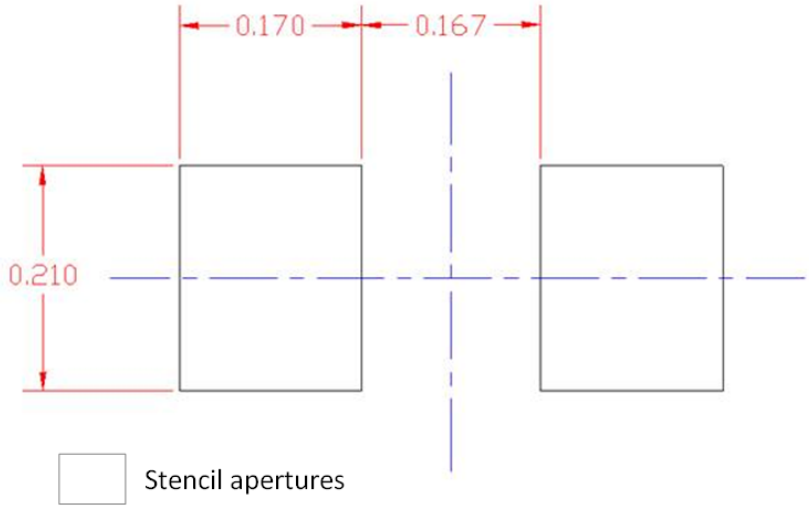
Figure 11. **Footprint in mm**



3.2 Stencil opening design

1. Recommended design reference
   a. Stencil opening dimensions: 75 µm / 3 mils

Figure 12. **Stencil opening recommendations**



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3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

3.4 Placement

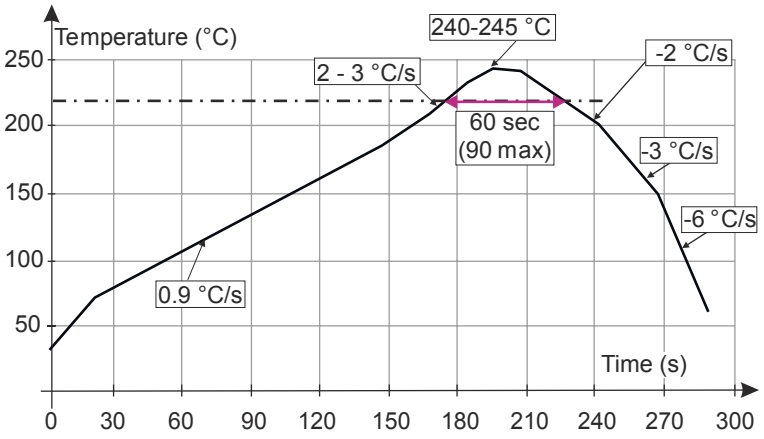
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 13. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

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4 Ordering information

Figure 15. **Ordering information scheme**

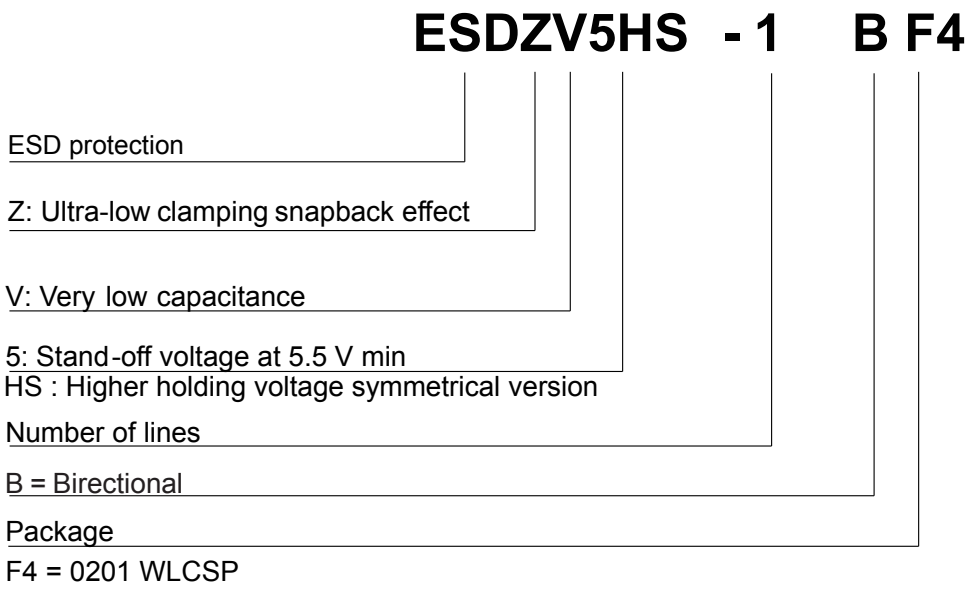

Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDZV5HS-1BF4	U	0201 WLCSP	0.116 mg	15000	Tape and reel

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Revision history

Table 5. **Document revision history**

Date	Revision	Changes
02-Nov-2017	1	Initial release.
16-Feb-2018	2	Updated Table 3: "0201 package mechanical data".
28-Jun-2018	3	Updated package information naming.

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