

C3M0032120K

Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

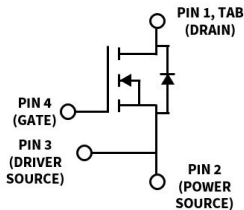
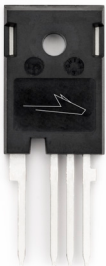
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Typical Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

Package



Part Number	Package	Marking
C3M0032120K	TO-247-4L	C3M0032120K

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			69	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19
				53		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			264		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			341	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design


Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6	V	$V_{DS} = V_{GS}, I_D = 11.5\text{ mA}$	Fig. 11
			2.0		V	$V_{DS} = V_{GS}, I_D = 11.5\text{ mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance	23	32	43	m Ω	$V_{GS} = 15\text{ V}, I_D = 40\text{ A}$	Fig. 4, 5, 6
			57.6			$V_{GS} = 15\text{ V}, I_D = 40\text{ A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		27		S	$V_{DS} = 20\text{ V}, I_{DS} = 40\text{ A}$	Fig. 7
			22			$V_{DS} = 20\text{ V}, I_{DS} = 40\text{ A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		3357		pF	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V}$ $F = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		129				
C_{rss}	Reverse Transfer Capacitance		8				
E_{oss}	C_{oss} Stored Energy		76		μJ		Fig. 16
E_{ON}	Turn-On Switching Energy (External Diode)		367		μJ	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 40\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 65.7\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$	Fig. 26
E_{OFF}	Turn Off Switching Energy (External Diode)		123				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		955		μJ	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 40\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 65.7\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		107				
$t_{d(on)}$	Turn-On Delay Time		25		ns	$V_{DD} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 40\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 65.7\text{ }\mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 27
t_r	Rise Time		18				
$t_{d(off)}$	Turn-Off Delay Time		32				
t_f	Fall Time		9				
$R_{G(int)}$	Internal Gate Resistance		1.7		Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Q_{gs}	Gate to Source Charge		40		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 40\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		34				
Q_g	Total Gate Charge		118				



Reverse Diode Characteristics (T_c = 25 °C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V _{SD}	Diode Forward Voltage	4.6		V	V _{GS} = -4 V, I _{SD} = 20 A, T _J = 25 °C	Fig. 8, 9, 10
		4.2		V	V _{GS} = -4 V, I _{SD} = 20 A, T _J = 175 °C	
I _S	Continuous Diode Forward Current		62	A	V _{GS} = -4 V, T _C = 25 °C	
I _{SM}	Diode pulse Current		264	A	V _{GS} = -4 V, pulse width t _p limited by T _{Jmax}	
t _{rr}	Reverse Recover time	27		ns	V _{GS} = -4 V, I _{SD} = 40 A, V _R = 800 V dif/dt = 2250 A/μs, T _J = 175 °C	
Q _{rr}	Reverse Recovery Charge	478		nC		
I _{rrm}	Peak Reverse Recovery Current	27		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
R _{JA}	Thermal Resistance Junction to Ambient	40	°C/W		Fig. 21
R _{θJC}	Thermal Resistance from Junction to Case	0.44			

Typical Performance

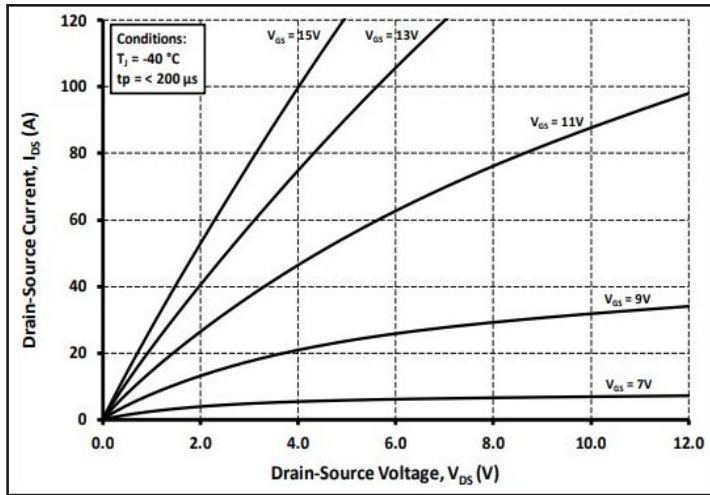
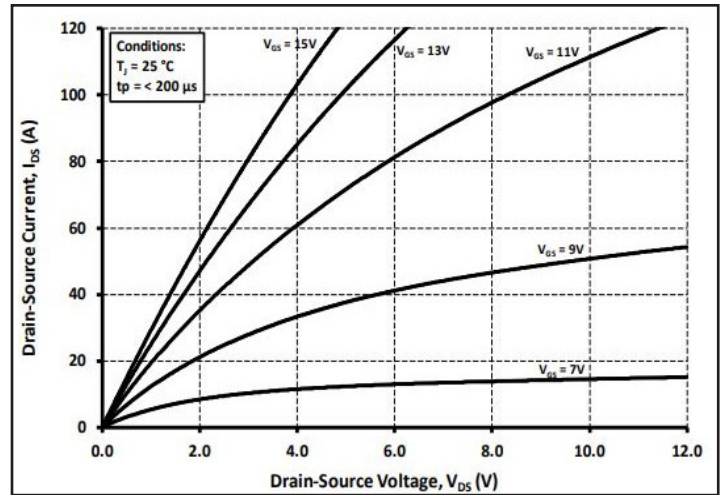
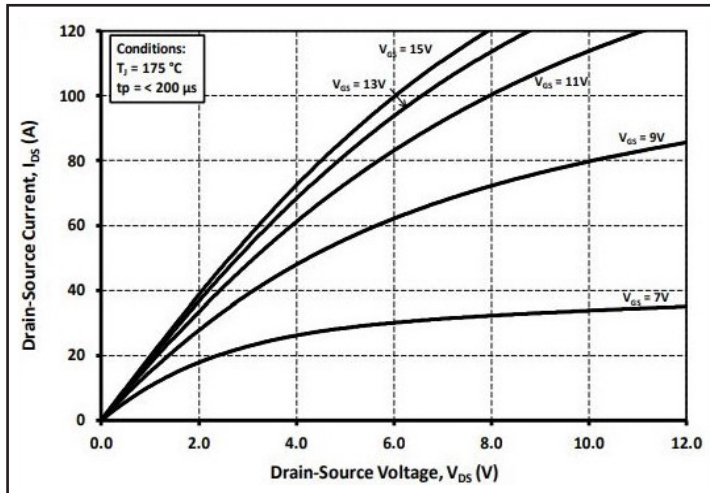
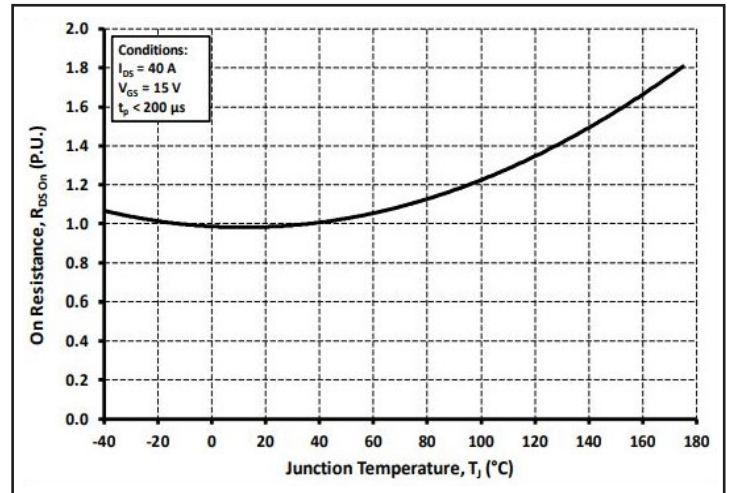
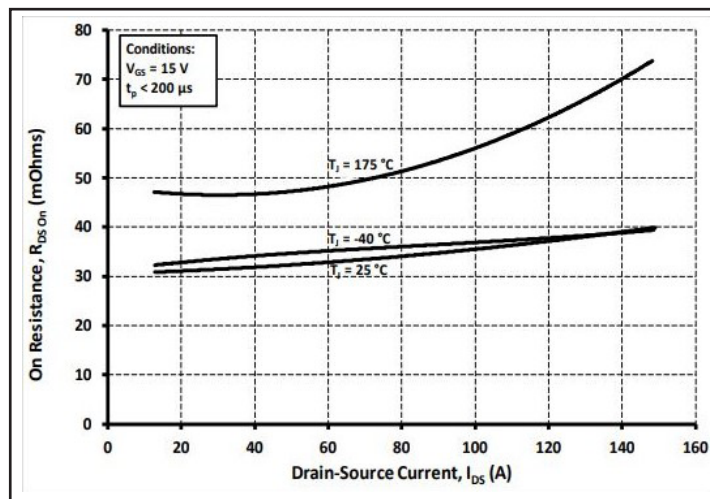
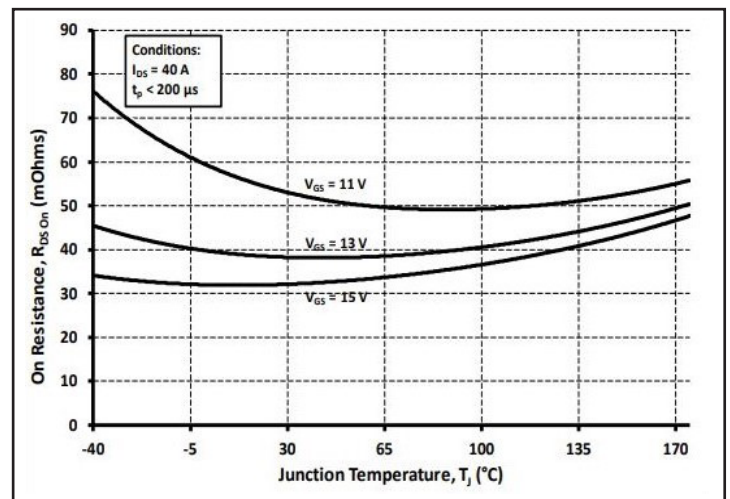
Figure 1. Output Characteristics $T_j = -40\text{ }^{\circ}\text{C}$ Figure 2. Output Characteristics $T_j = 25\text{ }^{\circ}\text{C}$ Figure 3. Output Characteristics $T_j = 175\text{ }^{\circ}\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

Figure 5. On-Resistance vs. Drain Current
For Various TemperaturesFigure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

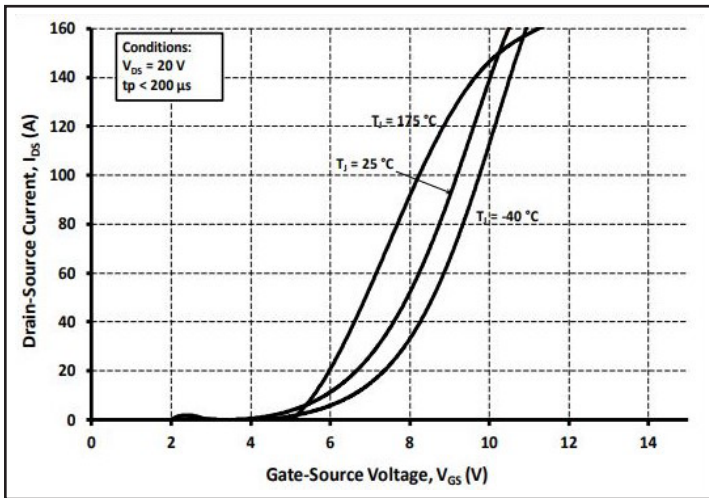


Figure 7. Transfer Characteristic for Various Junction Temperatures

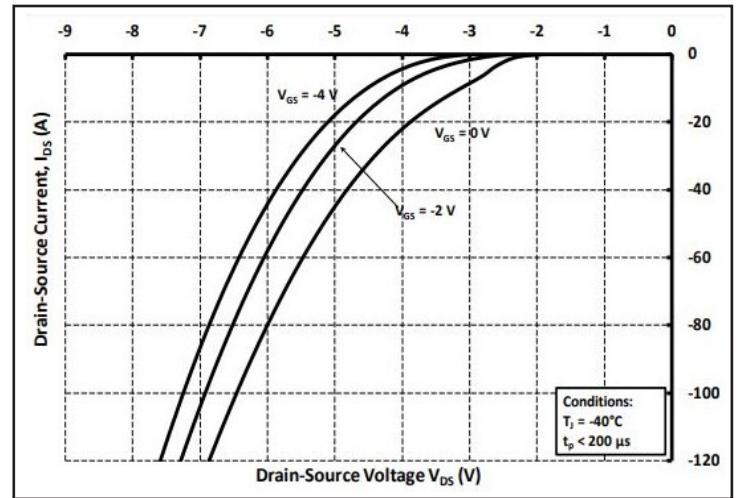


Figure 8. Body Diode Characteristic at -40 °C

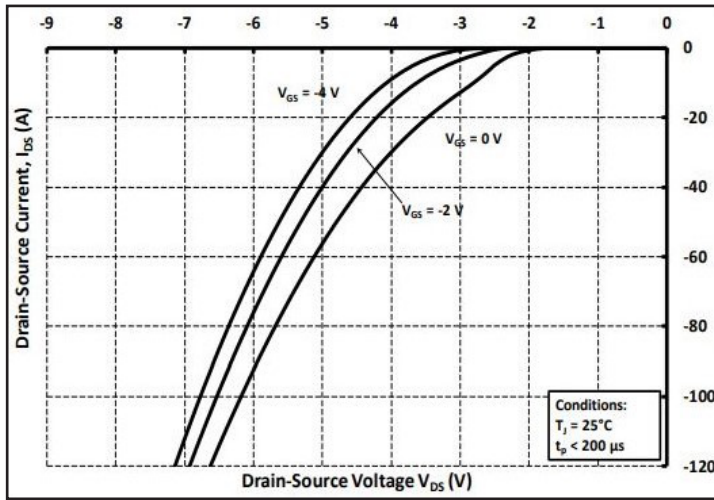


Figure 9. Body Diode Characteristic at 25 °C

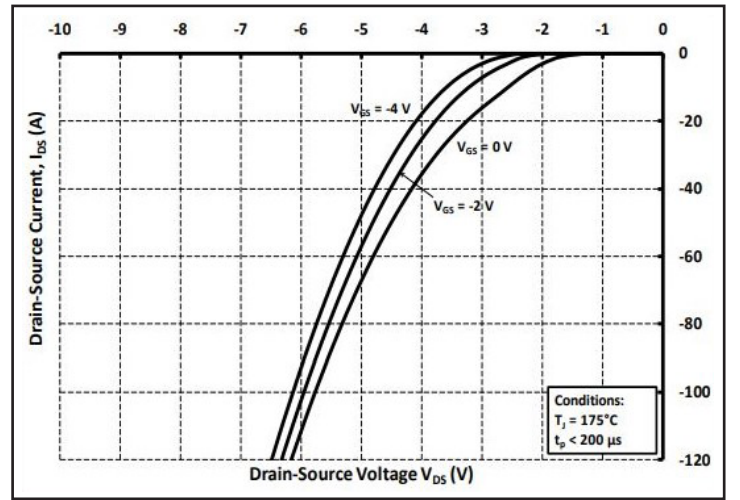


Figure 10. Body Diode Characteristic at 175 °C

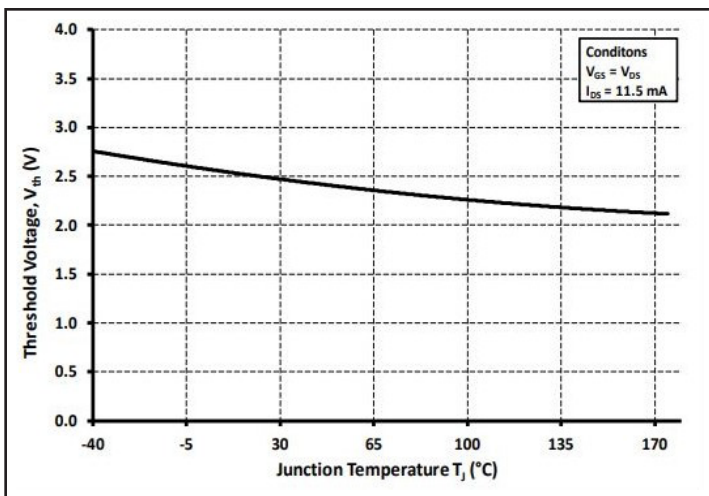


Figure 11. Threshold Voltage vs. Temperature

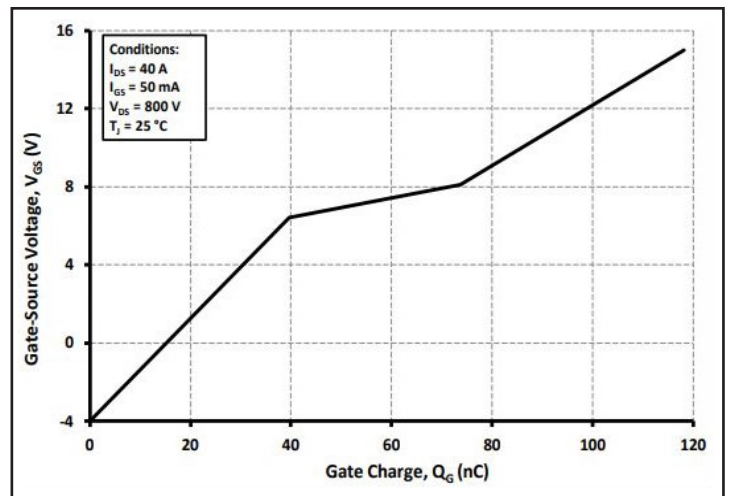


Figure 12. Gate Charge Characteristics

Typical Performance

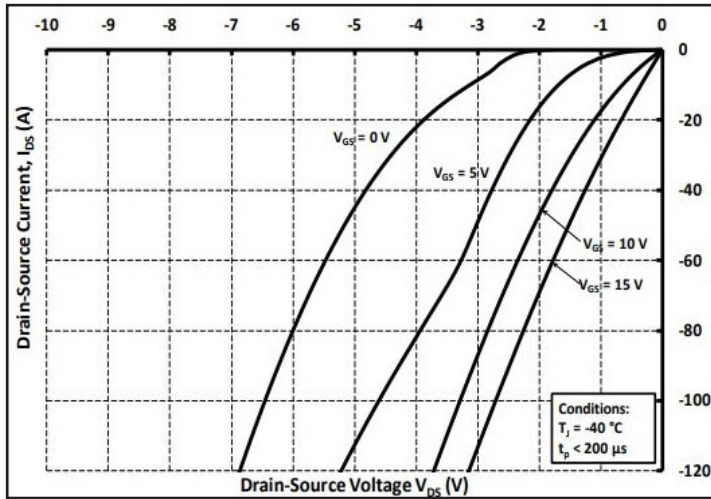


Figure 13. 3rd Quadrant Characteristic at -40 °C

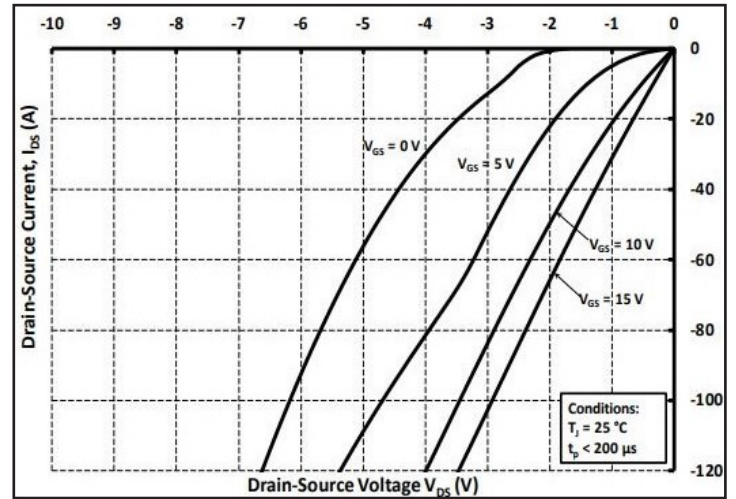


Figure 14. 3rd Quadrant Characteristic at 25 °C

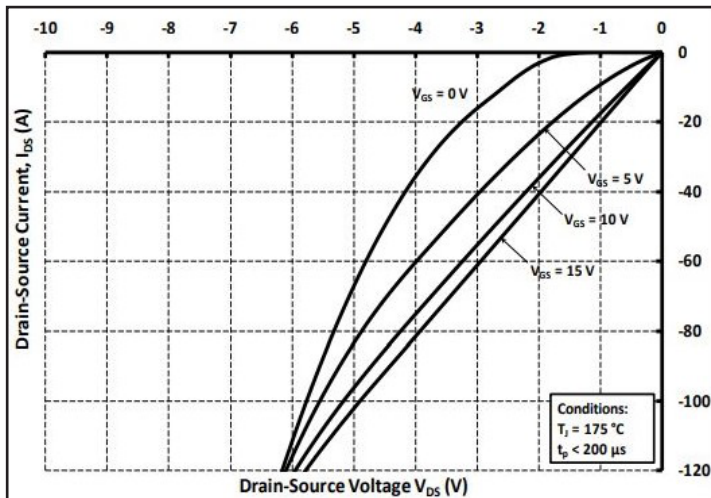


Figure 15. 3rd Quadrant Characteristic at 175 °C

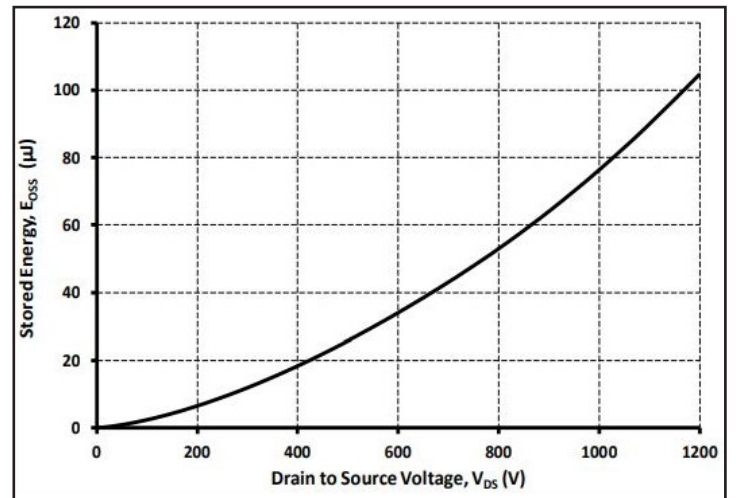


Figure 16. Output Capacitor Stored Energy

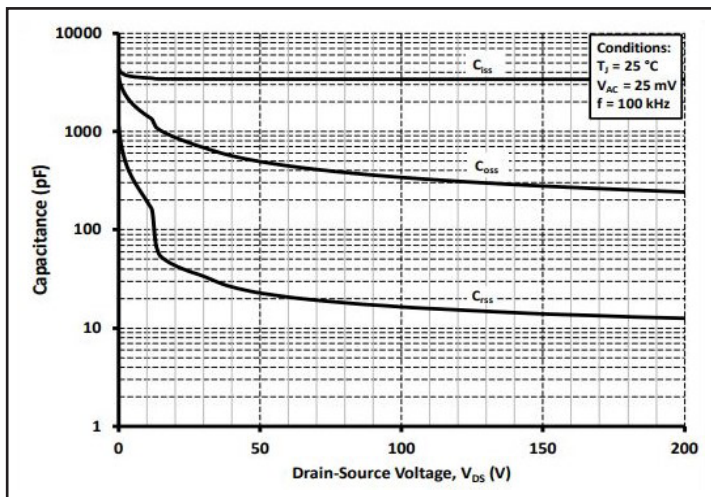


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

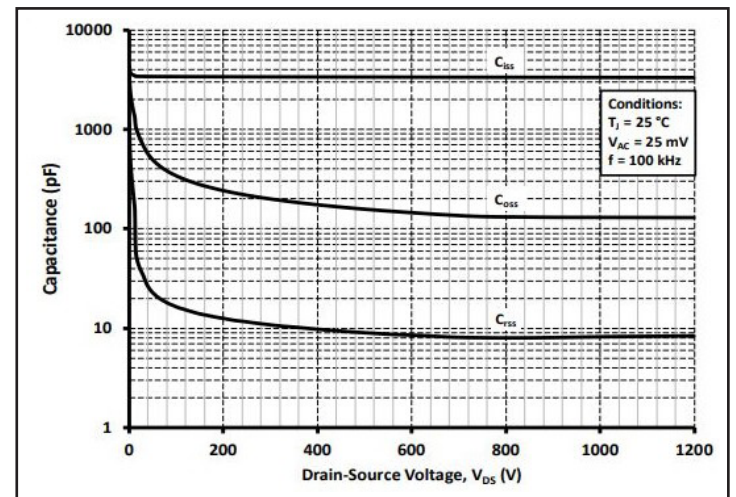


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

Typical Performance

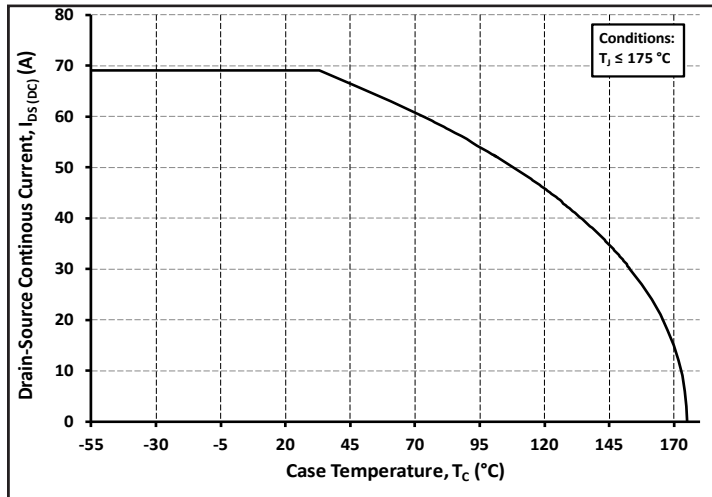


Figure 19. Continuous Drain Current Derating vs. Case Temperature

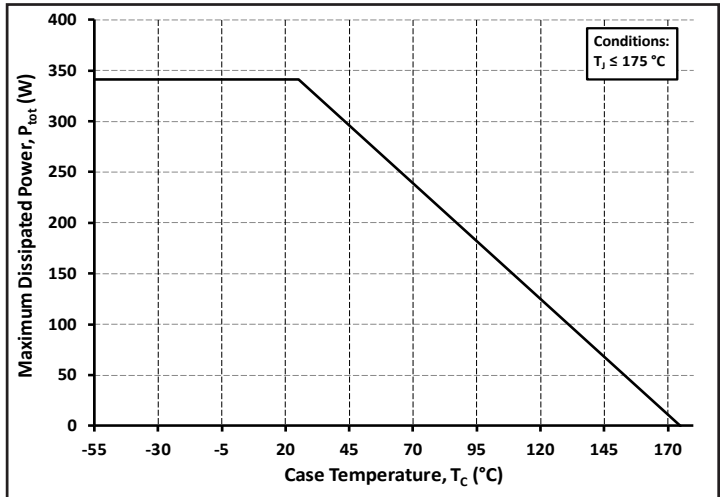


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

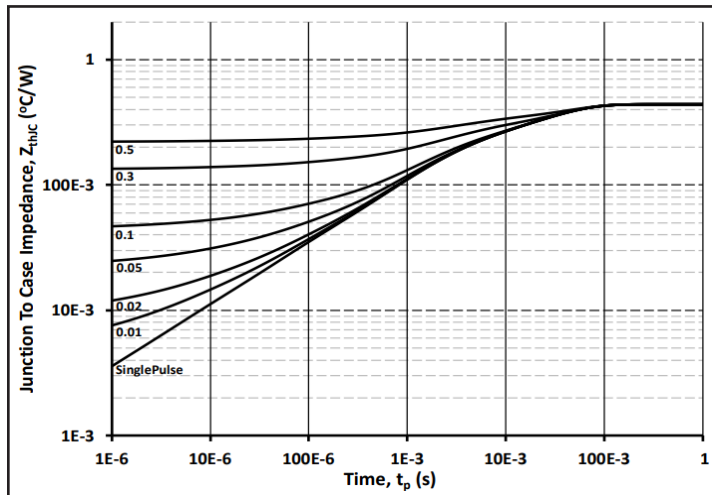


Figure 21. Transient Thermal Impedance (Junction - Case)

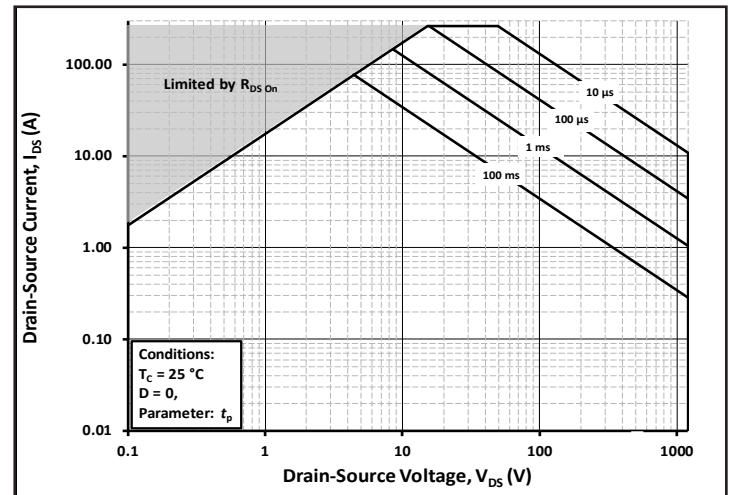


Figure 22. Safe Operating Area

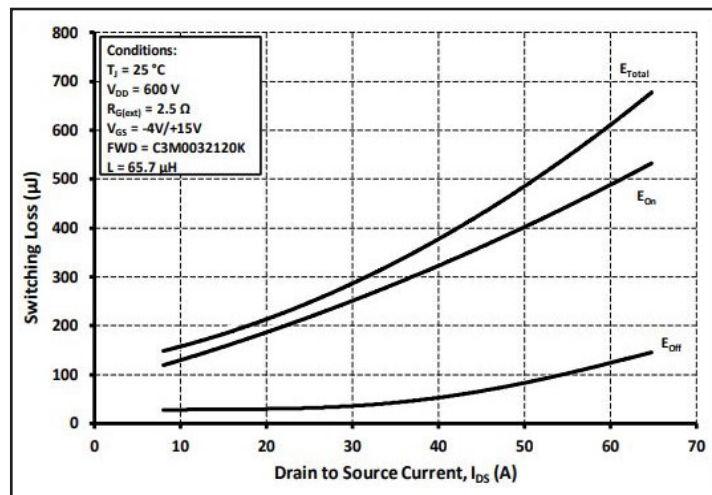


Figure 23. Clamped Inductive Switching Energy vs. Low Drain Current ($V_{DD} = 600V$)

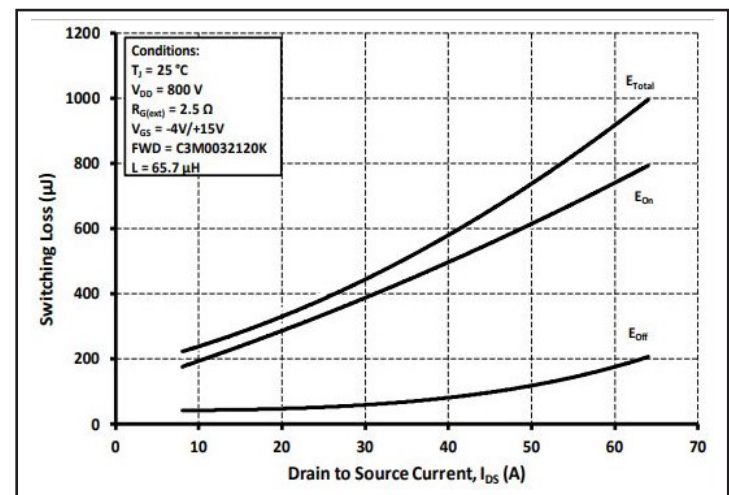


Figure 24. Clamped Inductive Switching Energy vs. High Drain Current ($V_{DD} = 800V$)

Typical Performance

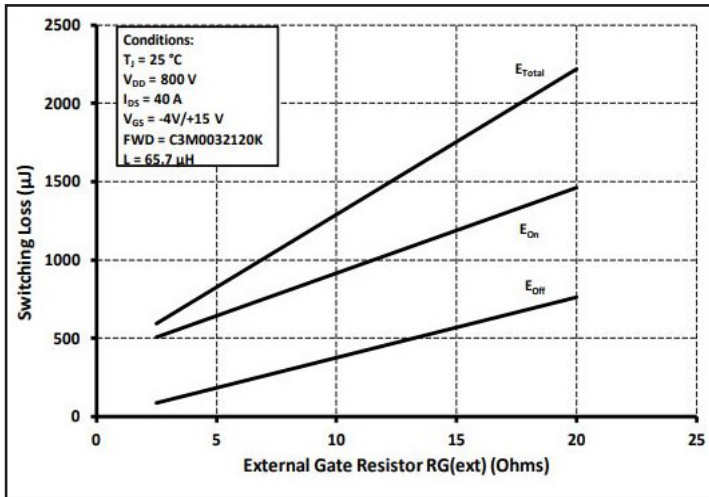


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$

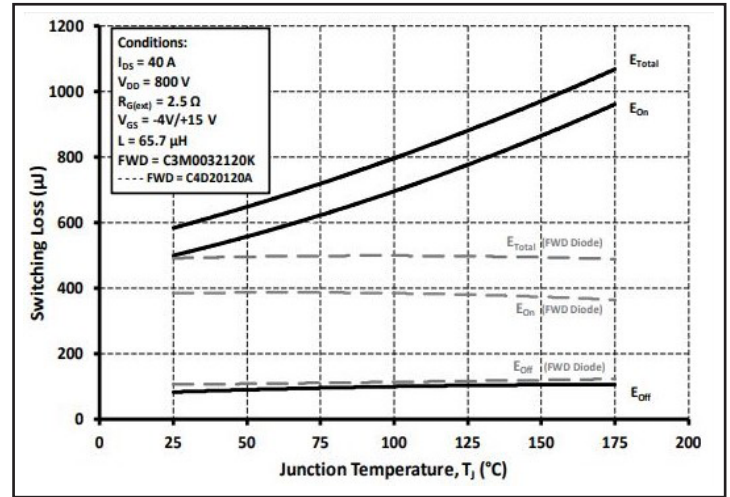


Figure 26. Clamped Inductive Switching Energy vs. Temperature

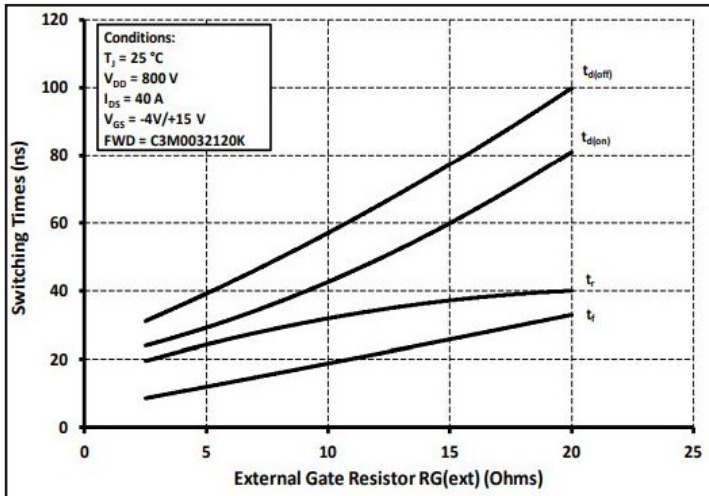


Figure 27. Switching Times vs. $R_{G(\text{ext})}$

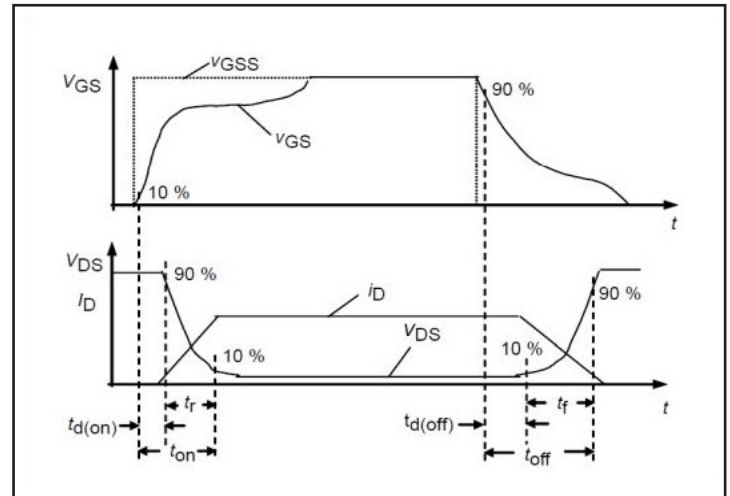


Figure 28. Switching Times Definition



Test Circuit Schematic

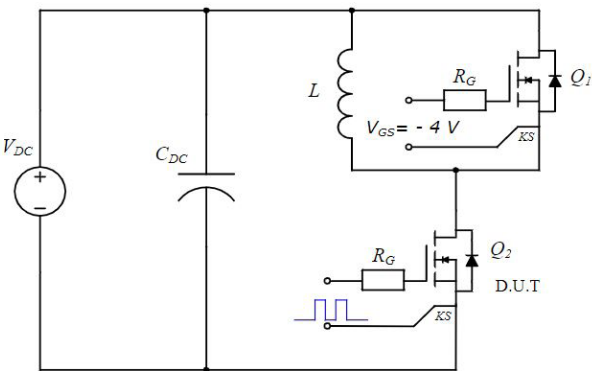
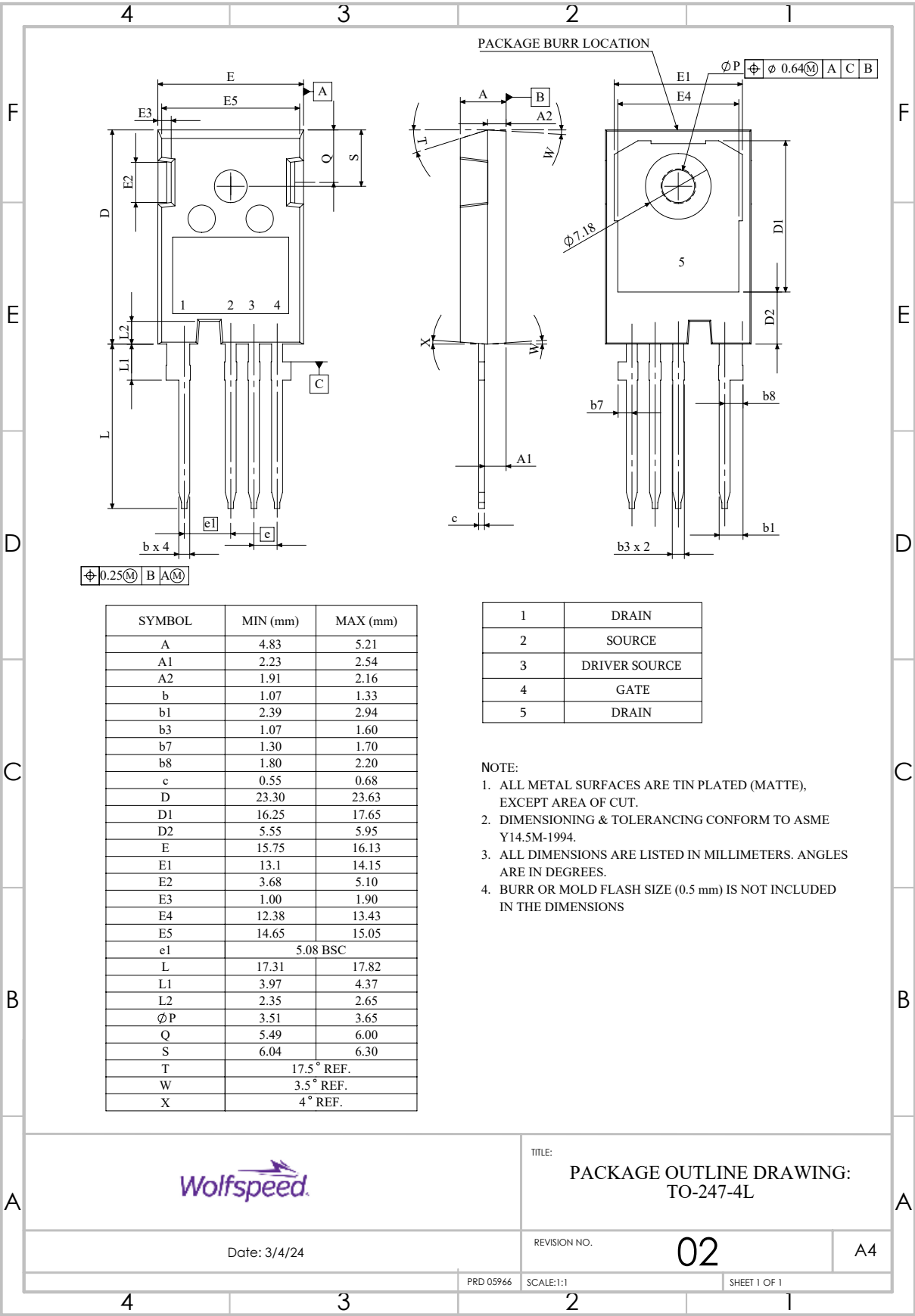


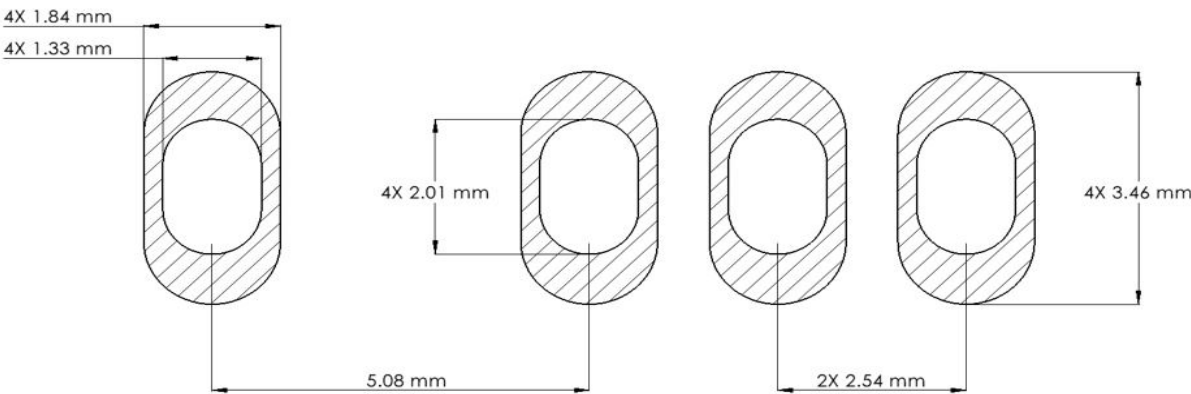
Figure 29. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions





Recommended Solder Pad Layout



Revision history

Document Version	Date of release	Description of changes
3	November-2020	Initial datasheet
4	December-2023	Update Package Drawing, package image, solder pad layout, added revision history table, Table 1 layout revised
5	February-2024	Updated ID, IDM, Pd, and Rthj-c based off latest data
6	September - 2024	Legal Disclaimer and POD



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