N-Channel 80-V (D-S) MOSFET

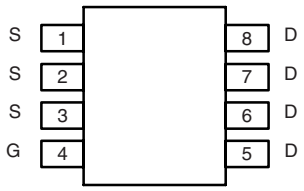
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
80	0.0165 at V_{GS} = 10 V	9.5
	0.022 at V_{GS} = 6.0 V	8.3

FEATURES

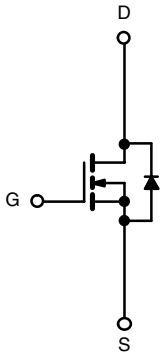
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

SO-8



Top View



N-Channel MOSFET

Ordering Information: Si4896DY-T1-E3 (Lead (Pb)-free)
Si4896DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	80		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	9.5	6.7	A
	T_A = 70 °C		7.6	5.4	
Pulsed Drain Current		I_{DM}	50		
Avalanche Current	L = 0.1 mH	I_{AS}	40		
Continuous Source Current (Diode Conduction)[a]		I_S	2.8	1.4	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	3.1	1.56	W
	T_A = 70 °C		2.0	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	33	40	°C/W
	Steady State		65	80	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.

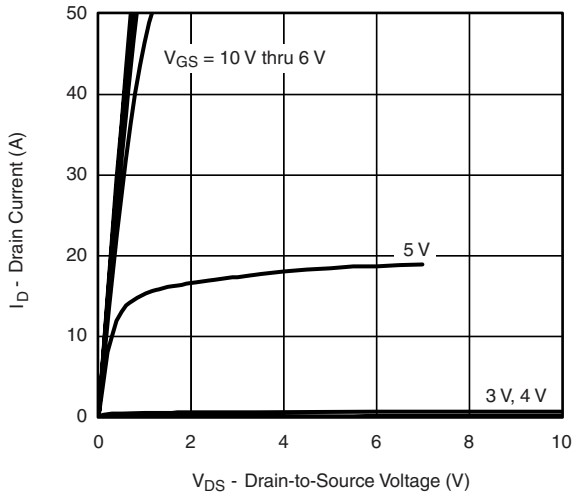
Downloaded from Arrow.com.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 64 V, V_{GS} = 0 V			1	µA
		V_{DS} = 64 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A		0.0135	0.0165	Ω
		V_{GS} = 6.0 V, I_D = 8.0 A		0.0175	0.022	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A		25		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.8 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 10 A		34	41	nC
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			11.0		
Gate Resistance	R_g		0.2	0.85	1.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 40 Ω $I_D \cong$ 1.0 A, V_{GEN} = 10 V, R_g = 6 Ω		17	25	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			31	45	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.8 A, dI/dt = 100 A/µs		45	75	

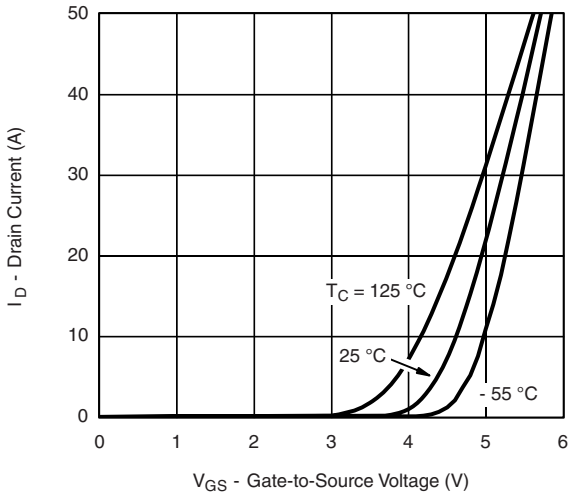
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



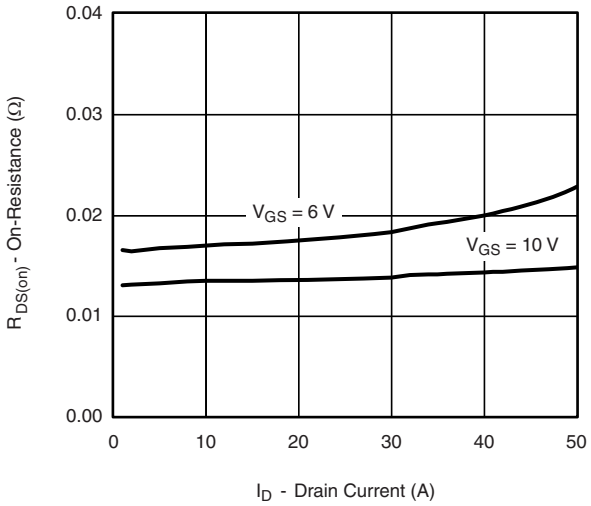
Output Characteristics



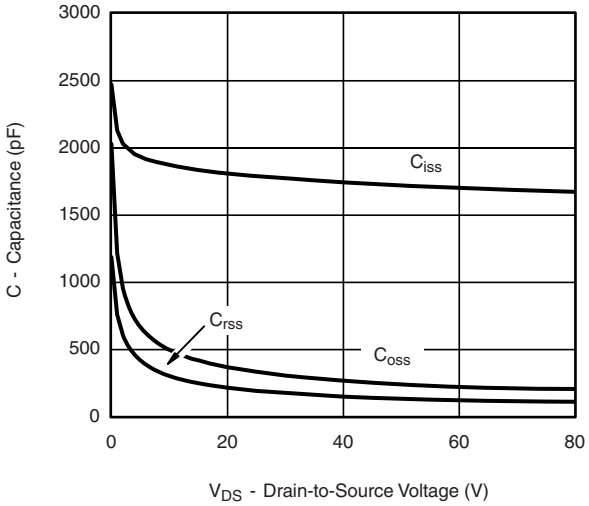
Transfer Characteristics

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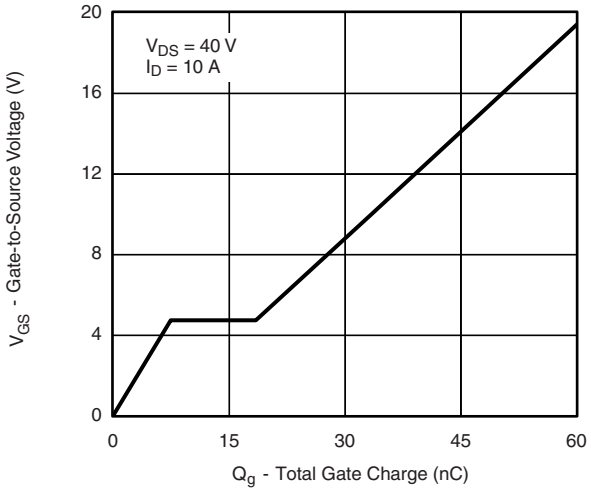
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



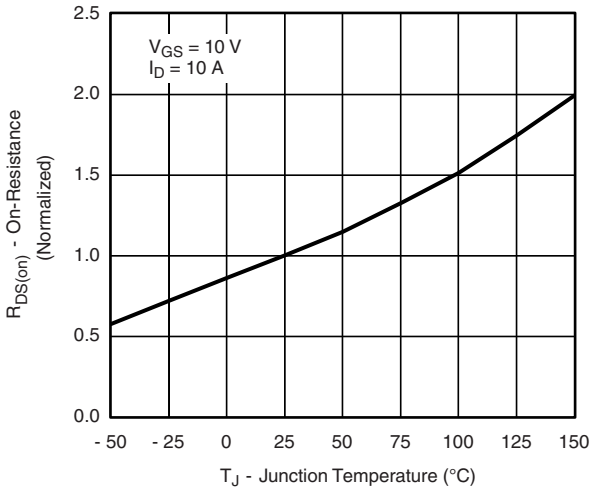
On-Resistance vs. Drain Current



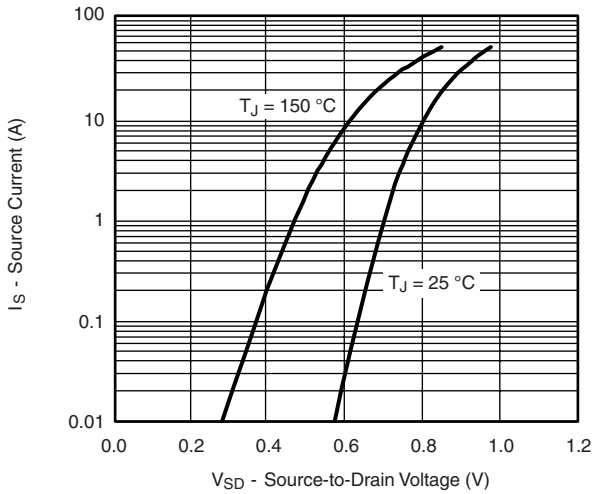
Capacitance



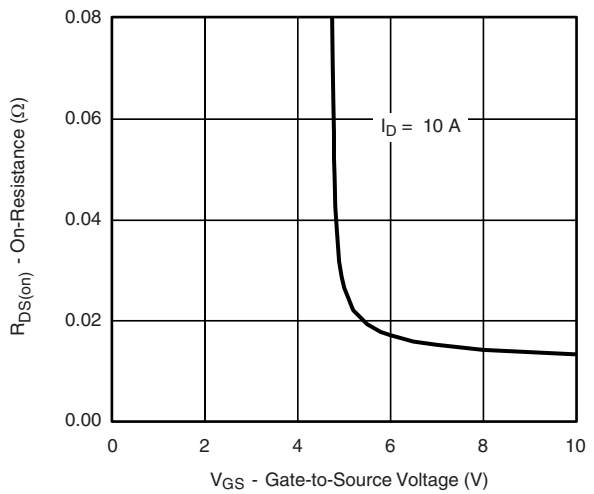
Gate Charge



On-Resistance vs. Junction Temperature



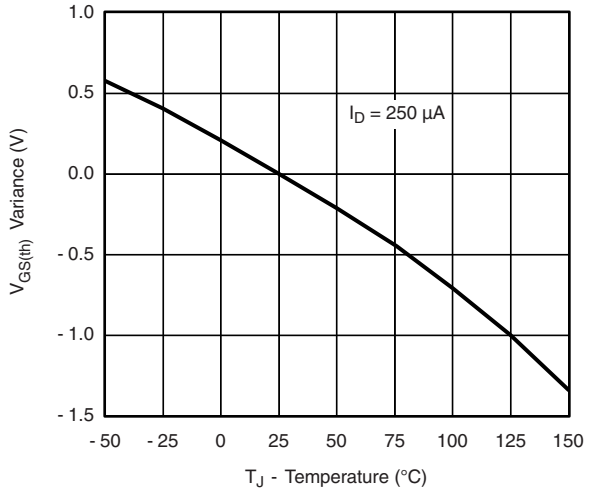
Source-Drain Diode Forward Voltage



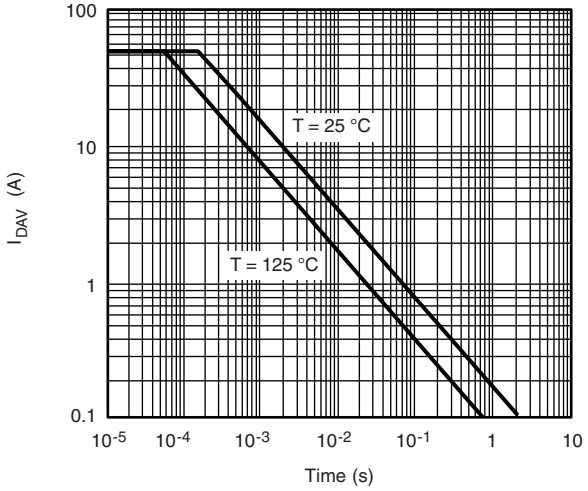
On-Resistance vs. Gate-to-Source Voltage

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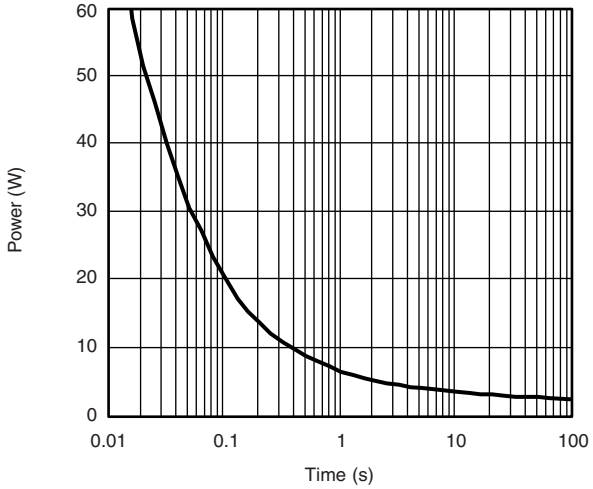
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



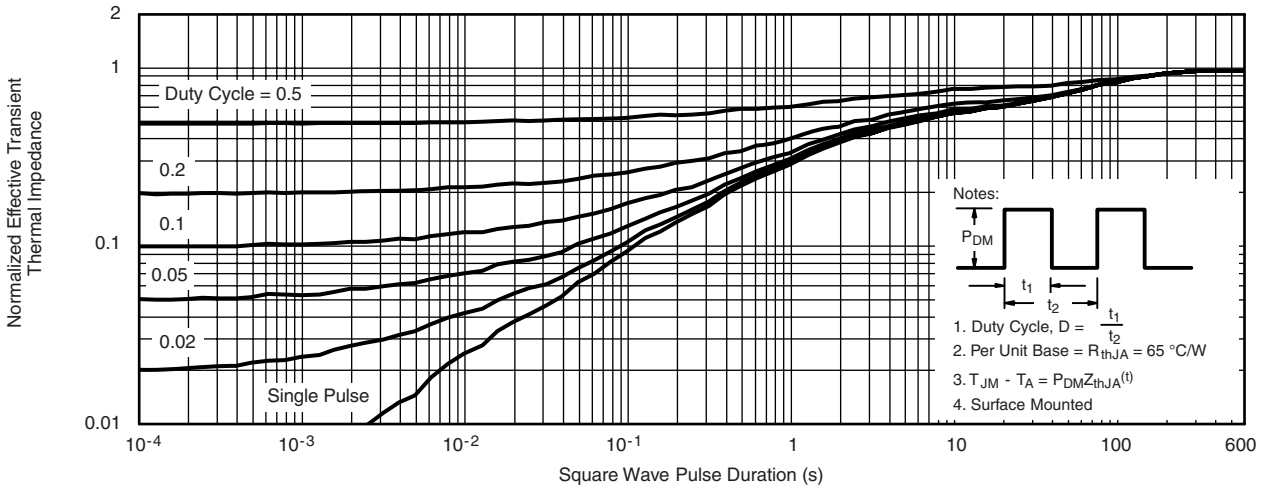
Threshold Voltage



Avalanche Current vs. Time



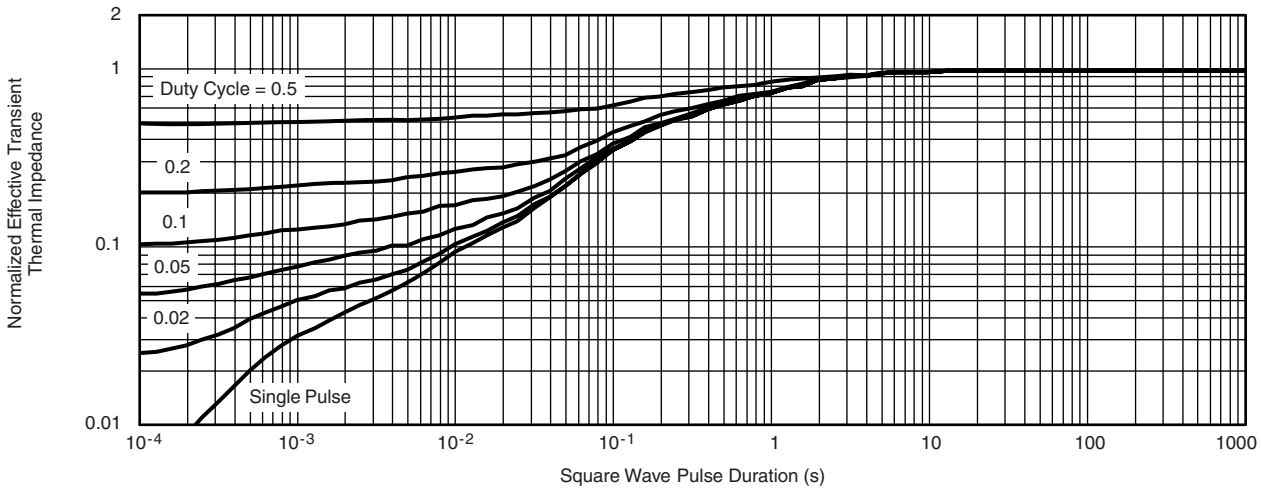
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

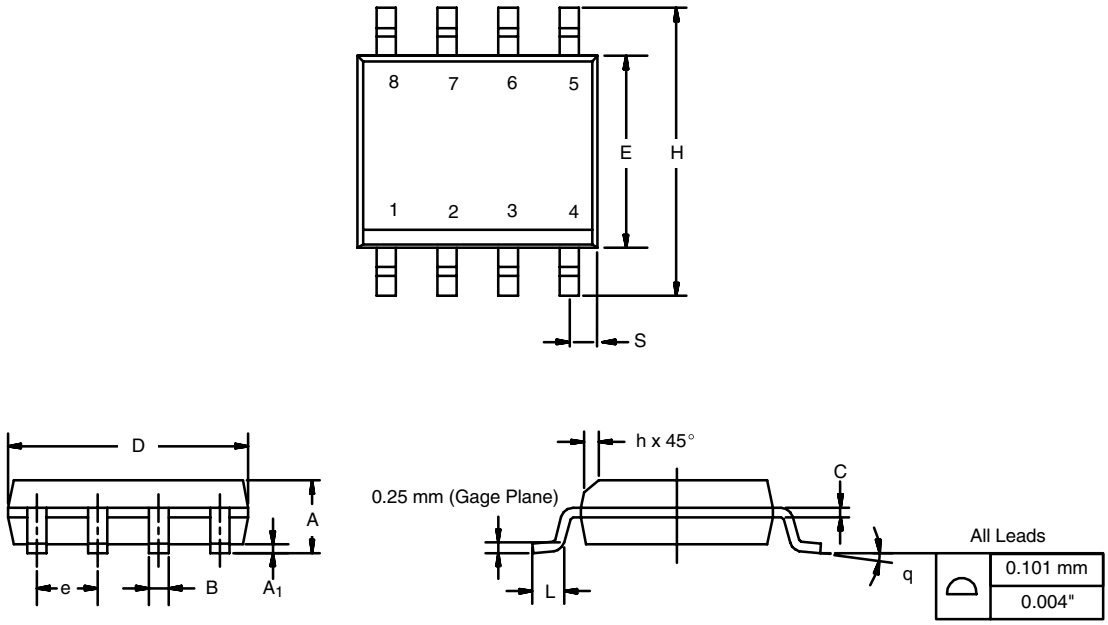


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71300.

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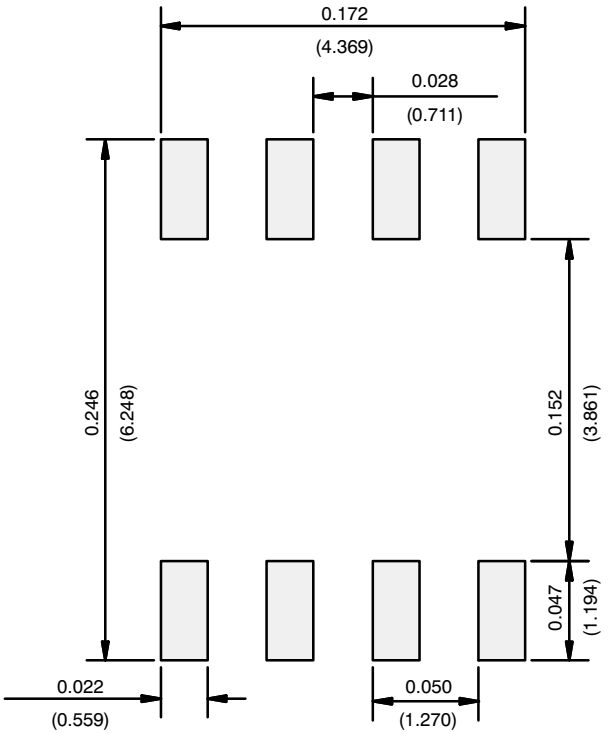
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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