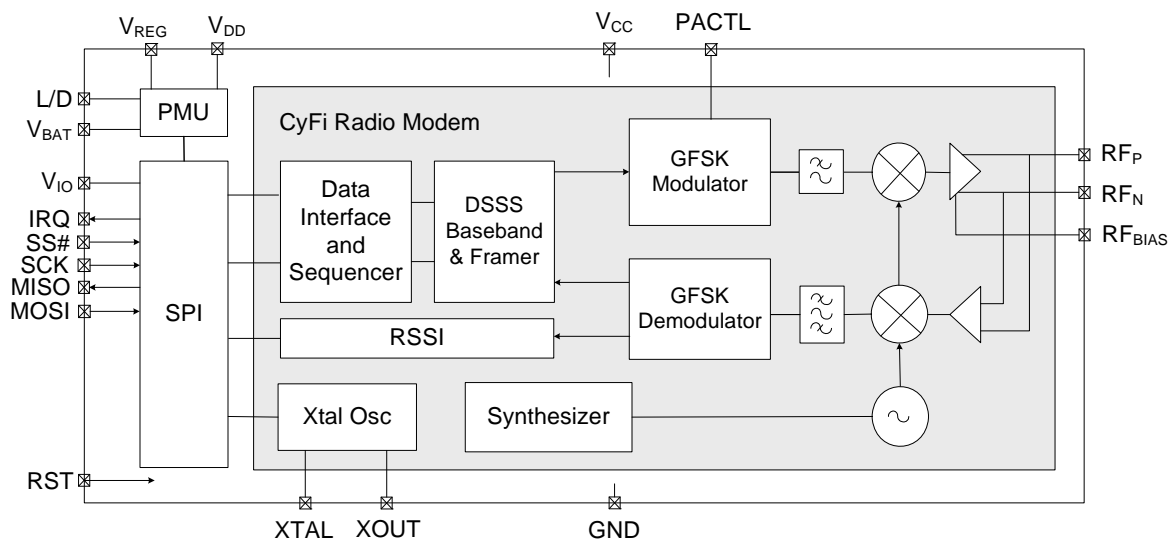


## Features

- 2.4-GHz direct sequence spread spectrum (DSSS) radio transceiver
- Operates in the unlicensed worldwide industrial, scientific, and medical (ISM) band (2.400 GHz to 2.483 GHz)
- 21-mA operating current (transmit at -5 dBm)
- Transmit power up to +4 dBm
- Receive sensitivity up to -97 dBm
- Sleep current less than 1  $\mu$ A
- DSSS data rates up to 250 kbps, Gaussian frequency-shift keying (GFSK) data rate of 1 Mbps
- Low external component count
- Auto transaction sequencer (ATS) - no MCU intervention
- Framing, length, CRC16, and auto acknowledge (ACK)
- Power management unit (PMU) for MCU
- Fast startup and fast channel changes
- Separate 16 byte transmit and receive FIFOs
- Dynamic data rate reception
- Receive signal strength indication (RSSI)
- Serial peripheral interface (SPI) control while in sleep mode
- 4-MHz SPI microcontroller interface
- Battery voltage monitoring circuitry
- Supports coin-cell operated applications

## Logic Block Diagram



- Operating voltage from 1.8 V to 3.6 V
- Operating temperature from 0 °C to 70 °C
- Space saving 40-pin QFN 6 x 6 mm package

## Applications

- Wireless sensor networks
- Wireless actuator control
- Home automation
- White goods
- Commercial building automation
- Automatic meter readers
- Precision agriculture
- Remote controls
- Consumer electronics
- Personal health and fitness
- Toys

## Applications Support

The CYRF7936 CyFi™ transceiver is a radio IC designed for low power embedded wireless applications. It can be used only with Cypress's PSoC programmable system-on-chip. Combined with the PSoC and a CyFi network protocol stack, CYRF7936 can be used to implement a complete CyFi wireless system.

See [www.cypress.com](http://www.cypress.com) for development tools, reference designs, and application notes.

Not recommended for new designs

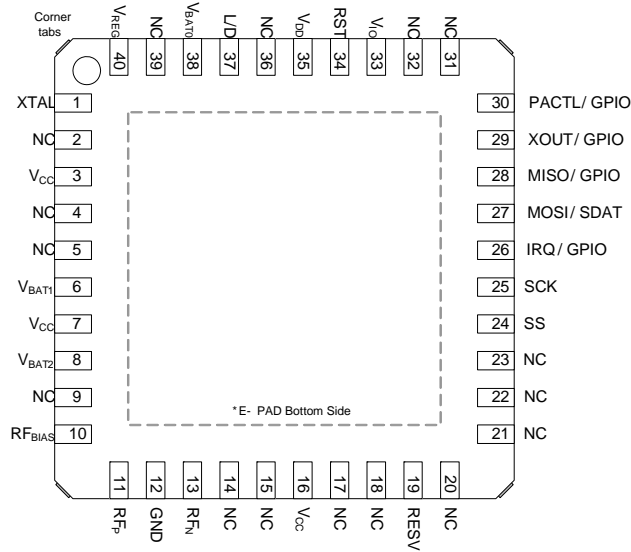
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Not recommended for new designs

Pinouts

Figure 1. Pin Diagram - CYRF7936 40-Pin QFN



Pin Description

CYRF7936 40-Pin QFN

| Pin Number   | Name                  | Type | Default | Description   |
|--|-----------------------|------|---------|---|
| 1  | XTAL                  | I    | I       | 12-MHz crystal  |
| 2, 4, 5, 9, 14, 15, 17, 18, 20, 21, 22, 23, 31, 32, 36, 39 | NC                    | NC   |         | Connect to GND  |
| 3, 7, 16   | V <sub>CC</sub>       | Pwr  |         | V <sub>CC</sub> = 2.4 V to 3.6 V. Typically connected to V <sub>REG</sub> .   |
| 6, 8, 38   | V <sub>BAT(0-2)</sub> | Pwr  |         | V <sub>BAT</sub> = 1.8 V to 3.6 V. Main supply.   |
| 10   | RF <sub>BIAS</sub>    | O    | O       | RF I/O 1.8 V reference voltage  |
| 11   | RF <sub>P</sub>       | I/O  | I       | Differential RF signal to and from antenna  |
| 12   | GND                   | GND  |         | Ground  |
| 13   | RF <sub>N</sub>       | I/O  | I       | Differential RF signal to and from antenna  |
| 19   | RESV                  | I    |         | Must be connected to GND  |
| 24   | SS#                   | I    | I       | SPI enable, active LOW assertion. Enables and frames transfers.   |
| 25   | SCK                   | I    | I       | SPI clock   |
| 26   | IRQ                   | I/O  | O       | Interrupt output (configurable active HIGH or LOW), or GPIO   |
| 27   | MOSI                  | I/O  | I       | SPI data input pin master out slave in (MOSI) or serial data (SDAT)   |
| 28   | MISO                  | I/O  | Z       | SPI data output pin - master in slave out (MISO), or GPIO (in SPI 3-pin mode). Tristates when SPI 3PIN = 0 and SS# is deasserted.   |
| 29   | XOUT                  | I/O  | O       | Buffered 0.75, 1.5, 3, 6, or 12 MHz clock, PACTL, or GPIO. Tristates in sleep mode (configure as GPIO drive LOW).   |
| 30   | PACTL                 | I/O  | O       | Control signal for external PA, T/R switch, or GPIO   |
| 33   | V <sub>IO</sub>       | Pwr  |         | I/O interface voltage, 1.8 V to 3.6 V   |
| 34   | RST                   | I    | I       | Device reset. Internal 10-kΩ pull-down resistor. Active HIGH, typically connect through a 0.47-μF capacitor to V <sub>BAT</sub> . Must have RST = 1 event the first time power is applied to the radio. Otherwise, the radio control register state is unknown. |

Not recommended for new designs

## Pin Description *(continued)*

### CYRF7936 40-Pin QFN

| Pin Number  | Name             | Type | Default | Description  |
|-------------|------------------|------|---------|--|
| 35          | V <sub>DD</sub>  | Pwr  |         | Decoupling pin for 1.8 V logic regulator, connect through a 0.47- $\mu$ F capacitor to GND.  |
| 37          | LVD              | O    |         | PMU inductor or diode connection, when used. If not used, connect to GND.  |
| 40          | V <sub>REG</sub> | Pwr  |         | PMU boosted output voltage feedback  |
| E-pad       | GND              | GND  |         | Must be soldered to ground   |
| Corner tabs | NC               | NC   |         | Do not solder the tabs and keep other signal traces clear. All tabs are common to the lead frame or paddle, which is grounded after the pad is grounded. While they are visible to the user, they do not extend to the bottom. |

## Functional Overview

The CYRF7936 IC is designed to implement wireless device links operating in the worldwide 2.4-GHz ISM frequency band. It is intended for systems compliant with worldwide regulations covered by ETSI EN 301 489-1 V1.41, ETSI EN 300 328-1 V1.3.1 (Europe), FCC CFR 47 Part 15 (USA and Industry Canada), and TELEC ARIB\_T66\_March, 2003 (Japan).

The CYRF7936 contains a 2.4-GHz CyFi radio modem, which features a 1-Mbps GFSK radio front-end, packet data buffering, packet framer, DSSS baseband controller, and RSSI. CYRF7936 features a SPI interface for data transfer and device configuration.

The CyFi radio modem supports 98 discrete 1-MHz channels (regulations may limit the use of some of these channels in certain jurisdictions).

The baseband performs DSSS spreading and despreading, start-of-packet (SOP), end-of-packet (EOP) detection, and CRC16 generation and checking. The baseband may also be configured to automatically transmit ACK handshake packets whenever a valid packet is received.

When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates. This enables the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems that use high data rates at shorter distances or in a low-moderate interference environment or both. It changes to lower data rates at longer distances or in high interference environments or both.

In addition, the CYRF7936 IC has a power management unit (PMU), which allows direct connection of the device to any battery voltage in the range 1.8 V to 3.6 V. The PMU conditions the battery voltage to provide the supply voltages required by the device, and may supply external devices.

### Data Transmission Modes

The CyFi radio transceiver supports two different data transmission modes:

- In GFSK mode, data is transmitted at 1 Mbps, without any DSSS.
- In 8DR mode, DSSS is enabled and eight bits are encoded in each derived code symbol transmitted.

Both 64 chip and 32 chip pseudo noise (PN) codes are supported in 8DR mode. In general, lower data rates reduce packet error rate in any given environment.

### Packet Framing

The CYRF7936 IC device supports the following data packet framing features:

#### SOP

Packets begin with a two-symbol SOP marker. The SOP\_CODE\_ADR PN code used for the SOP is different from that used for the “body” of the packet, and if necessary may be a different length. SOP must be configured to be the same length on both sides of the link.

#### Length

This is the first eight bits after the SOP symbol and is transmitted at the payload data rate. An EOP condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16.

#### CRC16

The device may be configured to append a 16-bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver verifies the calculated CRC16 for the payload data against the received value in the CRC16 field. The seed value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed. The received data CRC16 is checked against both the configured and zero CRC16 seeds.

CRC16 detects the following errors:

- Any one bit in error.
- Any two bits in error (irrespective of how far apart, which column, and so on).
- Any odd number of bits in error (irrespective of the location).
- An error burst as wide as the checksum itself.

Figure 2 shows an example packet with SOP, CRC16, and lengths fields enabled and Figure 3 shows a standard ACK packet.

Figure 2. Example Packet Format

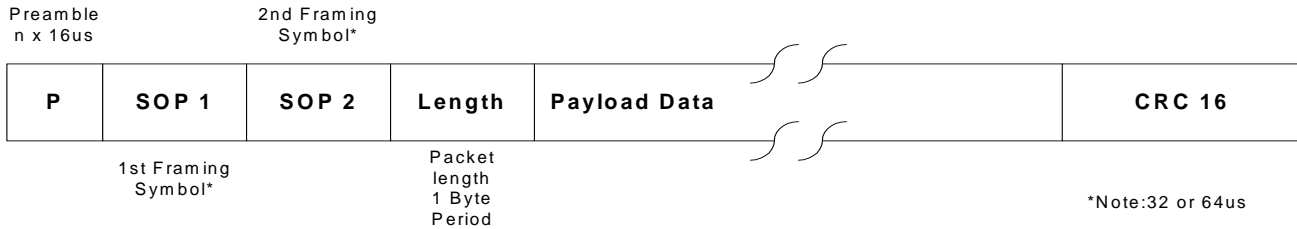
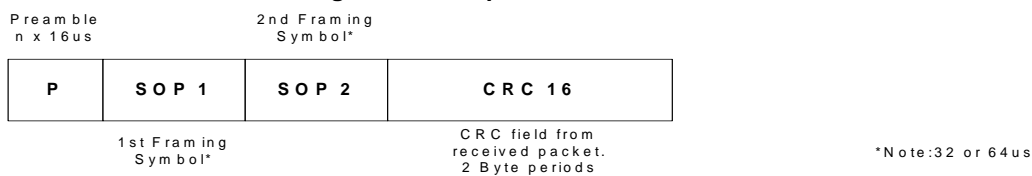


Figure 3. Example ACK Packet Format



### Packet Buffers

All data transmission and reception use the 16-byte packet buffers: one for transmission and one for reception.

The transmit buffer allows loading a complete packet of up to 16 bytes of payload data in one burst SPI transaction. This is then transmitted with no further MCU intervention. Similarly, the receive buffer allows receiving an entire packet of payload data up to 16 bytes with no firmware intervention required until the packet reception is complete.

Maximum packet length depends on the accuracy of the clock on each end of the link. Packet lengths up to 40 bytes are supported when the delta between the transmitter and receiver crystals is 60 ppm or better. Interrupts are provided to allow an MCU to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the MCU can load 16 bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the MCU must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

### Auto Transaction Sequencer (ATS)

The CYRF7936 IC provides automated support for transmission and reception of acknowledged data packets.

When transmitting in transaction mode, the device automatically:

- Starts the crystal and synthesizer
- Enters transmit mode
- Transmits the packet in the transmit buffer
- Transitions to receive mode and waits for an ACK packet
- Transitions to the transaction end state when an ACK packet is received or a timeout period expires

Similarly, when receiving in transaction mode, the device automatically:

- Waits in receive mode for a valid packet to be received
- Transitions to transmit mode, transmits an ACK packet
- Transitions to the transaction end state (receive mode to await the next packet, and so on.)

The contents of the packet buffers are not affected by the transmission or reception of ACK packets.

In each case, the entire packet transaction takes place without any need for MCU firmware action (as long as packets of 16 bytes or less are used). To transmit data, the MCU must load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware must retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

### Data Rates

The CYRF7936 IC supports the following data rates by combining the PN code lengths and data transmission modes described in the previous sections:

- 1000 kbps (GFSK)
- 250 kbps (32 chip 8DR)
- 125 kbps (64 chip 8DR)

Not recommended for new designs

## Functional Block Overview

### 2.4-GHz CyFi Radio Modem

The CyFi radio modem is a dual conversion low IF architecture optimized for power, range, and robustness. The CyFi radio modem employs channel-matched filters to achieve high performance in the presence of interference. An integrated power amplifier (PA) provides up to +4 dBm transmit power, with an output power control range of 34 dB in seven steps. The supply current of the device is reduced as the RF output power is reduced.

**Table 1. Internal PA Output Power Step Table**

| PA Setting | Typical Output Power (dBm) |
|------------|----------------------------|
| 7          | +4                         |
| 6          | 0                          |
| 5          | -5                         |
| 4          | -13                        |
| 3          | -18                        |
| 2          | -24                        |
| 1          | -30                        |
| 0          | -35                        |

### Frequency Synthesizer

Prior to transmission or reception, the frequency synthesizer must settle. The settling time varies depending on the channel; 25 fast channels are provided with a maximum settling time of 100  $\mu$ s.

The 'fast channels' (less than 100  $\mu$ s settling time) are every third channel, starting at 0 up to and including 72 (for example, 0, 3, 6, 9 .... 69, 72).

### Baseband and Framer

The baseband and framer blocks provide the DSSS encoding and decoding, SOP generation and reception, CRC16 generation and checking, and EOP detection and length field.

### Packet Buffers and Radio Configuration Registers

Packet data and configuration registers are accessed through the SPI interface. All configuration registers are directly addressed through the address field in the SPI packet. Configuration registers allow configuration of DSSS PN codes, data rate, operating mode, interrupt masks, interrupt status, and so on.

### SPI Interface

The CYRF7936 IC has an SPI interface supporting communication between an application MCU and one or more slave devices (including the CYRF7936). The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of slave select (SS#), serial clock (SCK), MOSI, MISO, or SDAT.

SPI communication is described as follows:

- Command direction (bit 7) = '1' enables SPI write transaction. When it equals a '0', it enables SPI read transactions.
- Command increment (bit 6) = '1' enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access. Otherwise the same address is accessed.
- Six bits of address
- Eight bits of data

The device receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active LOW SS# pin must be asserted to initiate an SPI transfer.

The application MCU can initiate SPI data transfers using a multibyte transaction. The first byte is the Command/Address byte and the following bytes are the data bytes as shown in Table 2 through Figure 6 on page 7.

The SPI communications interface has a burst mechanism, where the first byte can be followed by as many data bytes as required. A burst transaction is terminated by deasserting the slave select (SS# = 1).

The SPI communications interface single read and burst read sequences are shown in Figure 4 and Figure 5 on page 7, respectively.

The SPI communications interface single write and burst write sequences are shown in Figure 6 and Figure 7 on page 7, respectively.

This interface may be optionally operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT). When using the 3-pin mode, firmware must ensure that the MOSI pin on the MCU is in a high-impedance state except when MOSI is actively transmitting data.

The device registers may be written to or read from one byte at a time, or several sequential register locations may be written or read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files. Register files are FIFOs written to and read from using nonincrementing burst SPI transactions.

The IRQ pin function may be optionally multiplexed to the MOSI pin. When this option is enabled, the IRQ function is not available while the SS# pin is LOW. When using this configuration, firmware must ensure that the MOSI pin on the MCU is in a high impedance state whenever the SS# pin is HIGH.

The SPI interface is not dependent on the internal 12 MHz clock. Registers may therefore be read from or written to when the device is in sleep mode, and the 12 MHz oscillator disabled.

The SPI interface and the IRQ and RST pins have a separate voltage reference pin ( $V_{IO}$ ). This enables the device to interface directly to MCUs operating at voltages below the CYRF7936 IC supply voltage.

Not recommended for new designs

Table 2. SPI Transaction Format

| Parameter | Byte 1 |     |         | Byte 1+N |
|-----------|--------|-----|---------|----------|
| Bit #     | 7      | 6   | [5:0]   | [7:0]    |
| Bit Name  | DIR    | INC | Address | Data     |

Figure 4. SPI Single Read Sequence

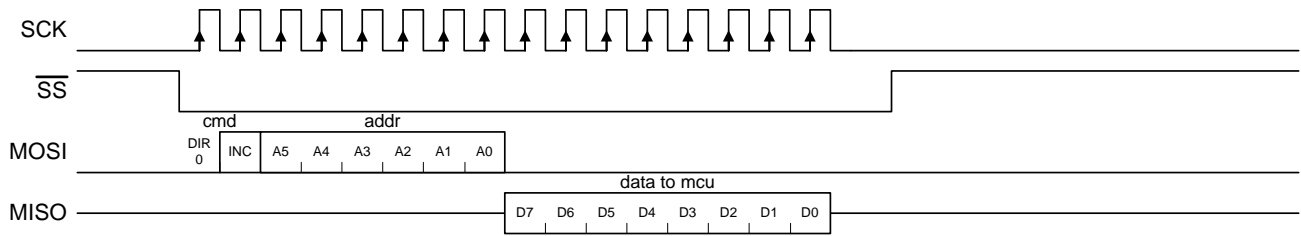


Figure 5. SPI Incrementing Burst Read Sequence

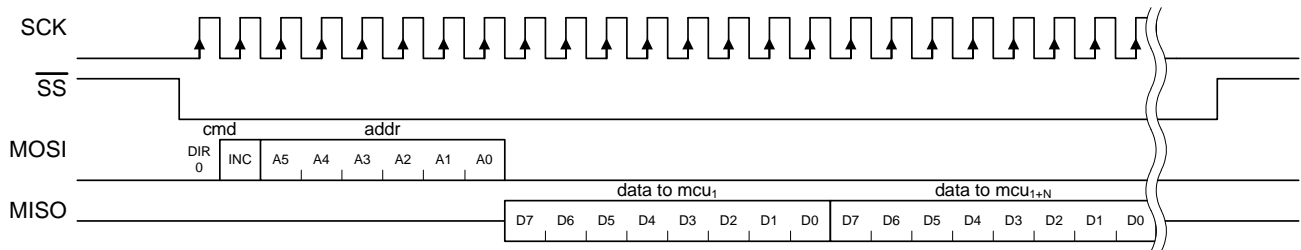


Figure 6. SPI Single Write Sequence

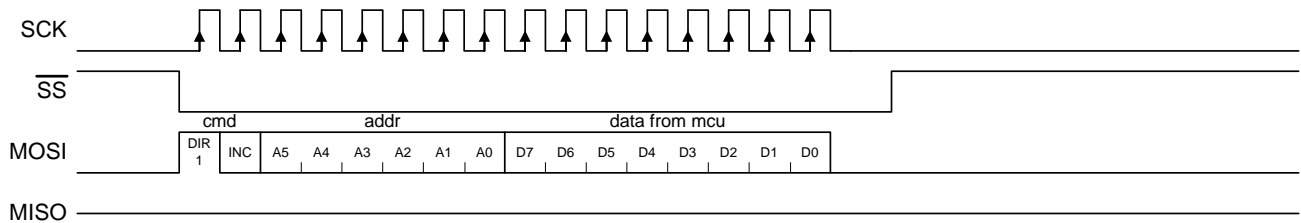
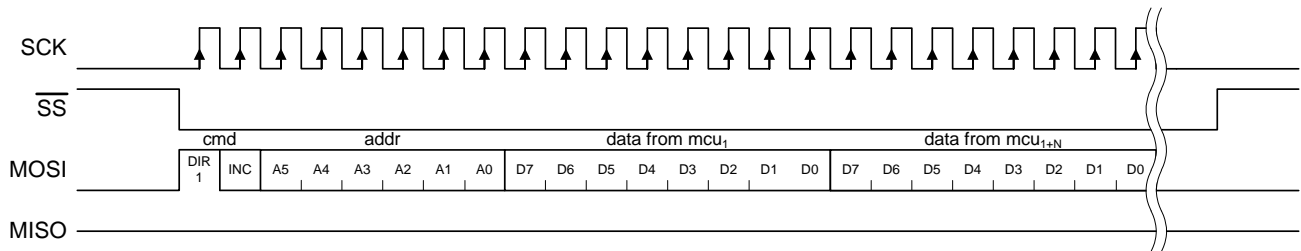


Figure 7. SPI Incrementing Burst Write Sequence



Not recommended for new designs

## Interrupts

The device provides an interrupt (IRQ) output, which is configurable to indicate the occurrence of different events. The IRQ pin can be programmed to be either active HIGH or active LOW; it can be a CMOS or open drain output.

The CYRF7936 IC features three sets of interrupts: transmit, receive, and system interrupts. These interrupts all share a single pin (IRQ), but can be independently enabled or disabled. The contents of the enable registers are preserved when switching between transmit and receive modes.

If more than one interrupt is enabled at any time, it is necessary to read the relevant status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that otherwise causes an interrupt can be determined by reading the appropriate status register. It is therefore possible to use devices without the IRQ pin, by polling the status registers to wait for an event, rather than using the IRQ pin.

## Clocks

A 12-MHz crystal (30 ppm or better) is directly connected between XTAL and GND without the need for external capacitors. A digital clock out function is provided, with selectable output frequencies of 0.75, 1.5, 3, 6, or 12 MHz. This output may be used to clock an external microcontroller (MCU) or ASIC. This output is enabled by default, but may be disabled.

The requirements to directly connect the crystal to the XTAL pin and GND are:

- Nominal frequency: 12 MHz
- Operating mode: Fundamental mode
- Resonance mode: Parallel resonant
- Frequency stability:  $\pm 30$  ppm
- Series resistance:  $\leq 60 \Omega$
- Load capacitance: 10 pF
- Drive level: 100  $\mu$ W

## Power Management

The operating voltage of the device is 1.8 V to 3.6 V DC, which is applied to the  $V_{BAT}$  pin. The device can be shut down to a fully static sleep mode by writing to the FRC END = 1 and END STATE = 000 bits in the XACT\_CFG\_ADR register over the SPI interface. The device enters sleep mode within 35  $\mu$ s after the last SCK positive edge at the end of this SPI transaction. Alternatively, the device may be configured to automatically enter sleep mode after completing the packet transmission or reception. When in sleep mode, the on-chip oscillator is stopped, but the SPI interface remains functional. The device wakes from sleep mode automatically when the device is commanded to enter transmit or receive mode. When resuming from sleep mode, there is a short delay while the oscillator restarts. The device can be configured to assert the IRQ pin when the oscillator has stabilized.

The output voltage ( $V_{REG}$ ) of the PMU is configurable to several minimum values between 2.4 V and 2.7 V.  $V_{REG}$  may be used to provide up to 15 mA (average load) to external devices. It is possible to disable the PMU and provide an externally regulated DC supply voltage to the device's main supply in the range 2.4 V to 3.6 V. The PMU also provides a regulated 1.8 V supply to the logic.

The PMU is designed to provide high boost efficiency (74%–85% depending on input voltage, output voltage, and load) when using a Schottky diode and power inductor. This eliminates the need for an external boost converter in many systems where other components require a boosted voltage. However, reasonable efficiencies (69%–82% depending on input voltage, output voltage, and load) can be achieved when using low cost components such as SOT23 diodes and 0805 inductors.

The current through the diode must stay within the linear operating range of the diode. For some loads the SOT23 diode is sufficient, but with higher loads it is not; a SS12 diode must be used to stay within this linear range of operation. Along with the diode, the inductor used must not saturate its core. In higher loads, a lower resistance/higher saturation coil such as the inductor from Sumida must be used.

The PMU also provides a configurable low battery detection function, which can be read over the SPI interface. One of seven thresholds between 1.8 V and 2.7 V can be selected. The interrupt pin can be configured to assert when the voltage on the  $V_{BAT}$  pin falls below the configured threshold. LV IRQ is not a latched event. Battery monitoring is disabled when the device is in sleep mode.

## Receiver Front End

The gain of the receiver can be controlled directly by writing to the low-noise amplifier (LNA) bit and the attenuation (ATT) bit of the RX\_CFG\_ADR register. Clearing the LNA bit reduces the receiver gain approximately 20 dB, allowing accurate reception of very strong received signals (for example, when operating a receiver very close to the transmitter). Approximately 30 dB of receiver attenuation can be added by setting the ATT bit. This limits data reception to devices at very short ranges. Enabling LNA is recommended, unless receiving from a device using external PA.

When the device is in receive mode, the RSSI\_ADR register returns the relative signal strength of the on-channel signal power.

When receiving, the device automatically measures and stores the relative strength of the signal being received as a five bit value. An RSSI reading is taken automatically when the SOP is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI\_ADR register. This allows the background RF energy level on any given channel to be easily measured when RSSI is read while no signal is being received. A new reading can occur as fast as once every 12  $\mu$ s.

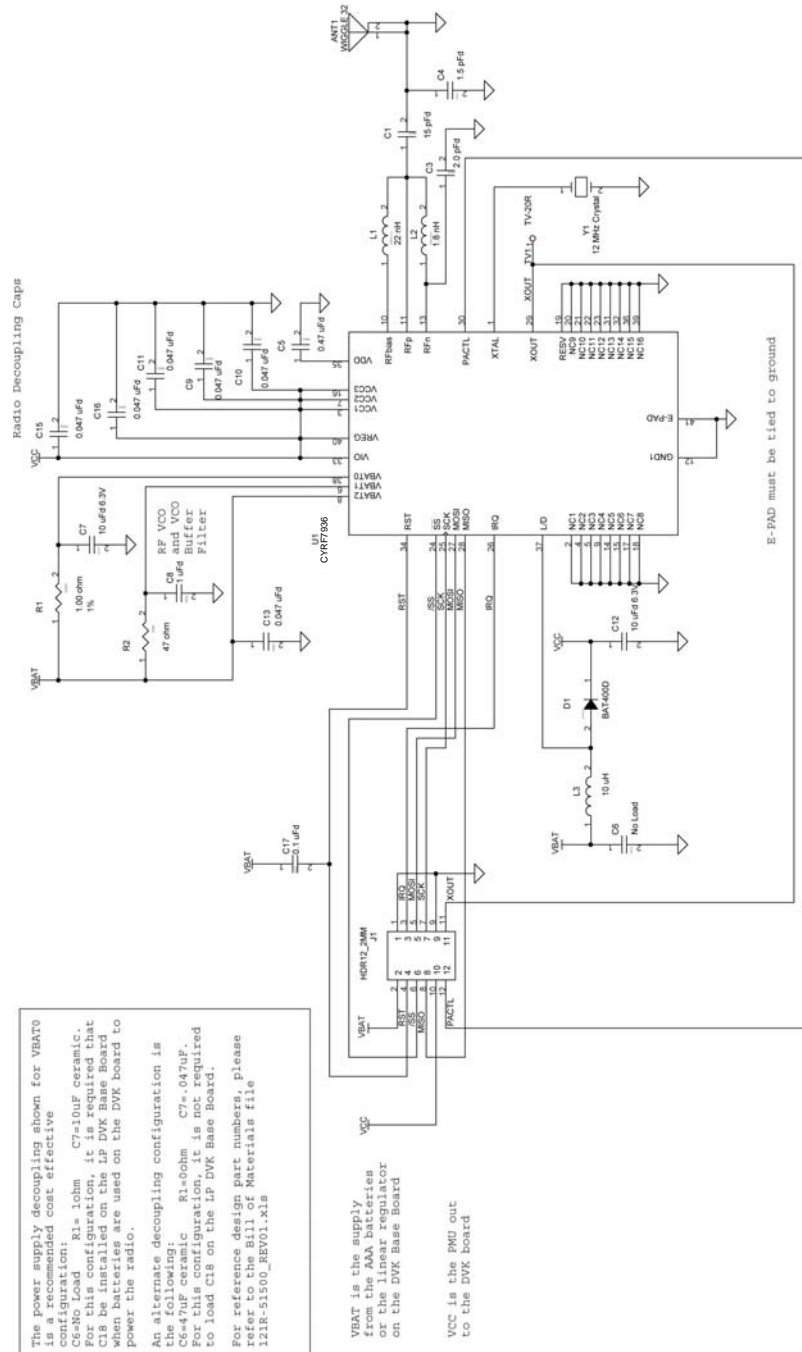
### Receive Spurious Response

The transmitter may exhibit spurs around 50MHz offset at levels approximately 50dB to 60dB below the carrier power. Receivers operating at the transmit spur frequency may receive the spur if the spur level power is greater than the receive sensitivity level.

The workaround for this is to program an additional byte in the packet header which contains the transmitter channel number. After the packet is received, the channel number can be checked. If the channel number does not match the receive channel then the packet is rejected.

### Application Examples

Figure 8. Recommended Circuit for Systems where  $V_{BAT} \leq 2.4 V$



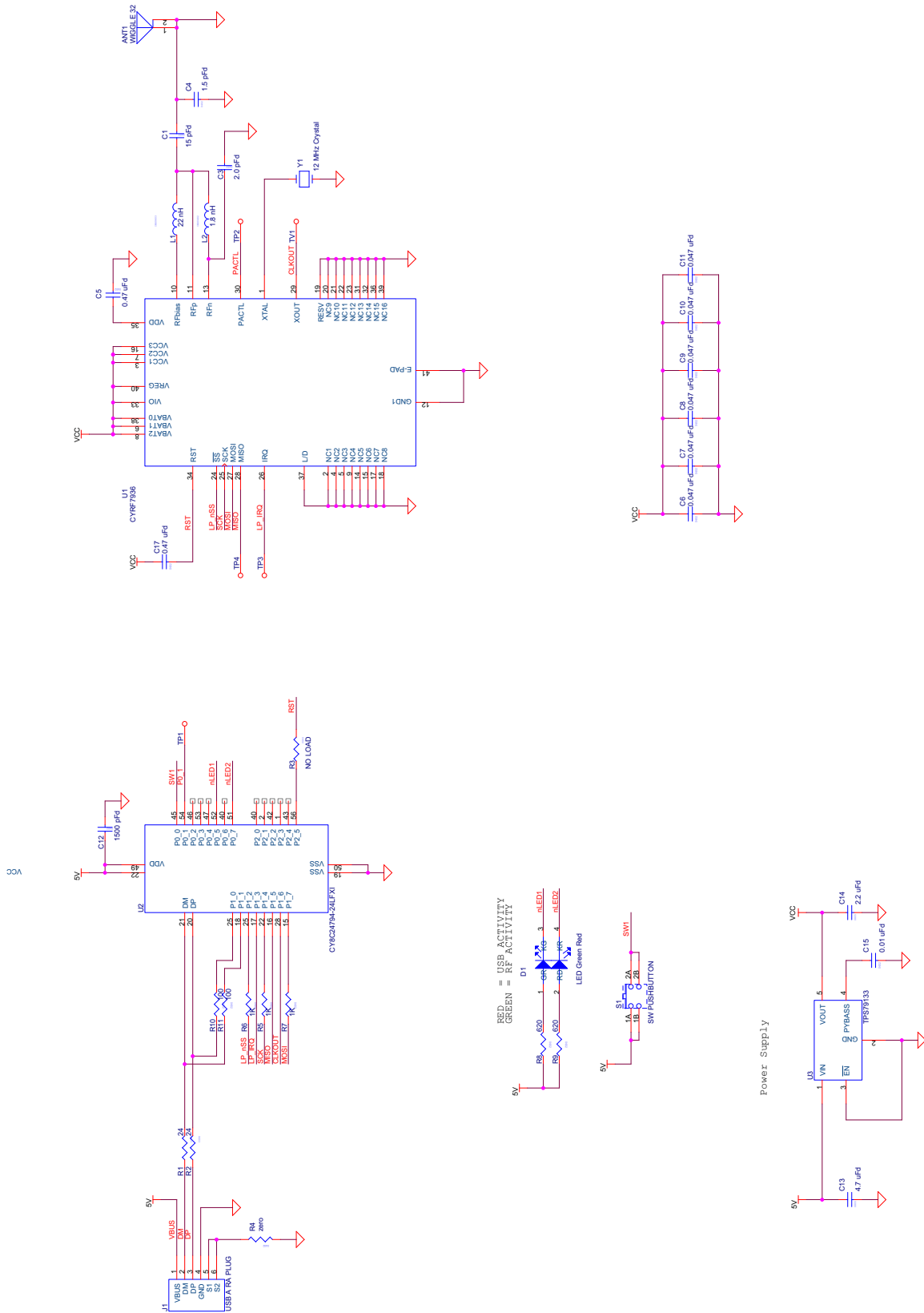
Not recommended for new designs

**Table 3. Recommended BoM for Systems where  $V_{BAT} \leq 2.4 V$** 

| Item | Qty | CY Part Number  | Reference               | Description                                  | Manufacturer             | Mfr Part Number     |
|------|-----|-----------------|-------------------------|--|--------------------------|---------------------|
| 1    | 1   | NA              | ANT1                    | 2.5 GHz H-STUB Wiggle Antenna for 32 MIL PCB | NA                       | NA                  |
| 2    | 1   | 730-10012       | C1                      | CAP 15 PF 50 V CERAMIC NPO 0402              | Panasonic                | ECJ-0EC1H150J       |
| 3    | 1   | 730-11955       | C3                      | CAP 2.0 PF 50 V CERAMIC NPO 0402             | Kemet                    | C0402C209C5GACTU    |
| 4    | 1   | 730-11398       | C4                      | CAP 1.5PF 50 V CERAMIC NPO 0402 SMD          | PANASONIC                | ECJ-0EC1H1R5C       |
| 5    | 1   | 730R-13322      | C5                      | CAP CER.47 uF 6.3 V X5R 0402                 | Murata                   | GRM155R60J474KE1 9D |
| 6    | 2   | 730-13037       | C12,C7                  | CAP CERAMIC 10 uF 6.3 V X5R 0805             | Kemet                    | C0805C106K9PACTU    |
| 7    | 1   | 730-13400       | C8                      | CAP 1 uF 6.3 V CERAMIC X5R 0402              | Panasonic                | ECJ-0EB0J105M       |
| 8    | 6   | 730-13404       | C9,C10,C11, C13,C15,C16 | CAP 0.047 uF 50 V CERAMIC X5R 0402           | AVX                      | 0402YD473KAT2A      |
| 9    | 1   | 730R-11952      | C17                     | CAP.10UF 10 V CERAMIC X5R 0402               | Kemet                    | C0402C104K8PACTU    |
| 10   | 1   | 800-13317       | D1                      | Diode Schottky 0.5A 40 V SOT23               | DIODES INC               | BAT400D-7-F         |
| 11   | 1   | 420-11976       | J1                      | CONN HEADER 12 PIN 2MM GOLD                  | Hirose Electric Co. Ltd. | DF11-12DP-2DSA(01)  |
| 12   | 1   | 800-13401       | L1                      | INDUCTOR 22NH 2% FIXED 0603 SMD              | Panasonic - ECG          | ELJ-RE22NGF2        |
| 13   | 1   | 800-11651       | L2                      | INDUCTOR 1.8NH +/- .3NH FIXED 0402 SMD       | Panasonic - ECG          | ELJ-RF1N8DF         |
| 14   | 1   | 800-10594       | L3                      | COIL 10UH 1100MA CHOKE 0805                  | Newark                   | 30K5421             |
| 15   | 1   | 630-11356       | R1                      | RES 1.00 OHM 1/8W 1% 0805 SMD                | Yageo                    | 9C08052A1R00FKHFT   |
| 16   | 1   | 610-13402       | R2                      | RES 47 OHM 1/16W 5% 0402 SMD                 | Panasonic - ECG          | ERJ-2GEJ470X        |
| 17   | 1   | CYRF7936-40LFXC | U1                      | IC, LP 2.4 GHz Radio SoC QFN-40              | Cypress Semiconductor    | CYRF7936-40LFXC     |
| 18   | 1   | 800-13259       | Y1                      | Crystal 12.00 MHZ HC49 SMD                   | eCERA                    | GF-1200008          |
| 19   | 1   | PDCR-9515 REV01 | PCB                     | Printed Circuit Board                        | Cypress Semiconductor    | PDCR-9515 REV01     |
| 20   | 1   | 920-11206       | LABEL1                  | Serial Number                                |                          |                     |
| 21   | 1   | 920-51500 REV01 | LABEL2                  | PCA #  |                          | 121R-51500 REV01    |

Not recommended for new designs

Figure 9. Recommended Circuit for Systems where  $V_{BAT}$  is 2.4 V to 3.6 V (PMU Disabled)



Not recommended for new designs

Table 4. Recommended BoM for Systems where V<sub>BAT</sub> is 2.4 V - 3.6 V (PMU disabled)

| Item | Qty | CY Part Number   | Reference            | Description                                 | Manufacturer                     | Mfr Part Number    |
|------|-----|------------------|----------------------|---|----------------------------------|--------------------|
| 1    | 1   | NA               | ANT1                 | 2.5 GHz H-STUB Wiggle Antenna for 32MIL PCB | NA                               | NA                 |
| 2    | 1   | 730-10012        | C1                   | CAP 15 PF 50 V CERAMIC NPO 0402             | Panasonic                        | ECJ-0EC1H150J      |
| 3    | 1   | 730-11955        | C3                   | CAP 2.0 PF 50 V CERAMIC NPO 0402            | Kemet                            | C0402C209C5GACTU   |
| 4    | 1   | 730-11398        | C4                   | CAP 1.5 PF 50 V CERAMIC NPO 0402 SMD        | PANASONIC                        | ECJ-0EC1H1R5C      |
| 5    | 1   | 730-13322        | C5                   | CAP 0.47 uF 6.3 V CERAMIC X5R 0402          | Murata                           | GRM155R60J474KE19D |
| 6    | 6   | 730-13404        | C6,C7,C8,C9,C10, C11 | CAP 0.047 uF 16 V CERAMIC X5R 0402          | AVX                              | 0402YD473KAT2A     |
| 7    | 1   | 730-11953        | C12                  | CAP 1500PF 50V CERAMIC X7R 0402             | Kemet                            | C0402C152K5RACTU   |
| 8    | 1   | 730-13040        | C13                  | CAP CERAMIC 4.7UF 6.3V XR5 0805             | Kemet                            | C0805C475K9PACTU   |
| 9    | 1   | 730-12003        | C14                  | CAP CER 2.2 uF 10 V 10% X7R 0805            | Murata Electronics North America | GRM21BR71A225KA01L |
| 10   | 1   | 800-13333        | D1                   | LED GREEN/RED BICOLOR 1210 SMD              | LITEON                           | LTST-C155KGJRKT    |
| 11   | 1   | 420-13046        | J1                   | CONN USB PLUG TYPE A PCB SMT                | ACON                             | UAR72-4N5J10       |
| 12   | 1   | 800-13401        | L1                   | INDUCTOR 22NH 2% FIXED 0603 SMD             | Panasonic - ECG                  | ELJ-RE22NGF2       |
| 13   | 1   | 800-11651        | L2                   | INDUCTOR 1.8NH +/- .3NH FIXED 0402 SMD      | Panasonic - ECG                  | ELJ-RF1N8DF        |
| 14   | 2   | 610-10037        | R1, R2               | RES 24 OHM 1/16W 5% 0603 SMD                | Panasonic - ECG                  | ERJ-3GEYJ240V      |
| 15   | 1   | 610-10343        | R4                   | RES ZERO OHM 1/16W 0402 SMD                 | Panasonic - ECG                  | ERJ-2GE0R00X       |
| 16   | 3   | 610-10016        | R5, R6, R7           | RES CHIP 1K OHM 1/16W 5% 0402 SMD           | Panasonic - ECG                  | ERJ-2GEJ102X       |
| 17   | 2   | 610-13472        | R9,R8                | RES CHIP 620 OHM 1/16W 5% 0402 SMD          | Panasonic - ECG                  | ERJ-2GEJ621X       |
| 18   | 2   | 610-10684        | R10, R11             | RES CHIP 100 OHM 1/16W 5% 0402 SMD          | Phycomp USA Inc                  | 9C1A04021000FLHF3  |
| 19   | 1   | 200-13471        | S1                   | SWITCH LT 3.5MMX2.9MM 160GF SMD             | Panasonic - ECG                  | EVQ-P7J01K         |
| 20   | 1   | CYRF7936-40LFC   | U1                   | IC, 2.4 GHz CyFi Transceiver QFN-40         | Cypress Semiconductor            | CYRF7936 Rev A5    |
| 21   | 1   | CY8C24794-24LFXI | U2                   | PSoC Mixed Signal Array                     | Cypress Semiconductor            | CY8C24794-24LFXI   |
| 22   | 1   | 800-13259        | Y1                   | Crystal 12.00 MHZ HC49 SMD                  | eCERA                            | GF-1200008         |
| 23   | 1   |                  | LABEL1               | Serial Number                               | XXXXXX                           |                    |

Not recommended for new designs

### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied . -55 °C to +125 °C
- Supply voltage on any power supply pin relative to  $V_{SS}$  ..... -0.3 V to +3.9 V
- DC voltage to logic inputs<sup>[8]</sup> ..... -0.3 V to  $V_{IO} + 0.3$  V
- DC voltage applied to outputs in high-Z state ..... -0.3 V to  $V_{IO} + 0.3$  V

- Static discharge voltage (digital)<sup>[9]</sup> ..... >2000 V
- Static discharge voltage (RF)<sup>[9]</sup> ..... 1100 V
- Latch-up current ..... +200 mA, -200 mA

### Operating Conditions

- $V_{CC}$  ..... 2.4 V to 3.6 V
- $V_{IO}$  ..... 1.8 V to 3.6 V
- $V_{BAT}$  ..... 1.8 V to 3.6 V
- $T_A$  (ambient temperature under bias) ..... 0 °C to +70 °C
- Ground voltage ..... 0 V
- $f_{OSC}$  (crystal frequency) ..... 12 MHz  $\pm$ 30 ppm b

### DC Characteristics

(T = 25 °C,  $V_{BAT}$  = 2.4 V, PMU disabled,  $f_{OSC}$  = 12.000000 MHz)

| Parameter                | Description                                  | Conditions   | Min                 | Typ      | Max         | Unit    |
|--------------------------|--|--|---------------------|----------|-------------|---------|
| $V_{BAT}$                | Battery voltage                              | 0 °C to 70 °C  | 1.8                 | -        | 3.6         | V       |
| $V_{REG}^{[10]}$         | PMU output voltage                           | 2.4 V mode   | 2.4                 | 2.43     | -           | V       |
| $V_{REG}^{[10]}$         | PMU output voltage                           | 2.7 V mode   | 2.7                 | 2.73     | -           | V       |
| $V_{IO}^{[11]}$          | $V_{IO}$ voltage                             |  | 1.8                 | -        | 3.6         | V       |
| $V_{CC}$                 | $V_{CC}$ voltage                             | 0 °C to 70 °C  | 2.4 <sup>[12]</sup> | -        | 3.6         | V       |
| $V_{OH1}$                | Output high voltage condition 1              | At $I_{OH} = -100.0 \mu A$                                     | $V_{IO} - 0.2$      | $V_{IO}$ | -           | V       |
| $V_{OH2}$                | Output high voltage condition 2              | At $I_{OH} = -2.0 mA$  | $V_{IO} - 0.4$      | $V_{IO}$ | -           | V       |
| $V_{OL}$                 | Output low voltage                           | At $I_{OL} = 2.0 mA$   | -                   | 0        | 0.45        | V       |
| $V_{IH}$                 | Input high voltage                           |  | $0.7V_{IO}$         | -        | $V_{IO}$    | V       |
| $V_{IL}$                 | Input low voltage                            |  | 0                   | -        | $0.3V_{IO}$ | V       |
| $I_{IL}$                 | Input leakage current                        | $0 < V_{IN} < V_{IO}$  | -1                  | 0.26     | +1          | $\mu A$ |
| $C_{IN}$                 | Pin input capacitance                        | Except XTAL, $RF_N$ , $RF_P$ , $RF_{BIAS}$                     | -                   | 3.5      | 10          | pF      |
| $I_{CC} (GFSK)^{[13]}$   | Average TX $I_{CC}$ , 1 Mbps, slow channel   | PA = 5, 2 way, 4 bytes/10 ms                                   | -                   | 0.87     | -           | mA      |
| $I_{CC} (32-8DR)^{[13]}$ | Average TX $I_{CC}$ , 250 kbps, fast channel | PA = 5, 2 way, 4 bytes/10 ms                                   | -                   | 1.2      | -           | mA      |
| $I_{SB}^{[14]}$          | Sleep mode $I_{CC}$                          |  | -                   | 0.8      | 10          | $\mu A$ |
| $I_{SB}^{[14]}$          | Sleep mode $I_{CC}$                          | PMU enabled  | -                   | 31.4     | -           | $\mu A$ |
| IDLE $I_{CC}$            | Radio off, XTAL Active                       | XOUT disabled  | -                   | 1.0      | -           | mA      |
| $I_{synth}$              | $I_{CC}$ during synth start                  |  | -                   | 8.4      | -           | mA      |
| TX $I_{CC}$              | $I_{CC}$ during transmit                     | PA = 5 (-5 dBm)  | -                   | 20.8     | -           | mA      |
| TX $I_{CC}$              | $I_{CC}$ during transmit                     | PA = 6 (0 dBm)   | -                   | 26.2     | -           | mA      |
| TX $I_{CC}$              | $I_{CC}$ during transmit                     | PA = 7 (+4 dBm)  | -                   | 34.1     | -           | mA      |
| RX $I_{CC}$              | $I_{CC}$ during receive                      | LNA off, ATT on  | -                   | 18.4     | -           | mA      |
| RX $I_{CC}$              | $I_{CC}$ during receive                      | LNA on, ATT off  | -                   | 21.2     | -           | mA      |
| Boost Eff                | PMU boost converter efficiency               | $V_{BAT} = 2.5 V$ , $V_{REG} = 2.73 V$ ,<br>$I_{LOAD} = 20 mA$ | -                   | 81       | -           | %       |
| $I_{LOAD\_EXT}^{[15]}$   | Average PMU external load current            | $V_{BAT} = 1.8 V$ , $V_{REG} = 2.73 V$ ,<br>0-50 °C, RX mode   | -                   | -        | 15          | mA      |
| $I_{LOAD\_EXT}^{[15]}$   | Average PMU external load current            | $V_{BAT} = 1.8V$ , $V_{REG} = 2.73V$ , 50 °C-70 °C,<br>RX mode | -                   | -        | 10          | mA      |

#### Notes

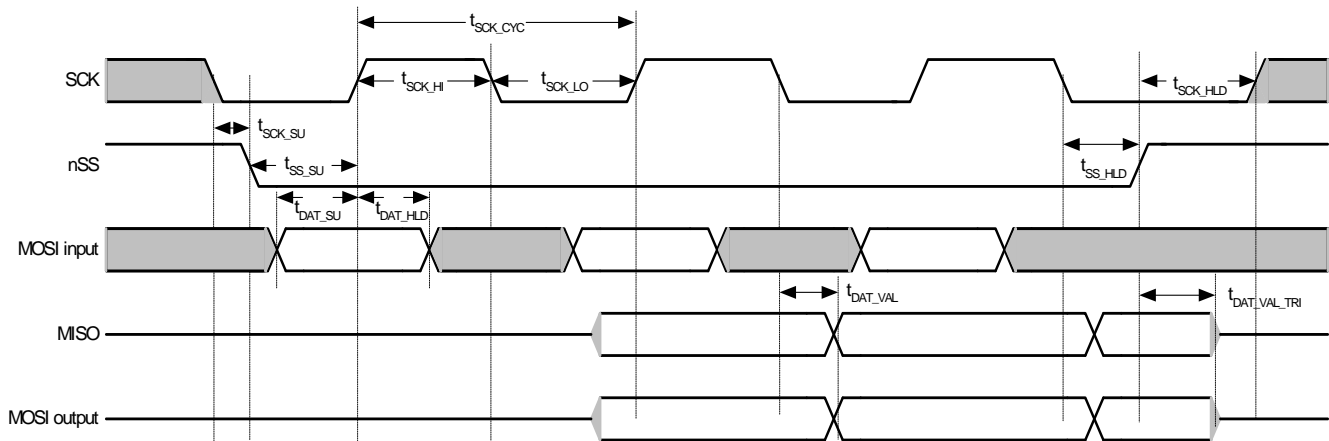
8. It is permissible to connect voltages above  $V_{IO}$  to inputs through a series resistor limiting input current to 1 mA. AC timing not guaranteed.
9. Human body model (HBM).
10.  $V_{REG}$  depends on battery input voltage.
11. In sleep mode, the I/O interface voltage reference is  $V_{BAT}$ .
12. In sleep mode,  $V_{CC}$  min. can be as low as 1.8 V.
13. Includes current drawn while starting crystal, starting synthesizer, transmitting packet (including SOP and CRC16), changing to receive mode, and receiving ACK handshake. Device is in sleep except during this transaction.
14. ISB is not guaranteed if any I/O pin is connected to voltages higher than  $V_{IO}$ .
15.  $I_{LOAD\_EXT}$  is dependant on external components and this entry applies when the components connected to L/D are SS12 series diode and DH53100LC inductor from Sumida.

## AC Characteristics

Table 5. SPI Interface<sup>[16, 17]</sup>

| Parameter                | Description   | Min   | Typ | Max | Unit |
|--------------------------|---|-------|-----|-----|------|
| t <sub>SCK_CYC</sub>     | SPI clock period  | 238.1 | –   | –   | ns   |
| t <sub>SCK_HI</sub>      | SPI clock high time   | 100   | –   | –   | ns   |
| t <sub>SCK_LO</sub>      | SPI clock low time  | 100   | –   | –   | ns   |
| t <sub>DAT_SU</sub>      | SPI input data setup time   | 25    | –   | –   | ns   |
| t <sub>DAT_HLD</sub>     | SPI input data hold time  | 10    | –   | –   | ns   |
| t <sub>DAT_VAL</sub>     | SPI output data valid time  | 0     | –   | 50  | ns   |
| t <sub>DAT_VAL_TRI</sub> | SPI output data tristate (MOSI from slave select deassert)                    |       | –   | 20  | ns   |
| t <sub>SS_SU</sub>       | SPI slave select setup time before first positive edge of SCK <sup>[18]</sup> | 10    | –   | –   | ns   |
| t <sub>SS_HLD</sub>      | SPI slave select hold time after last negative edge of SCK                    | 10    | –   | –   | ns   |
| t <sub>SS_PW</sub>       | SPI slave select minimum pulse width  | 20    | –   | –   | ns   |
| t <sub>SCK_SU</sub>      | SPI slave select setup time   | 10    | –   | –   | ns   |
| t <sub>SCK_HLD</sub>     | SPI SCK hold time   | 10    | –   | –   | ns   |
| t <sub>RESET</sub>       | Minimum RST pin pulse width   | 10    | –   | –   | ns   |

Figure 10. SPI Timing



**Notes**

- 16. AC values are not guaranteed if voltage on any pin exceeding V<sub>IO</sub>.
- 17. C<sub>LOAD</sub> = 30 pF
- 18. SCK must start low at the time SS# goes LOW, otherwise the success of SPI transactions are not guaranteed.

## RF Characteristics

**Table 6. Radio Parameters**

| Parameter Description  | Conditions                  | Min   | Typ   | Max   | Unit     |
|--|-----------------------------|-------|-------|-------|----------|
| RF frequency range   | Refer Note 19               | 2.400 | –     | 2.497 | GHz      |
| <b>Receiver</b> (T = 25 °C, V <sub>CC</sub> = 3.0 V, f <sub>OSC</sub> = 12.000000 MHz, BER < 1E-3) |                             |       |       |       |          |
| Sensitivity 125 kbps 64-8DR  | BER 1E-3                    |       | –97   | –     | dBm      |
| Sensitivity 250 kbps 32-8DR  | BER 1E-3                    |       | –93   | –     | dBm      |
| Sensitivity  | CER 1E-3                    | –80   | –87   | –     | dBm      |
| Sensitivity GFSK   | BER 1E-3, ALL SLOW = 1      |       | –84   | –     | dBm      |
| LNA gain   |                             | –     | 22.8  | –     | dB       |
| ATT gain   |                             | –     | –31.7 | –     | dB       |
| Maximum received signal  | LNA On                      | –15   | –6    | –     | dBm      |
| RSSI value for PWR <sub>in</sub> –60 dBm <sup>[20]</sup>   | LNA On                      |       | 21    | –     | Count    |
| RSSI slope   |                             |       | 1.9   | –     | dB/Count |
| <b>Interference Performance</b> (CER 1E-3)   |                             |       |       |       |          |
| Co-channel Interference rejection carrier-to-Interference (C/I)                                    | C = –60 dBm                 | –     | 9     | –     | dB       |
| Adjacent (±1 MHz) channel selectivity C/I 1 MHz  | C = –60 dBm                 | –     | 3     | –     | dB       |
| Adjacent (±2 MHz) channel selectivity C/I 2 MHz  | C = –60 dBm                 | –     | –30   | –     | dB       |
| Adjacent (≥ 3 MHz) channel selectivity C/I ≥ 3 MHz   | C = –67 dBm                 | –     | –38   | –     | dB       |
| Out-of-band blocking 30 MHz–12.75 MHz <sup>[21]</sup>  | C = –67 dBm                 | –     | –30   | –     | dBm      |
| Intermodulation  | C = –64 dBm, Δf = 5, 10 MHz | –     | –36   | –     | dBm      |
| <b>Receive Spurious Emission</b>   |                             |       |       |       |          |
| 800 MHz  | 100 kHz ResBW               | –     | –79   | –     | dBm      |
| 1.6 GHz  | 100 kHz ResBW               | –     | –71   | –     | dBm      |
| 3.2 GHz  | 100 kHz ResBW               | –     | –65   | –     | dBm      |
| <b>Transmitter</b> (T = 25°C, V <sub>CC</sub> = 3.0 V)   |                             |       |       |       |          |
| Maximum RF transmit power  | PA = 7                      | +2    | 4     | +6    | dBm      |
| Maximum RF transmit power  | PA = 6                      | –2    | 0     | +2    | dBm      |
| Maximum RF transmit power  | PA = 5                      | –7    | –5    | –3    | dBm      |
| Maximum RF transmit power  | PA = 0                      | –     | –35   | –     | dBm      |
| RF power control range   |                             | –     | 39    | –     | dB       |
| RF power range control step size   | Seven steps, monotonic      | –     | 5.6   | –     | dB       |
| Frequency deviation min  | PN code pattern 10101010    | –     | 270   | –     | kHz      |
| Frequency deviation max  | PN code pattern 11110000    | –     | 323   | –     | kHz      |
| Error vector magnitude (FSK error)   | >0 dBm                      | –     | 10    | –     | %rms     |
| Occupied bandwidth   | –6 dBc, 100 kHz ResBW       | 500   | 876   | –     | kHz      |
| <b>Transmit Spurious Emission</b> (PA = 7)   |                             |       |       |       |          |
| In-band spurious second channel power (±2 MHz)   |                             | –     | –38   | –     | dBm      |
| In-band spurious third channel power (≥3 MHz)  |                             | –     | –44   | –     | dBm      |

**Notes**

19. Subject to regulation.  
 20. RSSI value is not guaranteed. Extensive variation from part to part.  
 21. Exceptions F/3 and 5C/3.

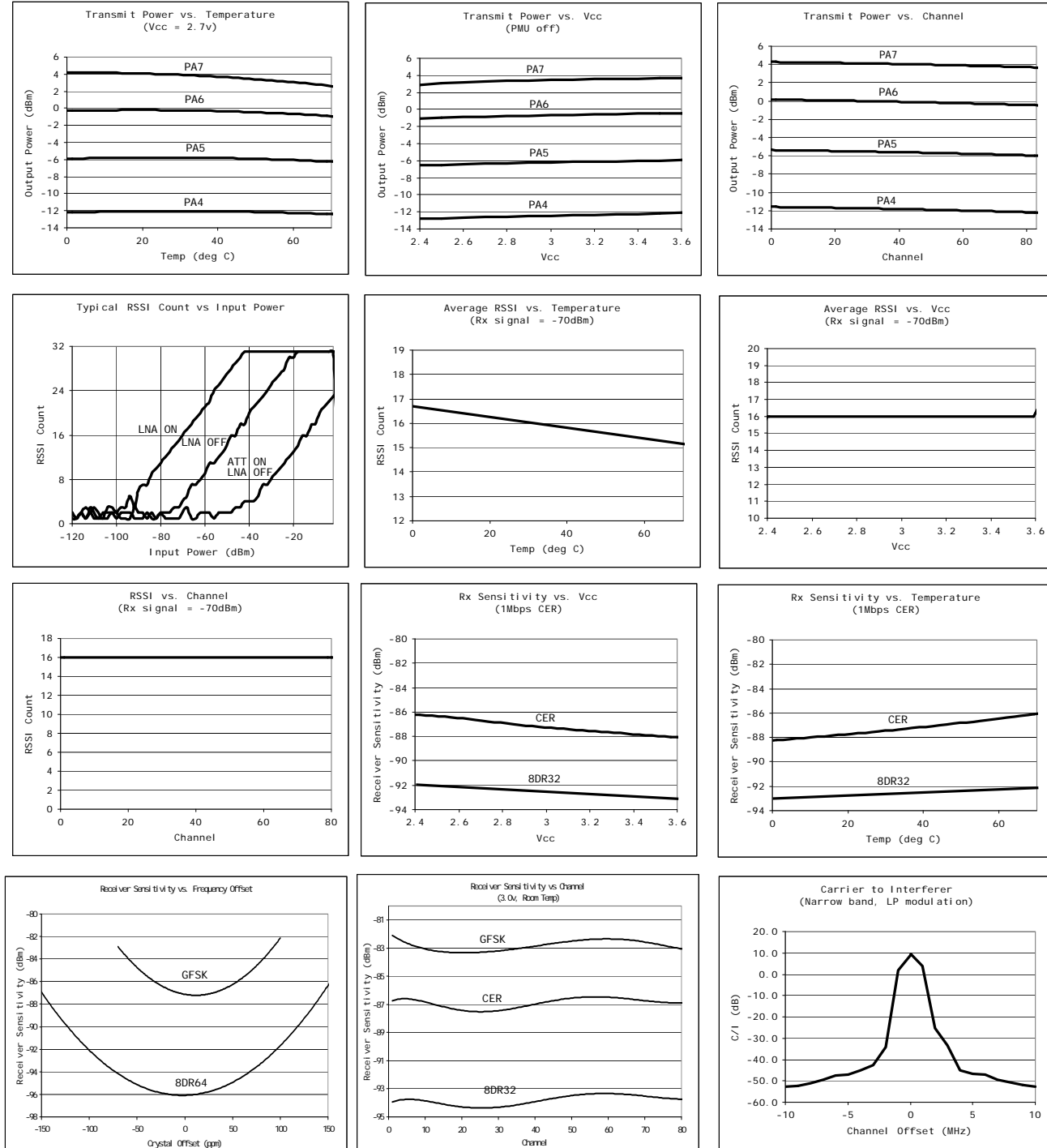
Table 6. Radio Parameters (continued)

| Parameter Description                                  | Conditions                 | Min | Typ | Max | Unit  |
|--|----------------------------|-----|-----|-----|-------|
| Non harmonically related spurs (800 MHz)               |                            | –   | –38 | –   | dBm   |
| Non harmonically related spurs (1.6 GHz)               |                            | –   | –34 | –   | dBm   |
| Non harmonically related spurs (3.2 GHz)               |                            | –   | –47 | –   | dBm   |
| Harmonic spurs (second harmonic)                       |                            | –   | –43 | –   | dBm   |
| Harmonic spurs (third harmonic)                        |                            | –   | –48 | –   | dBm   |
| Fourth and greater harmonics                           |                            | –   | –59 | –   | dBm   |
| <b>Power Management</b> (Crystal PN# eCERA GF-1200008) |                            |     |     |     |       |
| Crystal start to 10 ppm                                |                            | –   | 0.7 | 1.3 | ms    |
| Crystal start to IRQ                                   | XSIRQ EN = 1               | –   | 0.6 | –   | ms    |
| Synth settle   | Slow channels              | –   | –   | 270 | µs    |
| Synth settle   | Medium channels            | –   | –   | 180 | µs    |
| Synth settle   | Fast channels              | –   | –   | 100 | µs    |
| Link turnaround time                                   | GFSK                       | –   | –   | 30  | µs    |
| Link turnaround time                                   | 250 kbps                   | –   | –   | 62  | µs    |
| Link turnaround time                                   | 125 kbps                   | –   | –   | 94  | µs    |
| Link turnaround time                                   | <125 kbps                  | –   | –   | 31  | µs    |
| Maximum packet length                                  | <60 ppm crystal-to-crystal | –   | –   | 40  | bytes |

Not recommended for new designs

## Typical Operating Characteristics

The typical operating characteristics of CYRF7936 follow<sup>[22]</sup>

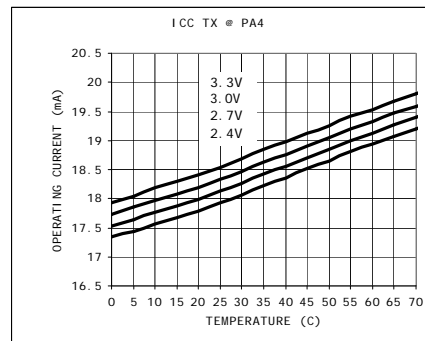
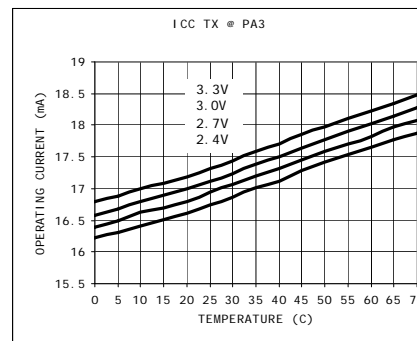
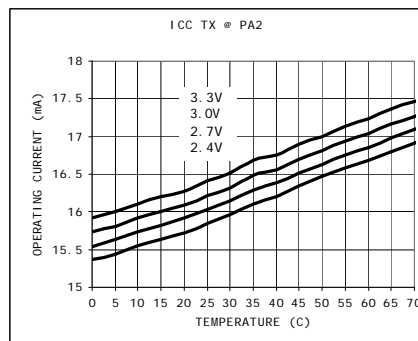
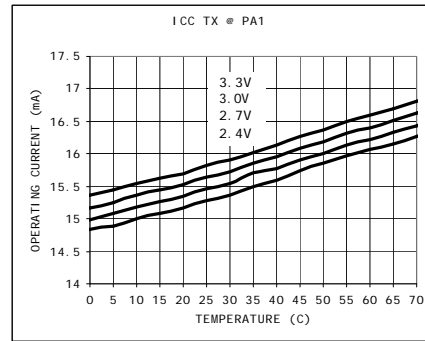
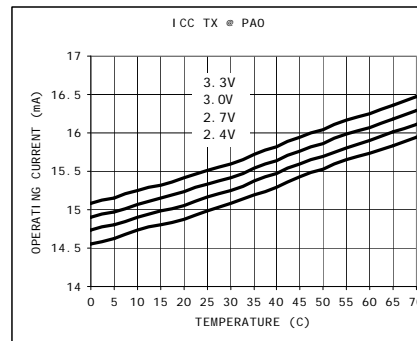
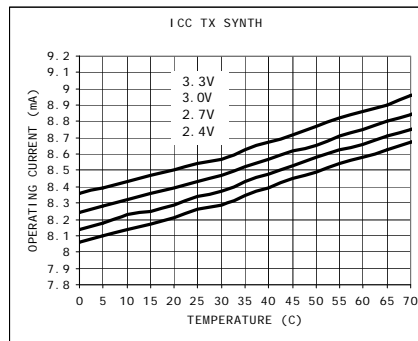
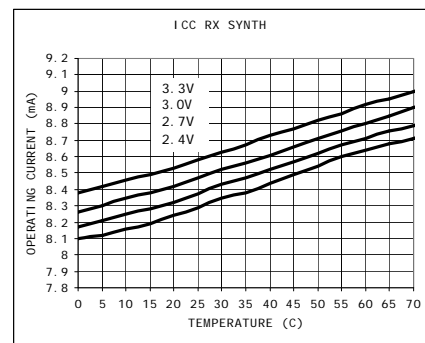
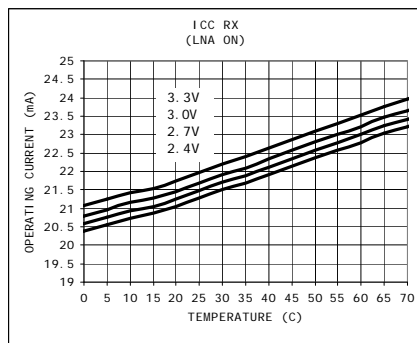
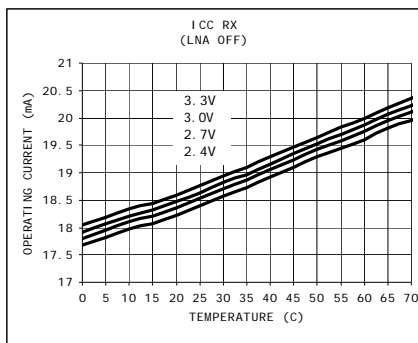
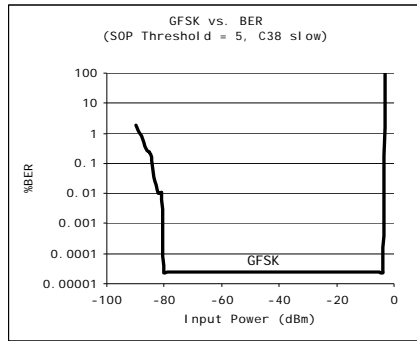
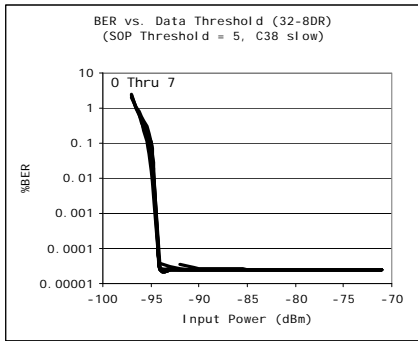


Not recommended for new designs

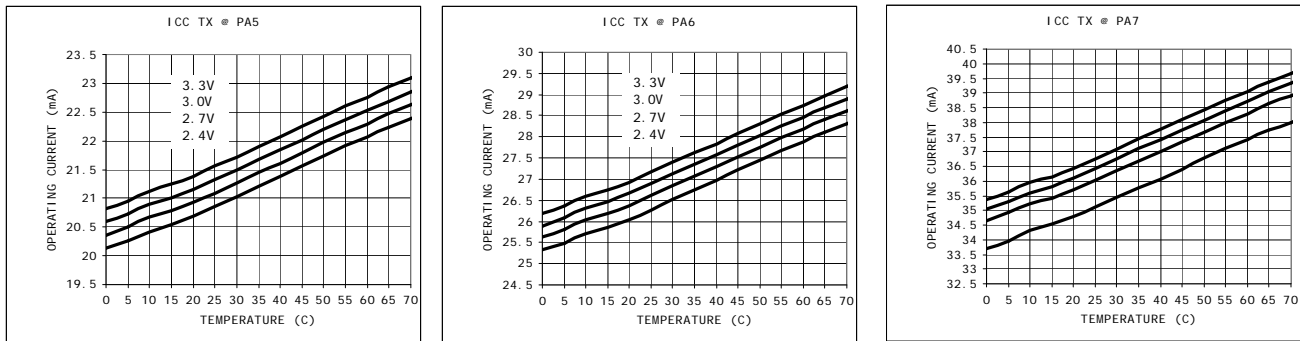
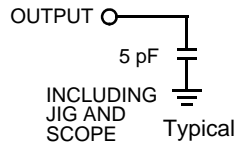
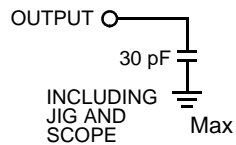
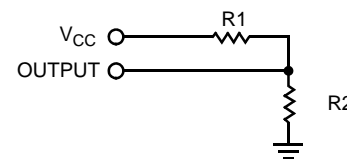
**Note**

22. With LNA on, ATT off, above -2dBm erroneous RSSI values may be read. Cross-checking RSSI with LNA off/on is recommended for accurate readings.

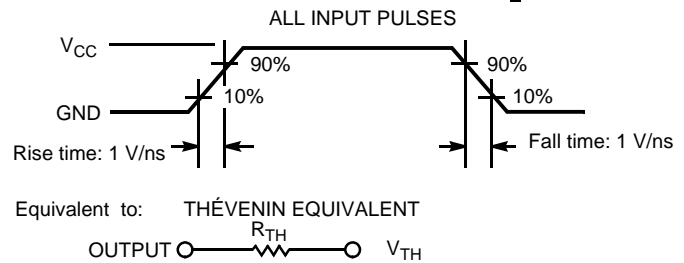
Typical Operating Characteristics (continued)



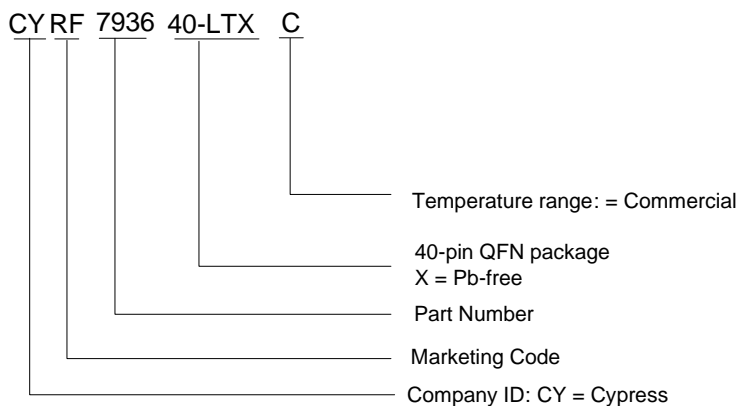
Not recommended for new designs

**Typical Operating Characteristics (continued)**

**Figure 11. AC Test Loads and Waveforms for Digital Pins**
**AC Test Loads**

**DC Test Load**


| Parameter       |      | Unit |
|-----------------|------|------|
| R1              | 1071 | Ω    |
| R2              | 937  | Ω    |
| R <sub>TH</sub> | 500  | Ω    |
| V <sub>TH</sub> | 1.4  | V    |
| V <sub>CC</sub> | 3.00 | V    |


**Ordering Information**

| Part Number     | Radio       | Package Name | Package Type       | Operating Range |
|-----------------|-------------|--------------|--------------------|-----------------|
| CYRF7936-40LTXC | Transceiver | 40-QFN       | 40-QFN (Sawn type) | Commercial      |

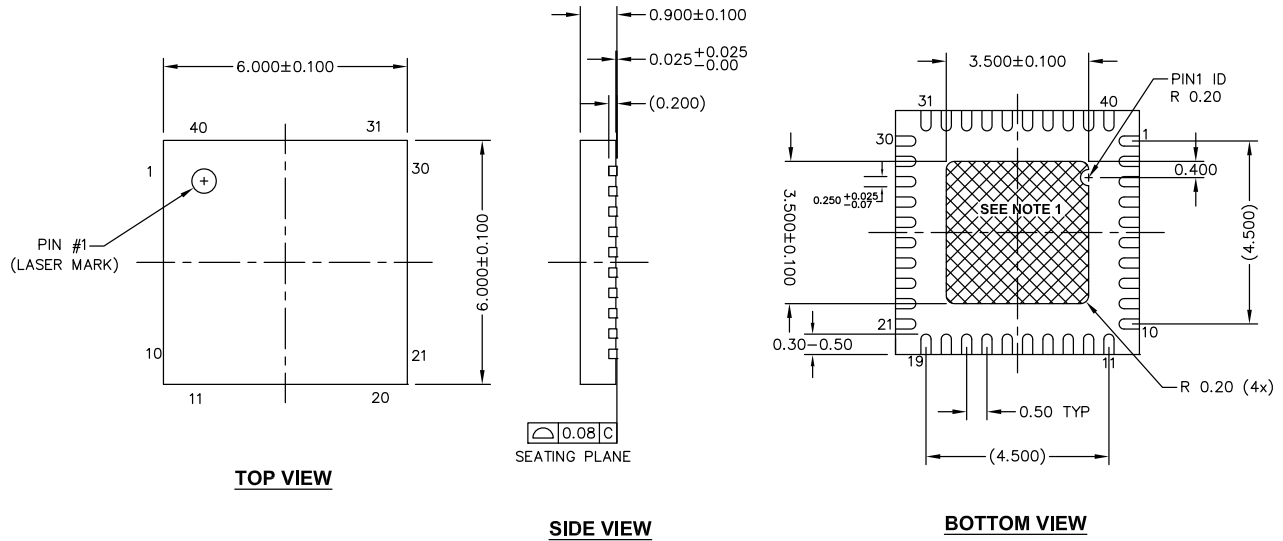
**Ordering Code Definitions**


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### Package Diagram

The recommended dimension of the PCB pad size for the E-pad underneath the QFN is 3.5 mm x 3.5 mm (width x length).

**Figure 12. 40-Pin QFN (6 x 6 x 0.90 mm) Sawn Package Outline**



**NOTES:**

1. HATCH IS SOLDERABLE EXPOSED AREA.
2. REFERENCE JEDEC #: MO-220
3. PACKAGE WEIGHT: 0.086g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-44328 \*G

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## Acronyms

Table 7. Acronyms Used in this Document

| Acronym | Description                              |
|---------|--|
| ACK     | acknowledge (packet received, no errors) |
| ATS     | auto transaction sequencer               |
| BER     | bit error rate                           |
| BOM     | bill of materials                        |
| CMOS    | complementary metal oxide semiconductor  |
| CRC     | cyclic redundancy check                  |
| DSSS    | direct sequence spread spectrum          |
| EOP     | end-of-packet                            |
| FEC     | forward error correction                 |
| GFSK    | gaussian frequency-shift keying          |
| HBM     | human body model                         |
| ISM     | industrial, scientific, and medical      |
| IRQ     | interrupt request                        |
| LNA     | low-noise amplifier                      |
| MCU     | microcontroller unit                     |
| MISO    | master in slave out                      |
| MOSI    | master out slave in                      |
| PA      | power amplifier                          |
| PLL     | phase locked loop                        |
| PMU     | power management unit                    |
| PN      | pseudo noise                             |
| QFN     | quad flat no-leads                       |
| RSSI    | received signal strength indication      |
| RF      | radio frequency                          |
| Rx      | receive                                  |
| SCK     | serial clock                             |
| SDAT    | serial data                              |
| SOP     | start-of-packet                          |
| SPI     | serial peripheral interface              |
| Tx      | transmit                                 |

## Document Conventions

### Units of Measure

Table 8. Units of Measure

| Symbol | Unit of Measure             |
|--------|-----------------------------|
| °C     | degree Celsius              |
| dB     | decibels                    |
| dBc    | decibel relative to carrier |
| dBm    | decibel-milliwatt           |
| Hz     | hertz                       |
| KB     | kilobyte, 1024 bytes        |
| Kbit   | kilobit, 1024 bits          |
| kHz    | kilohertz                   |
| kΩ     | kilohms                     |
| MHz    | megahertz                   |
| MΩ     | megaohm                     |
| μA     | microamperes                |
| μs     | microseconds                |
| μV     | microvolts                  |
| μVrms  | microvolts root-mean-square |
| μW     | microwatts                  |
| mA     | milliampere                 |
| ms     | millisecond                 |
| mV     | millivolts                  |
| nA     | nanoampere                  |
| ns     | nanosecond                  |
| nV     | nanovolts                   |
| Ω      | ohm                         |
| pp     | peak-to-peak                |
| ppm    | parts per million           |
| ps     | picosecond                  |
| sps    | samples per second          |
| V      | volts                       |

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Document History Page

| Description Title: CYRF7936, 2.4 GHz CyFi™ Transceiver<br>Document Number: 001-48013 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Revision   | ECN     | Orig. of Change | Submission Date | Description of Change   |
| **   | 2557501 | KKU / AESA      | 08/25/2008      | New data sheet  |
| *A   | 2615458 | KKU / AESA      | 01/13/2009      | Updated block diagram, changed SoP to SOP, changed EoP to EOP, changed Frequency Initial Stability to Frequency Stability, change section on Low Noise Amplifier. to Receiver Front End and removed AGC enable. Updated Register Map Summary. |
| *B   | 2672793 | DPT / PYRS      | 03/12/2009      | Updated packaging and ordering information.   |
| *C   | 2902376 | TGE             | 03/31/2010      | Removed inactive parts from Ordering Information.<br>Updated Package Diagram.   |
| *D   | 2927979 | TGE / AESA      | 05/05/2010      | Added <a href="#">Contents</a><br>Removed Register Descriptions section.<br>Updated links in <a href="#">Sales</a> , <a href="#">Solutions</a> , and <a href="#">Legal Information</a> .  |
| *E   | 3028381 | TGE             | 09/13/2010      | Updated <a href="#">Applications Support</a> .<br>Added <a href="#">Ordering Code Definitions</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .  |
| *F   | 3346285 | TGE             | 08/18/2011      | Added " <a href="#">Receive Spurious Response</a> " on page 9.<br>Added footnote 20 on page 16.<br>Updated to new template.   |
| *G   | 3611344 | TGE             | 05/08/2012      | Updated <a href="#">Package Diagram</a> :<br>spec 001-44328 – Changed revision from *D to *F.   |
| *H   | 4525927 | ANKC            | 10/06/2014      | Updated to new template.<br>Completing Sunset Review.   |
| *I   | 5742845 | SGUP            | 05/19/2017      | Added watermark "Not recommended for new designs" across the document.<br>Updated <a href="#">Package Diagram</a> :<br>spec 001-44328 – Changed revision from *F to *G.<br>Updated to new template.   |

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