

Octal D-Type Latch with 3-State Output

MC74VHC373, MC74VHCT373A

The MC74VHC373/MC74VHCT373A is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. The device achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC373/MC74VHCT373A is an 8-bit D-type latch controlled by a latch enable input and an output enable input. When the output enable is high, the 8 outputs are in high impedance state.

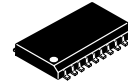
The MC74VHC373 inputs are compatible with standard CMOS levels while the MC74VHCT373A inputs are compatible with TTL levels. The MC74VHCT373A can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The MC74VHC373 and MC74VHCT373A input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT373A output structures provide protection when $V_{CC} = 0$ V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 5.0$ ns (Typ) at $V_{CC} = 5.0$ V (VHC)
 $t_{PD} = 7.7$ ns (Typ) at $V_{CC} = 5.0$ V (VHCT)
- Low Power Dissipation: $I_{CC} = 4.0$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$
- Power Down Protection Provided
- Balanced Propagation Delays
- Designed for: 2.0 V to 5.5 V (VHC)
4.5 V to 5.5 V (VHCT)
- Low Noise: $V_{OLP} = 0.9$ V (Max) (VHC)
 $V_{OLP} = 1.6$ V (Max) (VHCT)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- Chip Complexity: 196 FETs or 49 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

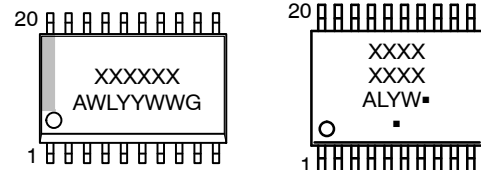


SOIC-20
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAMS



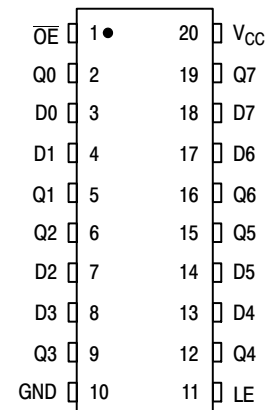
SOIC-20

TSSOP-20

- A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MC74VHC373, MC74VHCT373A

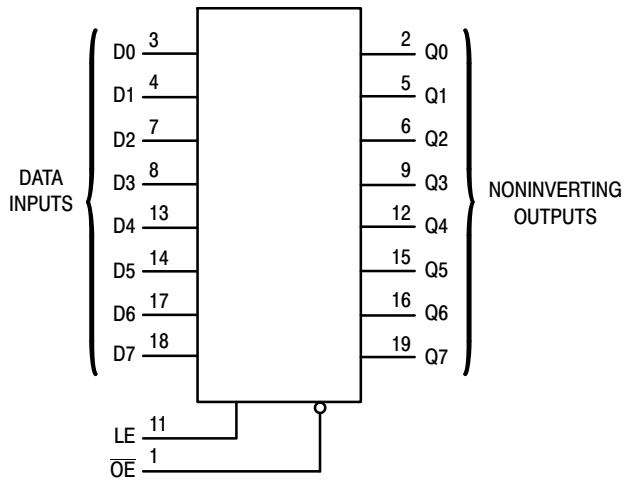


Figure 1. Logic Diagram

FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V	
V _{IN}	DC Input Voltage	−0.5 to +6.5	V	
V _{OUT}	DC Output Voltage (MC74VHC)	−0.5 to V _{CC} + 0.5	V	
	DC Output Voltage (MC74VHCT)	−0.5 to V _{CC} + 0.5		
	Active Mode (High or Low State)	−0.5 to +6.5		
	Tristate Mode (Note 1)	−0.5 to +6.5		
	Power-Off Mode (V _{CC} = 0 V)	−0.5 to +6.5		
I _{IN}	DC Input Current, per Pin	±20	mA	
I _{OUT}	DC Output Current, Per Pin	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA	
I _{IK}	Input Clamp Current	−20	mA	
I _{OK}	Output Clamp Current	MC74VHC373 MC74VHCT373A	±20 −20	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 2)	SOIC−20W TSSOP−20	96 150	°C/W
P _D	Power Dissipation in Still Air at 25°C	SOIC−20W TSSOP−20	1302 833	mW
MSL	Moisture Sensitivity	SOIC−20W All Other Packages	Level 3 Level 1	–
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.373 in	–
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V
I _{LATCHUP}	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

MC74VHC373, MC74VHCT373A

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
MC74VHC					
V _{CC}	DC Supply Voltage	2.0	5.5	V	
V _{IN}	DC Input Voltage (Note 5)	0	5.5	V	
V _{OUT}	DC Output Voltage (Note 5)	0	V _{CC}	V	
T _A	Operating Temperature	−40	+85	°C	
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	0	20	

MC74VHCT

V _{CC}	DC Supply Voltage	4.5	5.5	V		
V _{IN}	DC Input Voltage (Note 5)	0	5.5	V		
V _{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State)	0	V _{CC}	V	
		Tristate Mode	0	5.5		
		Power-Off Mode (V _{CC} = 0 V)	0	5.5		
T _A	Operating Temperature	−40	+85	°C		
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 4.5 V to 5.5 V		0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74VHC373)

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25^\circ\text{C}$			$T_A = -40\text{ to }85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$			1.50 $V_{CC} \times 0.7$		V
V_{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 $V_{CC} \times 0.3$		0.50 $V_{CC} \times 0.3$	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -50\text{ }\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -4\text{ mA}$ $I_{OH} = -8\text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 50\text{ }\mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4\text{ mA}$ $I_{OL} = 8\text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5\text{ V or GND}$	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74VHC373, MC74VHCT373A

AC ELECTRICAL CHARACTERISTICS (MC74VHC373)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.3 9.8	11.4 14.9	1.0 1.0	13.5 17.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		4.9 6.4	7.2 9.2	1.0 1.0	8.5 10.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, LE to Q	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.0 6.5	7.2 9.2	1.0 1.0	8.5 10.5	
t _{PZL} , t _{PZH}	Output Enable Time, OE to Q	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.3 9.8	11.4 14.9	1.0 1.0	13.5 17.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.5 7.0	8.1 10.1	1.0 1.0	9.5 11.5	
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Q	V _{CC} = 3.3 ± 0.3 V C _L = 50 pF		9.5	13.2	1.0	15.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 50 pF		6.5	9.2	1.0	10.5	
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 3.3 ± 0.3 V C _L = 50 pF (Note 6)			1.5		1.5	ns
		V _{CC} = 5.5 ± 0.5 V C _L = 50 pF (Note 6)			1.0		1.0	ns
C _{in}	Maximum Input Capacitance			4	10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High- Impedance State)			6				pF

C _{PD}	Power Dissipation Capacitance (Note 7)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		27	

6. Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC373, MC74VHCT373A

NOISE CHARACTERISTICS (MC74VHC373) ($C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.6	-0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (MC74VHC373)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40$ to 85°C	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$		5.0 5.0	5.0 5.0	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$		4.0 4.0	4.0 4.0	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \pm 0.5 \text{ V}$		1.0 1.0	1.0 1.0	ns

MC74VHC373, MC74VHCT373A

DC ELECTRICAL CHARACTERISTICS (MC74VHCT373A)

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V _{IL}	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OH} = - 50 μA	4.5	4.4	4.5		4.4		V
		I _{OH} = - 8 mA	4.5	3.94			3.80		
V _{OL}	Maximum Low-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5		0.0	0.1		0.1	V
		I _{OL} = 8 mA	4.5			0.36		0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I _{OZ}	Maximum 3-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5			±0.25		±2.5	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0	μA
I _{CC(T)}	Quiescent Supply Current	Per Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0			0.5		5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHCT373A)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, LE to Q	V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		7.7 8.5	12.3 13.3	1.0 1.0	13.5 14.5	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.1 5.9	8.5 9.5	1.0 1.0	9.5 10.5	ns
t _{PZL} , t _{PZH}	Output Enable Time, OE to Q	V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		6.3 7.1	10.9 11.9	1.0 1.0	12.5 13.5	ns
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Q	V _{CC} = 5.0 ± 0.5 V C _L = 50 pF		8.8	11.2	1.0	12.0	ns
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 5.5 ± 0.5 V C _L = 50 pF (Note 8)			1.0		1.0	ns
C _{in}	Maximum Input Capacitance			4	10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)			6				pF

C _{PD}	Power Dissipation Capacitance (Note 9)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		25	

8. Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.

9. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC373, MC74VHCT373A

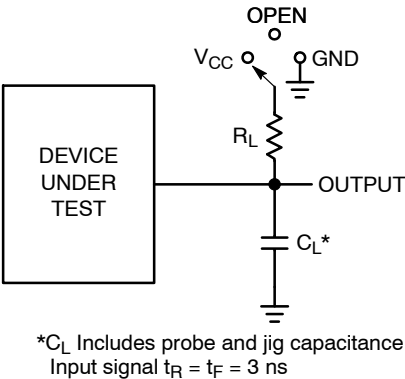
NOISE CHARACTERISTICS (MC74VHCT373A) ($C_L = 50 \text{ pF}$, $V_{CC} = 5.0\text{V}$)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-1.2	-1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (MC74VHCT373A)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40 \text{ to } 85^\circ\text{C}$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 5.0 \pm 0.5 \text{ V}$		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 5.0 \pm 0.5 \text{ V}$		1.5	1.5	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 5.0 \pm 0.5 \text{ V}$		3.5	3.5	ns

MC74VHC373, MC74VHCT373A



Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 2. Test Circuits

SWITCHING WAVEFORMS

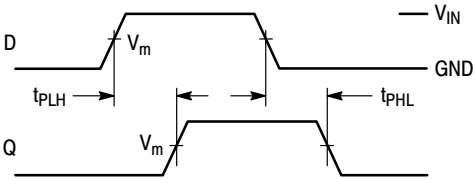


Figure 3.

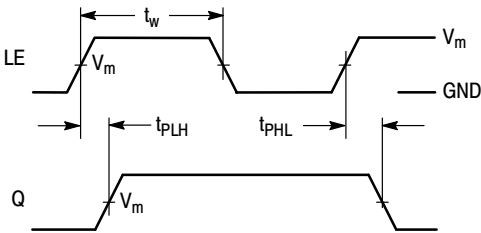


Figure 4.

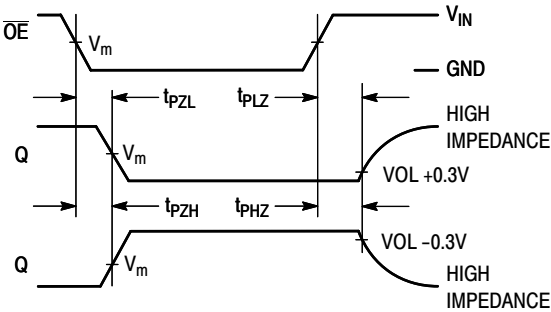


Figure 5.

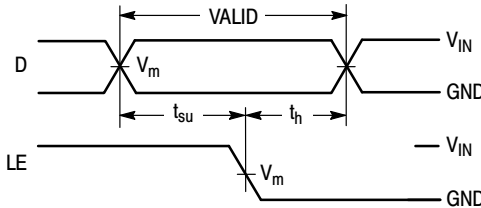


Figure 6.

Device	V _{IN} , V	V _m , V
MC74VHC373	V _{CC}	50% x V _{CC}
MC74VHCT373A	3 V	1.5 V

MC74VHC373, MC74VHCT373A

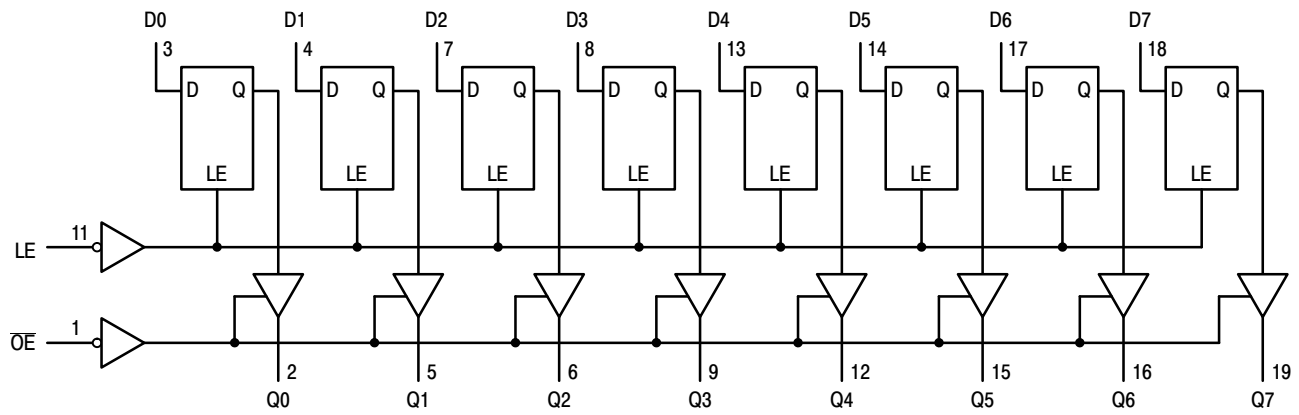


Figure 7. Expanded Logic Diagram

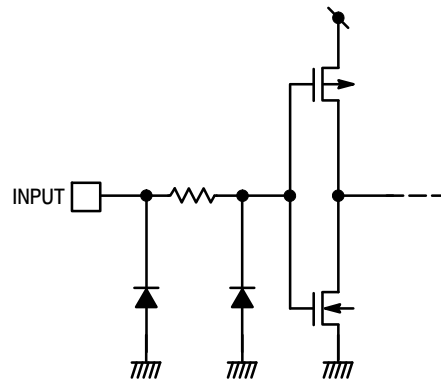


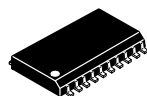
Figure 8. Input Equivalent Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74VHC373DWR2G	VHC373G	SOIC-20W	1000 / Tape & Reel
MC74VHC373DTR2G	VHC 373	TSSOP-20	2500 / Tape & Reel
MC74VHCT373ADWR2G	VHCT373AG	SOIC-20W	1000 / Tape & Reel
MC74VHCT373ADTR2G	VHCT 373A	TSSOP-20	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

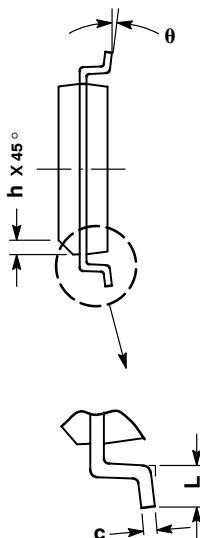
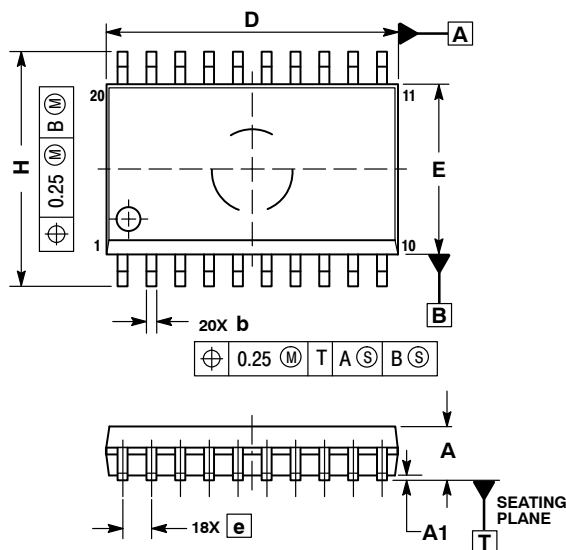
*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

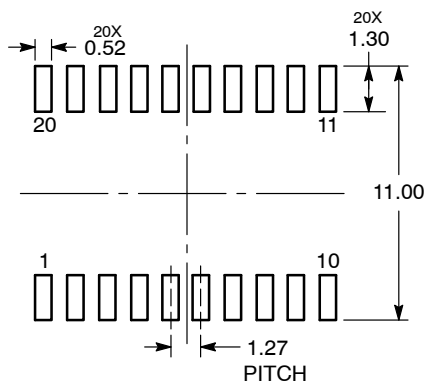


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

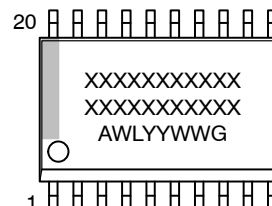
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

