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DATA SHEET
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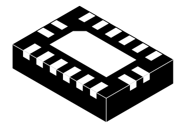
Low-Voltage Dual-Supply 6-Bit Voltage Translator with Auto-Direction Sensing

FXL2SD106



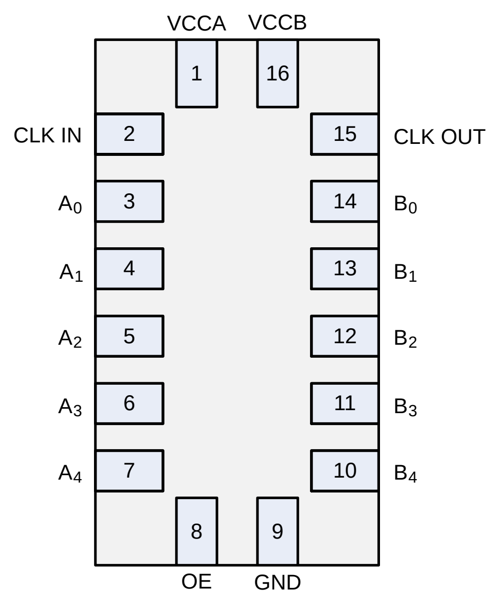
WQFN16 3.5x2.5, 0.5P
CASE 510CC

MARKING DIAGRAM

&Z&2&K
2SD106

2SD106 = Specific Device Code
&Z = Assembly Plant Code
&2 = 2-Digit Date Code
&K = 2-Digits Lot Run Traceability Code

CONNECTION DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

General Description

The FXL2SD106 is a configurable dual-voltage-supply translator designed for both uni-directional and bidirectional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

The device remains in 3-state until both V_{CC} reach active levels, allowing either V_{CC} to be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The OE input, when low, disables both A and B ports by placing them in a 3-state condition. The FXL2SD106 is designed so that OE and CLK IN are supplied by V_{CCA}.

The device senses an input signal on A or B port automatically. The input signal is transferred to the other port.

The FXL2SD106 is not designed for SD card applications. The internal bus hold circuitry conflicts with pull-up resistors. SD cards have internal pull-up resistors on the CD/DAT3 pins.

Features

- Bi-Directional Interface between Two Levels: 1.1 V and 3.6 V
- Fully Configurable: Inputs and Outputs Track V_{CC} Level
- Non-Preferential Power-up; Either V_{CC} May Be Powered-up First
- Outputs Remain in 3-State until Active V_{CC} Level is Reached
- Outputs Switch to 3-State if Either V_{CC} is at GND
- Power-Off Protection
- Bus hold on Data Inputs Eliminates Need for Pull-up Resistors (Do NOT Use Resistors on the A or B Ports)
- OE and CLK IN are Referenced to V_{CCA} Voltage
- Packaged in 16-Terminal DQFN (2.5 mm x 3.5 mm)
- Direction Control Not Needed
- 80 Mbps Throughput Translating between 1.8 V and 2.5 V
- ESD Protection Exceeds:
  - 12 kV HBM (B port I/O to GND) (per JESD22−A114 & Mil Std 883e 3015.7)
  - 8 kV HBM (A port I/O to GND) (per JESD22−A114 & Mil Std 883e 3015.7)
  - 1 kV CDM (per ESD STM 5.3)

PIN DESCRIPTION

Number	Name	Description
1	V_{CCA}	A-Side Power Supply
2	CLK IN	A-Side Input
3–7	A_0–A_4	A-Side Inputs or 3-State Outputs
8	OE	Output Enable Input
9	GND	Ground
10–14	B_4–B_0	B-Side Inputs or 3-State Outputs
15	CLK OUT	3-State Output
16	V_{CCB}	B-Side Power Supply

Functional Diagram

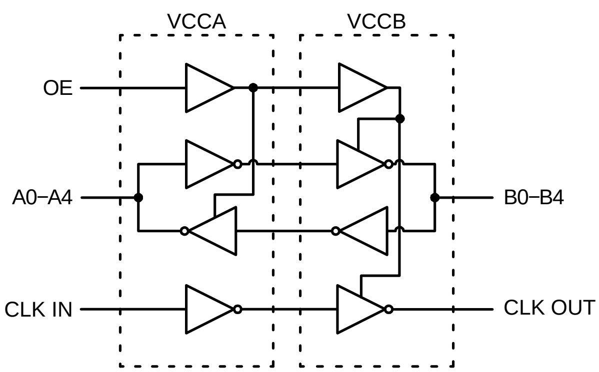


Figure 1. Functional Diagram

FUNCTIONAL TABLE

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up / power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is the following:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input high to enable the device.

The recommended power-down sequence is the following:

1. Drive OE input low to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	–0.5 V to +4.6 V
V_I	DC Input Voltage I/O Port A I/O Port B OE, CLK IN	 –0.5 V to +4.6 V –0.5 V to +4.6 V –0.5 V to +4.6 V
V_O	Output Voltage (Note 1) Outputs 3-STATE Outputs Active (A_n) Outputs Active (B_n, CLK OUT)	 –0.5 V to +4.6 V –0.5 V to V_{CCA} + 0.5 V –0.5 V to V_{CCB} + 0.5 V
I_{IK}	DC Input Diode Current at $V_I < 0$ V	–50 mA
I_{OK}	DC Output Diode Current at $V_O < 0$ V $V_O > V_{CC}$	 –50 mA +50 mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	–50 mA / +50 mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100 mA
T_{STG}	Storage Temperature Range	–65 °C to +150 °C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O Absolute Maximum Rating must be observed.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1 V to 3.6 V
	Input Voltage Port A Port B OE, CLK IN	 0.0 V to 3.6 V 0.0 V to 3.6 V 0.0 V to V_{CCA}
	Dynamic Output Current in I_{OH}/I_{OL} with V_{CC} at 3.0 V to 3.6 V 2.3 V to 2.7 V 1.65 V to 1.95 V 1.4 V to 1.65 V 1.1 V to 1.4 V	 ±18.0 mA ±11.8 mA ±7.4 mA ±5.0 mA ±2.6 mA
	Static Output Current I_{OH}/I_{OL} with V_{CC} at 1.1 V to 3.6 V	±20.0 μA
T_A	Free Air Operating Temperature	–40 °C to +85 °C
Δt / ΔV	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1 V to 3.6 V	10 ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

DC ELECTRICAL CHARACTERISTICS (T_A = −40 °C to 85 °C)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs A_n, CLK IN, OE	0.6 x V_{CCA}	–	–	V
		1.1–1.4	1.1–3.6		0.9 x V_{CCA}	–	–	
		1.1–3.6	1.4–3.6	Data inputs B_n	0.6 x V_{CCB}	–	–	
		1.1–3.6	1.1–1.4		0.9 x V_{CCB}	–	–	
V_{IL}	Low Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs A_n, CLK IN, OE	–	–	0.35 x V_{CCA}	V
		1.1 –1.4	1.1–3.6		–	–	0.1 x V_{CCA}	
		1.1–3.6	1.4–3.6	Data inputs B_n	–	–	0.35 x V_{CCB}	
		1.1–3.6	1.1–1.4		–	–	0.1 x V_{CCB}	
V_{OH} (Note 3)	High Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs A_n, I_{HOLD} = –20 μA	0.75 x V_{CCA}	–	–	V
		1.1–1.4	1.1–3.6		–	0.8	–	
		1.1–3.6	1.65–3.6	Data outputs B_n, I_{HOLD} = –20 μA	0.75 x V_{CCB}	–	–	
		1.1–3.6	1.1–1.4		–	0.8	–	
V_{OL} (Note 3)	Low Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs A_n, I_{HOLD} = 20 μA	–	–	0.2 x V_{CCA}	V
		1.1–1.4	1.1–3.6		–	0.3	–	
		1.1–3.6	1.65–3.6	Data outputs B_n, I_{HOLD} = 20 μA	–	–	0.2 x V_{CCB}	
		1.1–3.6	1.1–1.4		–	0.3	–	
$I_{I(ODH)}$ (Note 4)	Bushold Input Overdrive High Current	3.6	3.6	Data inputs A_n, B_n	450	–	–	μA
		2.7	2.7		300	–	–	
		1.95	1.95		200	–	–	
		1.6	1.6		120	–	–	
		1.4	1.4		80	–	–	
$I_{I(ODL)}$ (Note 5)	Bushold Input Overdrive Low Current	3.6	3.6	Data inputs A_n, B_n	−450	–	–	μA
		2.7	2.7		−300	–	–	
		1.95	1.95		−200	–	–	
		1.6	1.6		−120	–	–	
		1.4	1.4		−80	–	–	
I_I	Input Leakage Current	1.1–3.6	3.6	OE, CLK IN, V_I = V_{CCA} or GND	–	–	±1.0	μA

DC ELECTRICAL CHARACTERISTICS (T_A = −40 °C to 85 °C) (continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min	Typ	Max	Unit
I_{OFF}	Power Off Leakage Current	0	3.6	A_n, V_O = 0 V to 3.6 V	−	−	±2.0	μA
		3.6	0	B_n, CLK OUT, V_O = 0 V to 3.6 V	−	−	±2.0	
I_{OZ} (Note 6)	3-State Output Leakage	3.6	3.6	A_n, B_n, CLK OUT, V_O = 0 V or 3.6 V, OE = V_{IL}	−	−	±2.0	μA
		3.6	0	A_n, V_O = 0 V or 3.6 V, OE = Don't Care	−	−	±2.0	
		0	3.6	B_n, CLK OUT, V_O = 0 V or 3.6 V, OE = Don't Care	−	−	±2.0	
$I_{CCA/B}$ (Note 7, 8)	Quiescent Supply Current	1.1–3.6	1.1–3.6	V_I = V_{CCI} or GND, I_O = 0	−	−	5.0	μA
I_{CCZ} (Note 7)	Quiescent Supply Current	1.1–3.6	1.1–3.6	V_I = V_{CCI} or GND, I_O = 0, OE = V_{IL}	−	−	5.0	μA
I_{CCA} (Note 7)	Quiescent Supply Current	0	1.1–3.6	V_I = V_{CCB} or GND; I_O = 0	−	−	−2.0	μA
		1.1–3.6	0	V_I = V_{CCA} or GND; I_O = 0	−	−	2.0	
I_{CCB} (Note 7)	Quiescent Supply Current	1.1–3.6	0	V_I = V_{CCB} or GND; I_O = 0	−	−	−2.0	μA
		0	1.1–3.6	V_I = V_{CCA} or GND; I_O = 0	−	−	2.0	

3. This is the output voltage for static conditions. Dynamic drive specifications are given in "Dynamic Output Electrical Characteristics".
4. An external driver must source at least the specified current to switch LOW-to-HIGH.
5. An external driver must source at least the specified current to switch HIGH-to-LOW.
6. "Don't Care" indicates any valid logic level.
7. V_{CCI} is the V_{CC} associated with the input side.
8. Reflects current per supply, V_{CCA} or V_{CCB}.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS (Note 9)

A PORT (A_n)
Output Load: C_L = 15 pF, R_L > 1 MΩ

Symbol	Parameter	T_A = −40 °C to +85 °C, V_{CCA} =									Unit
		3.0 V to 3.6 V		2.3 V to 2.7 V		1.65 V to 1.95 V		1.4 V to 1.6 V		1.1 V to 1.3 V	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	
t_{rise} (Note 10)	Output Rise Time A Port	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
t_{fall} (Note 11)	Output Fall Time A Port	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
I_{OHD} (Note 10)	Dynamic Output Current High	−18.0	−	−11.8	−	−7.4	−	−5.0	−	−2.6	mA
I_{OLD} (Note 11)	Dynamic Output Current Low	+18.0	−	+11.8	−	+7.4	−	+5.0	−	+2.6	mA

B PORT (B_n, CLK OUT)
Output Load: C_L = 15 pF, R_L > 1 MΩ

Symbol	Parameter	T_A = −40 °C to +85 °C, V_{CCB} =									Unit
		3.0 V to 3.6 V		2.3 V to 2.7 V		1.65 V to 1.95 V		1.4 V to 1.6 V		1.1 V to 1.3 V	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	
t_{rise} (Note 10)	Output Rise Time B Port	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
t_{fall} (Note 11)	Output Fall Time B Port	−	3.0	−	3.5	−	4.0	−	5.0	7.5	ns
I_{OHD} (Note 10)	Dynamic Output Current High	−18.0	−	−11.8	−	−7.4	−	−5.0	−	−2.6	mA
I_{OLD} (Note 11)	Dynamic Output Current Low	+18.0	−	+11.8	−	+7.4	−	+5.0	−	+2.6	mA

9. Dynamic Output Characteristics are guaranteed, but not tested.
10. See Figure 6.
11. See Figure 7.

AC CHARACTERISTICS

Symbol	Parameter	T_A = −40 °C to +85 °C, V_{CCB} = 3.0 V − 3.6 V Typ	3.0 V − 3.6 V Max	2.3 V − 2.7 V Typ	2.3 V − 2.7 V Max	1.65 V − 1.95 V Typ	1.65 V − 1.95 V Max	1.4 V − 1.6 V Typ	1.4 V − 1.6 V Max	1.1 V − 1.3 V Typ	Unit
V_{CCA} = 3.0 V to 3.6 V											
t_{PLH}, t_{PHL}	A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	22.0	ns
	B to A	0.2	3.5	0.2	3.8	0.3	5.0	0.5	6.0	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT	−	3.0	−	3.5	−	4.5	−	6.0	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{skew} (Note 12)	A Port, B Port	−	0.5	−	0.5	−	0.5	−	1.0	1.0	ns
V_{CCA} = 2.3 V to 2.7 V											
t_{PLH}, t_{PHL}	A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	22.0	ns
	B to A	0.3	3.9	0.4	4.2	0.5	5.5	0.5	6.5	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT	−	3.5	−	4.0	−	4.5	−	6.5	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{skew} (Note 12)	A Port, B Port	−	0.5	−	0.5	−	0.5	−	1.0	1.0	ns
V_{CCA} = 1.65 V to 1.95 V											
t_{PLH}, t_{PHL}	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	22.0	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT	−	4.5	−	4.5	−	6.3	−	6.7	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{skew} (Note 12)	A Port, B Port	−	0.5	−	0.5	−	0.5	−	1.0	1.0	ns
V_{CCA} = 1.4 V to 1.6 V											
t_{PLH}, t_{PHL}	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	22.0	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	15.0	ns
t_{PLH}, t_{PHL}	CLK IN to CLK OUT	−	6.0	−	6.5	−	6.7	−	8.5	15.0	ns
t_{PZL}, t_{PZH}	OE to A, OE to B	−	1.7	−	1.7	−	1.7	−	1.7	1.7	μs
t_{skew} (Note 12)	A Port, B Port	−	1.0	−	1.0	−	1.0	−	1.0	1.0	ns

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (Low-to-High or High-to-Low). See Figure 9.

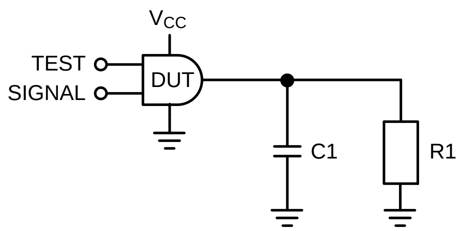
MAXIMUM DATA RATE (Note 13, 14)

V_{CCA}	T_A = −40 °C to +85 °C, V_{CCB} = 3.0 V to 3.6 V Min	2.3 V to 2.7 V Min	1.65 V to 1.95 V Min	1.4 V to 1.6 V Min	1.1 V to 1.3 V Min	Unit
V_{CCA} = 3.0 V to 3.6 V	100	100	80	60	20	Mbps
V_{CCA} = 2.3 V to 2.7 V	100	100	80	60	20	Mbps
V_{CCA} =1.65 V to 1.95 V	80	80	60	40	20	Mbps
V_{CCA} = 1.4 V to 1.6 V	60	60	40	40	20	Mbps
	Typ	**Typ**	**Typ**	**Typ**	**Typ**	
V_{CCA} = 1.1 V to 1.3 V	20	20	20	20	20	Mbps

13. Maximum data rate is guaranteed but not tested.
14. Maximum data rate is specified in megabits per second. See Figure 8. It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

CAPACITANCE

Symbol	Parameter		Conditions	T_A = +25 °C Typical	Unit
C_{IN}	Input Capacitance, OE, CLK IN		VccA = VccB = GND	4	pF
$C_{I/O}$	Input/Output Capacitance	A_n	VccA = VccB = 3.3 V, OE = VccA	5	pF
		B_n, CLK OUT		6	
C_{PD}	Power Dissipation Capacitance		VccA = VccB = 3.3 V, Vi = 0 V or Vcc, f = 10 MHz	25	pF

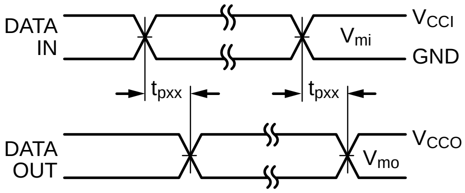


Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}
t_{PZL}	0 V	Low to High Switch
t_{PZH}	V_{CCI}	Low to High Switch

Figure 2. AC Test Circuit

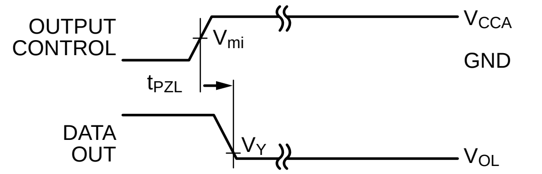
AC LOAD TABLE

V_{CCO}	Cl	Rl
1.2 V ±0.1 V	15 pF	1 MΩ
1.5 V ±0.1 V	15 pF	1 MΩ
1.8 V ±0.15 V	15 pF	1 MΩ
2.5 V ±0.2 V	15 pF	1 MΩ
3.3 V ±0.3 V	15 pF	1 MΩ



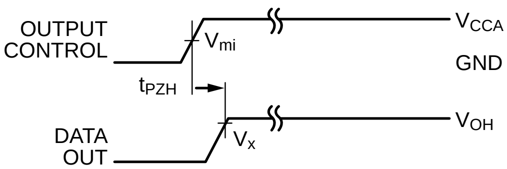
Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ Vi = 3.0 V to 3.6 V only

Figure 3. Waveform for Inverting and Non-inverting Functions



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ Vi = 3.0 V to 3.6 V only

Figure 4. 3-STATE Output Low Enable Time for Low Voltage Logic

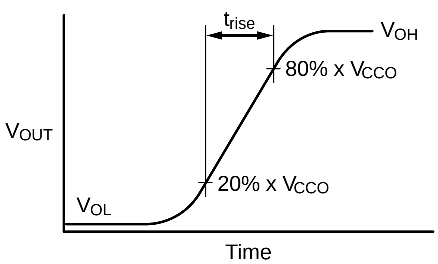


Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ Vi = 3.0 V to 3.6 V only

Figure 5. 3-STATE Output High Enable Time for Low Voltage Logic

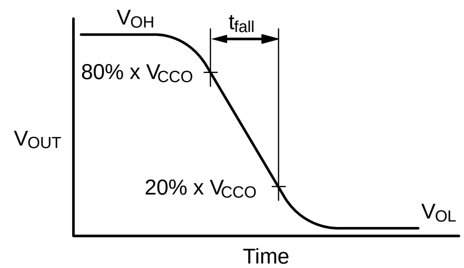
Symbol	Vcc
Vmi (Note 15)	V_{CCI} / 2
Vmo	V_{CCO} / 2
VX	0.9 x V_{CCO}
VY	0.1 x V_{CCO}

15. $V_{CCI} = V_{CCA}$ for control pin OE or Vmi = (V_{CCA} / 2).



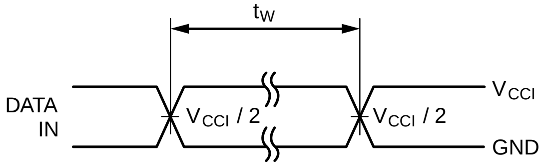
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

Figure 6. Active Output Rise Time and Dynamic Output Current High



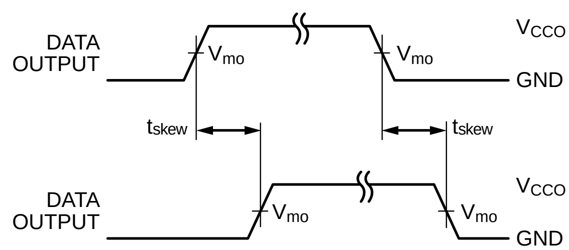
$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

Figure 7. Active Output Fall Time and Dynamic Output Current Low



Max. data rate, f = 1 / t_W

Figure 8. Maximum Data Rate



$t_{skew} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

Figure 9. Output Skew Time

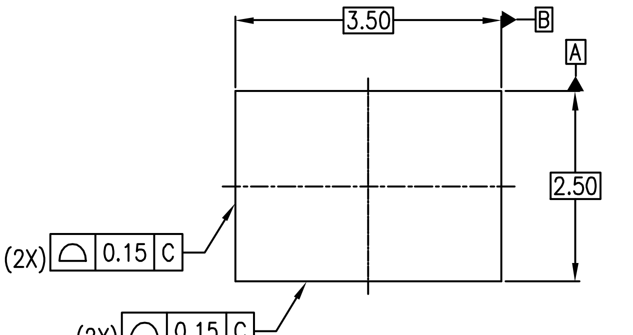
ORDERING INFORMATION

Order Number	Package Number	Package Description	Shipping†
FXL2SD106BQX	MLP16E	16-Terminal Depopulated Quad Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241, 2.5 mm x 3.5 mm (Pb-Free, Halide Free)	3000 / Tape & Reel

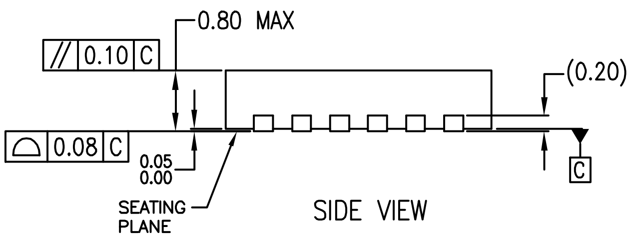
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WQFN16 3.5x2.5, 0.5P
CASE 510CC
ISSUE O

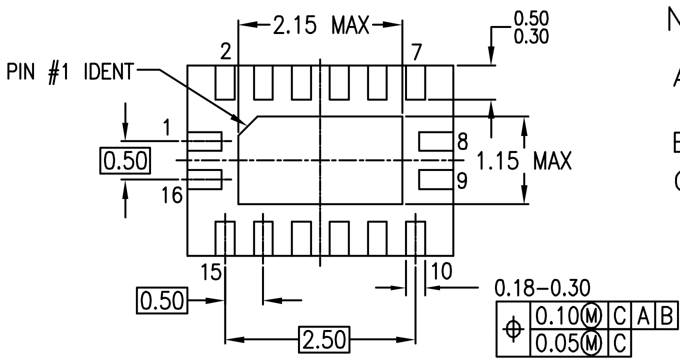
DATE 31 AUG 2016



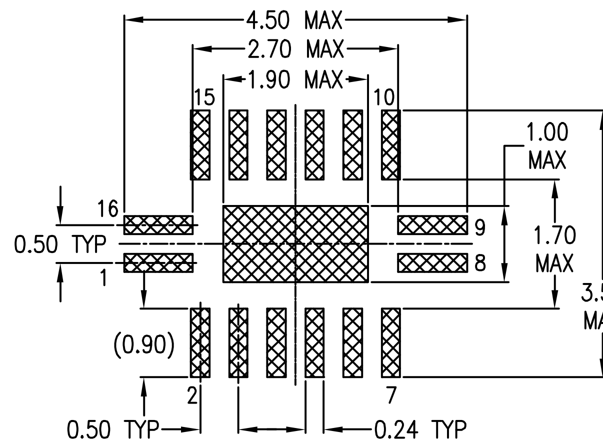
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AB
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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