

NC7SZ32

TinyLogic™ UHS 2-Input OR Gate

General Description

The NC7SZ32 is a single 2-Input OR Gate from Fairchild's Ultra High Speed Series of TinyLogic™. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage.

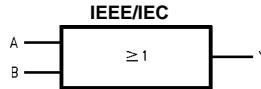
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra high speed t_{PD} 2.4 ns Typ into 50 pF at 5V V_{CC}
- High output drive ± 24 mA at 3V V_{CC}
- Broad V_{CC} operating range 1.65V–5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V–3V translation
- Patented noise/EMI reduction circuitry implemented

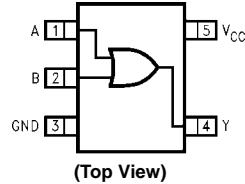
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ32M5	MA05B	7Z32	5-Lead SOT23, JEDEC MO-178, 1.6mm	250 Units on Tape and Reel
NC7SZ32M5X	MA05B	7Z32	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ32P5	MAA05A	Z32	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	250 Units on Tape and Reel
NC7SZ32P5X	MAA05A	Z32	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output

Function Table

$$Y = A + B$$

Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +6V
DC Input Voltage (V_{IN})	–0.5V to +6V
DC Output Voltage (V_{OUT})	–0.5V to +6V
DC Input Diode Current (I_{IK})	
@ $V_{IN} < -0.5V$	–50 mA
@ $V_{IN} > 6V$	+20 mA
DC Output Diode Current (I_{OK})	
@ $V_{OUT} < -0.5V$	–50 mA
@ $V_{OUT} > 6V, (V_{CC} = GND)$	+20 mA
DC Output Current (I_{OUT})	±50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±50 mA
Storage Temperature (T_{STG})	–65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L); Soldering, 10 seconds	260°C
Power Dissipation (P_D) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.65V to 5.5
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	–40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute Maximum Ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

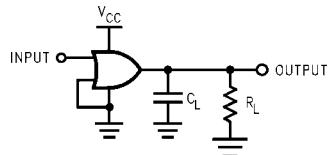
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			Units	Conditions
			Min	Typ	Max		
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}		0.75 V_{CC} 0.7 V_{CC}	V	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95 2.3 to 5.5		0.25 V_{CC} 0.3 V_{CC}		V	
V_{OH}	HIGH Level Output Voltage	1.65 1.8 2.3 3.0 4.5	1.55 1.7 2.2 2.9 4.4	1.65 1.8 2.3 3.0 4.5	1.65 1.7 2.2 2.9 4.4	V	$V_{IN} = V_{IH}$ $I_{OH} = -100 \mu A$
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20	1.29 1.9 2.4 2.3 3.8		
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20	1.29 1.9 2.4 2.3 3.8		
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20	1.29 1.9 2.4 2.3 3.8		
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20	1.29 1.9 2.4 2.3 3.8		
	LOW Level Output Voltage	1.65 1.8 2.3 3.0 4.5	0.0 0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1 0.1	0.1 0.1 0.1 0.1 0.1	V	$V_{IN} = V_{IL}$ $I_{OL} = 100 \mu A$
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
		1.65 2.3 3.0 3.0 4.5	0.08 0.10 0.15 0.22 0.22	0.24 0.3 0.4 0.55 0.55	0.24 0.3 0.4 0.55 0.55		
I_{IN}	Input Leakage Current	0 to 5.5		±1	±10	μA	$V_{IN} = 5.5V, GND$
I_{OFF}	Power Off Leakage Current	0.0		1	10	μA	V_{IN} or $V_{OUT} = 5.5V$
I_{CC}	Quiescent Supply Current	1.65 to 5.5		2.0	20	μA	$V_{IN} = 5.5V, GND$

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C			Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max				
t _{PLH} , t _{PHL}	Propagation Delay	1.65	2.0	5.5	12.0	2.0	12.7	ns	C _L = 15 pF, R _L = 1MΩ	Figures 1, 3	
		1.8	2.0	4.6	10	2.0	10.5				
		2.5 ± 0.2	0.8	3.0	7.0	0.8	7.5				
		3.3 ± 0.3	0.5	2.4	4.7	0.5	5.0				
		5.0 ± 0.5	0.5	1.9	4.1	0.5	4.4				
t _{PLH} , t _{PHL}	Propagation Delay	3.3 ± 0.3	1.5	3.0	5.2	1.5	5.5	ns	C _L = 50 pF, R _L = 500Ω	Figures 1, 3	
		5.0 ± 0.5	0.8	2.4	4.5	0.8	4.8				
C _{IN}	Input Capacitance	0	4					pF			
C _{PD}	Power Dissipation Capacitance	3.3	20					pF	(Note 3)	Figure 2	
		5.0	26								

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic})$.

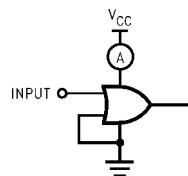
AC Loading and Waveforms



C_L includes load and stray capacitance.

Input PRR = 1.0 MHz, t_w = 500 ns.

FIGURE 1. AC Test Circuit



Input = AC Waveforms; t_r = t_f = 1.8 ns;

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

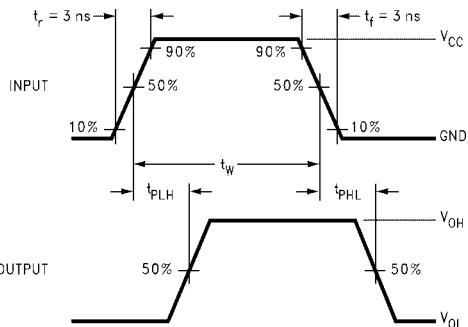


FIGURE 3. AC Waveforms

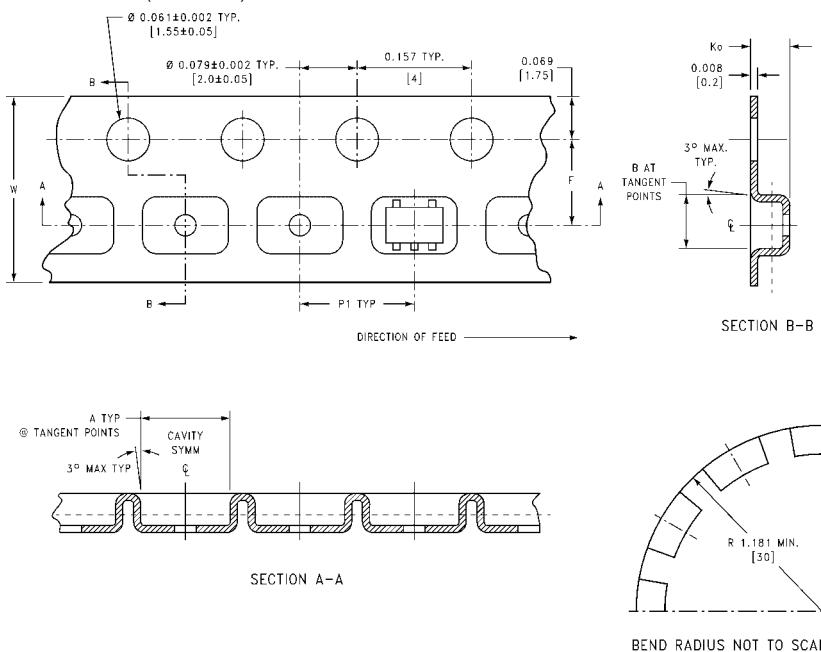
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Tape and Reel Specification

TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5, P5	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

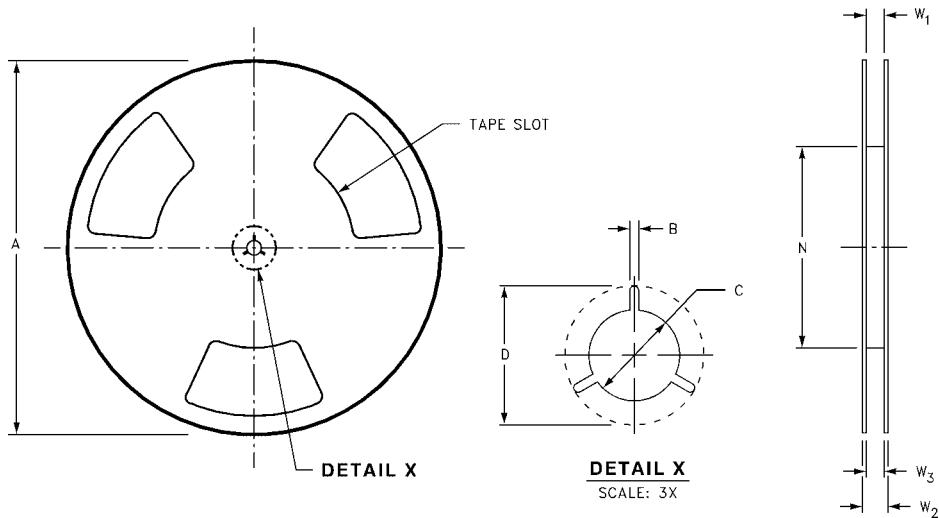
TAPE DIMENSIONS inches (millimeters)



Package	Tape Size	DIM A	DIM B	DIM F	DIM K ₀	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

Tape and Reel Specification (Continued)

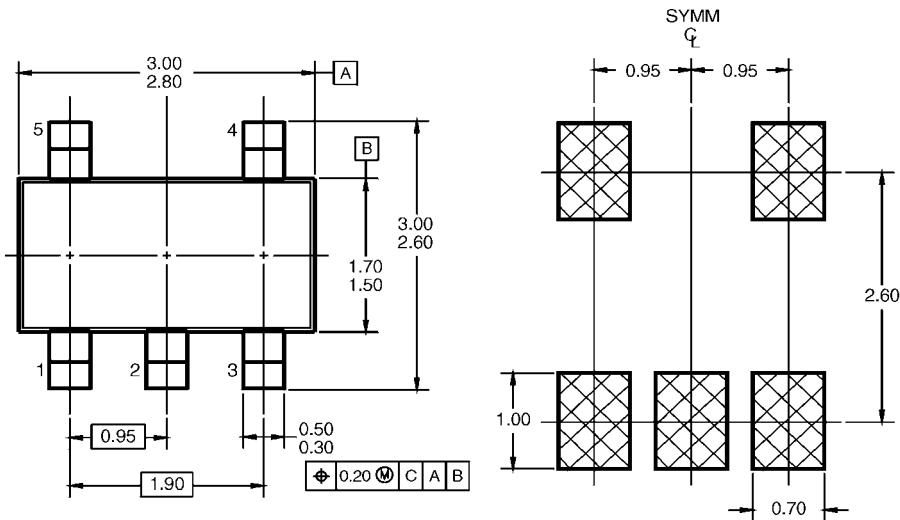
REEL DIMENSIONS inches (millimeters)



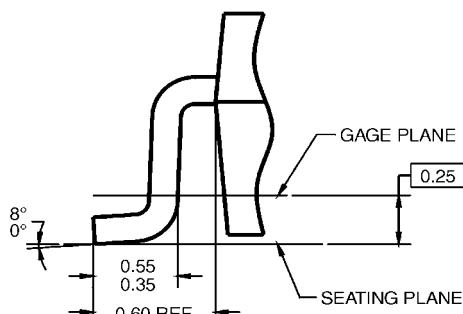
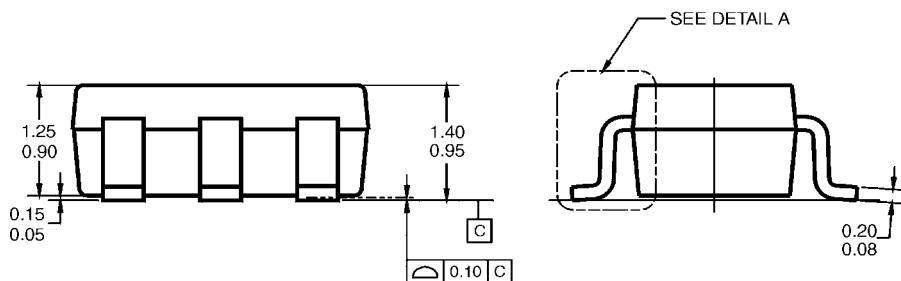
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

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Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



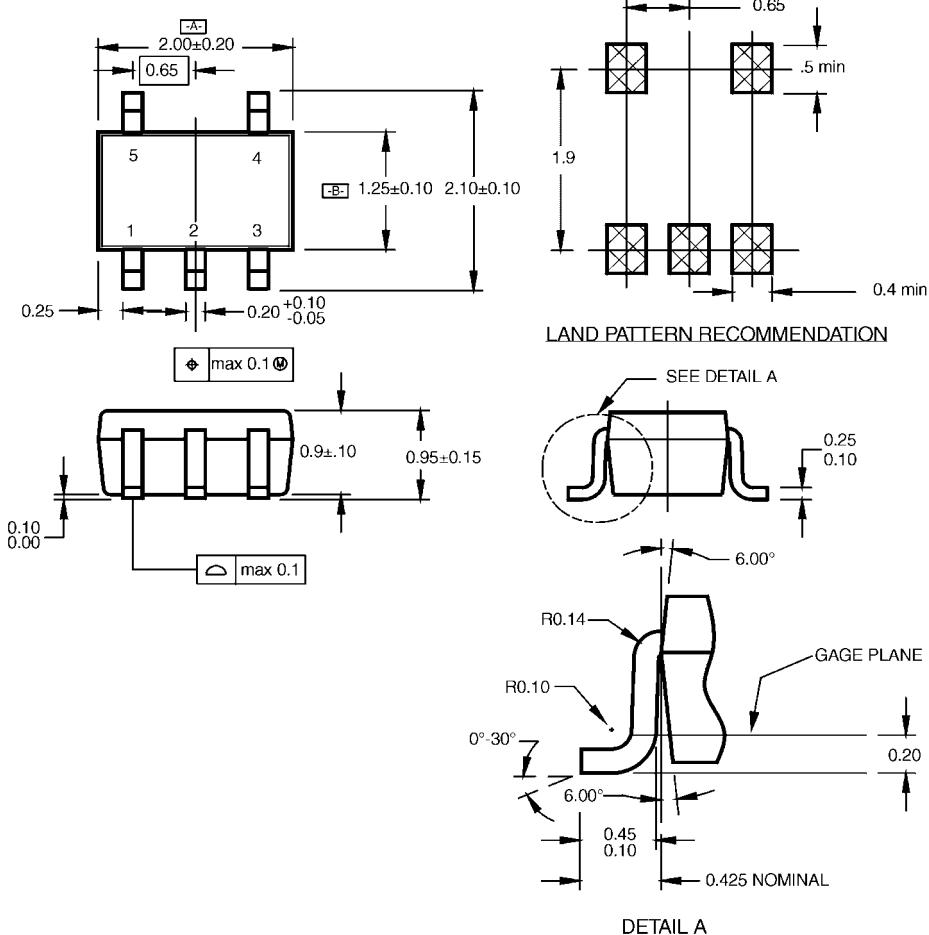
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC
MO-178, ISSUE B, VARIATION AA,
DATED JANUARY 1999.
B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

DETAIL A

5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DETAIL A

NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A**

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