128 Mb / 256 Mb / 512 Mb FS-S Flash

SPI Multi-I/O, 1.8 V, 102 MHz DDR

General description

This supplementary document contains information for the FS-S-102 MHz DDR. Specifications contained in this supplement supersede those in the S25FS128S, S25FS256S and S25FS512S datasheets. The maximum DDR Clock rate was increased from 80 MHz to 102 MHz. Refer to the latest S25FS128S, S25FS256S and S25FS512S datasheets for full electrical specifications.

Affected documents/Related documents

Table 1 Affected documents/Related documents

Title	Publication number
S25FS128S, S25FS256S 128 Mb (16 MB) / 256 Mb (32 MB) FS-S Flash, SPI Multi-I/O, 1.8 V	002-00368
S25FS512S 512 Mb (64 MB) FS-S Flash, SPI Multi-I/O, 1.8 V	002-00488

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1 DDR AC characteristics

Table 2 DDR AC characteristics operation

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for DDR READ instruction	DC	–	102	MHz
$P_{SCK, R}$	SCK clock period for DDR READ instruction	1/ F_{SCK}	–	∞	ns
t_{WH}, t_{CH}	Clock High time	50% P_{SCK} – 5%	–	50% P_{SCK} + 5%	
t_{WL}, t_{CL}	Clock Low time	50% P_{SCK} – 5%	–	50% P_{SCK} + 5%	
t_{CS}	CS# HIGH time (Read instructions) CS# HIGH time (Read instructions when Reset feature is enabled)	10 20	–	–	
t_{CSS}	CS# Active Setup time (Relative to SCK)	2	–	–	
t_{CSH}	CS# Active Hold time (Relative to SCK)	3	–	–	
t_{SU}	IO in Setup time	1.5	–	–	
t_{HD}	IO in Hold time	1.5	–	–	
t_V	Clock Low to Output valid	1.5	–	5[1]	
t_{HO}	Output Hold time	1	–	–	
t_{DIS}	Output Disable time Output Disable time (When Reset feature is enabled)	–	–	8 20	
t_{IO_skew}	First IO to last IO data valid time	–	–	400	ps
t_{DPD}	CS# High to Power-down mode	–	–	3	µs
t_{RES}	CS# High to Standby mode without Electronic Signature Read	–	–	30	

Notes
1. CL = 15 pF.

1.1 DDR input timing

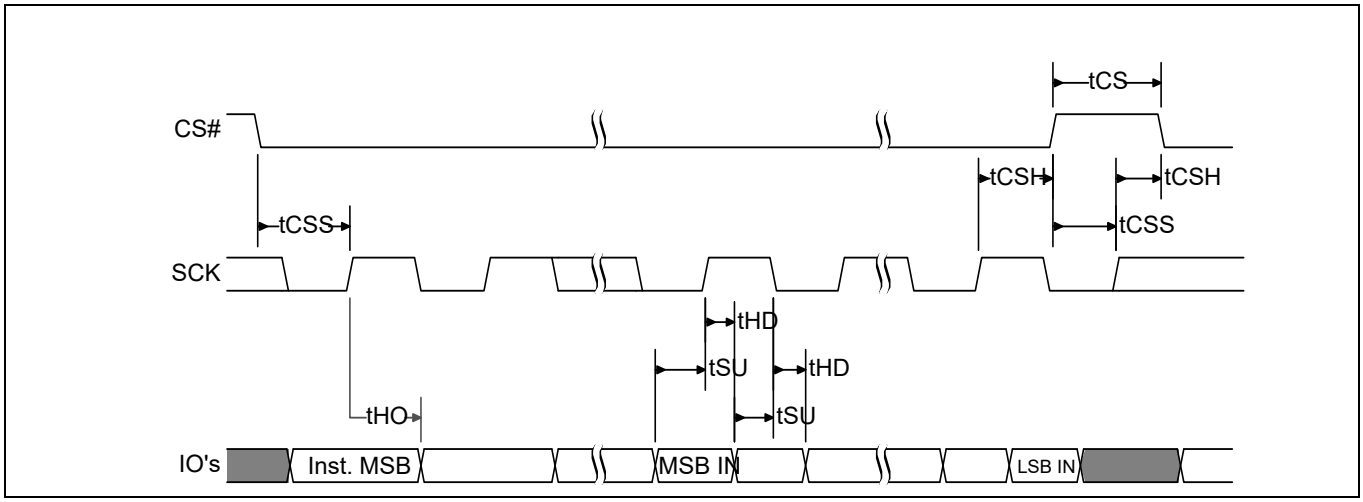


Figure 1 SPI DDR input timing

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1.2 DDR output timing

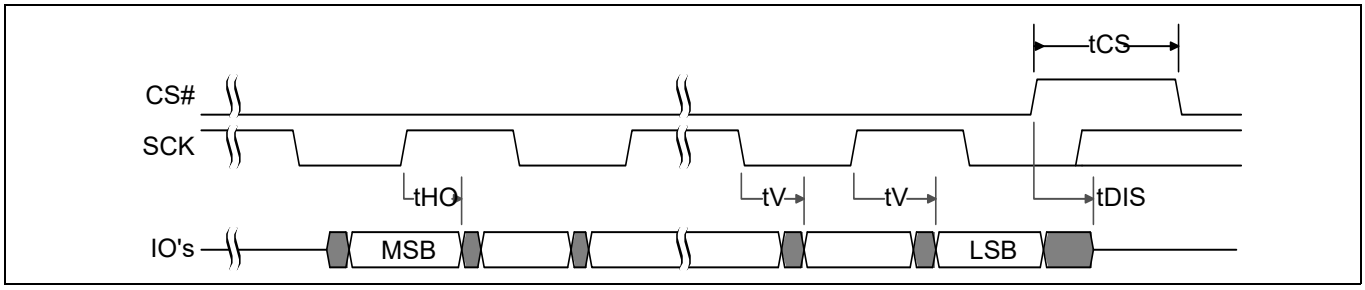


Figure 2 SPI DDR output timing

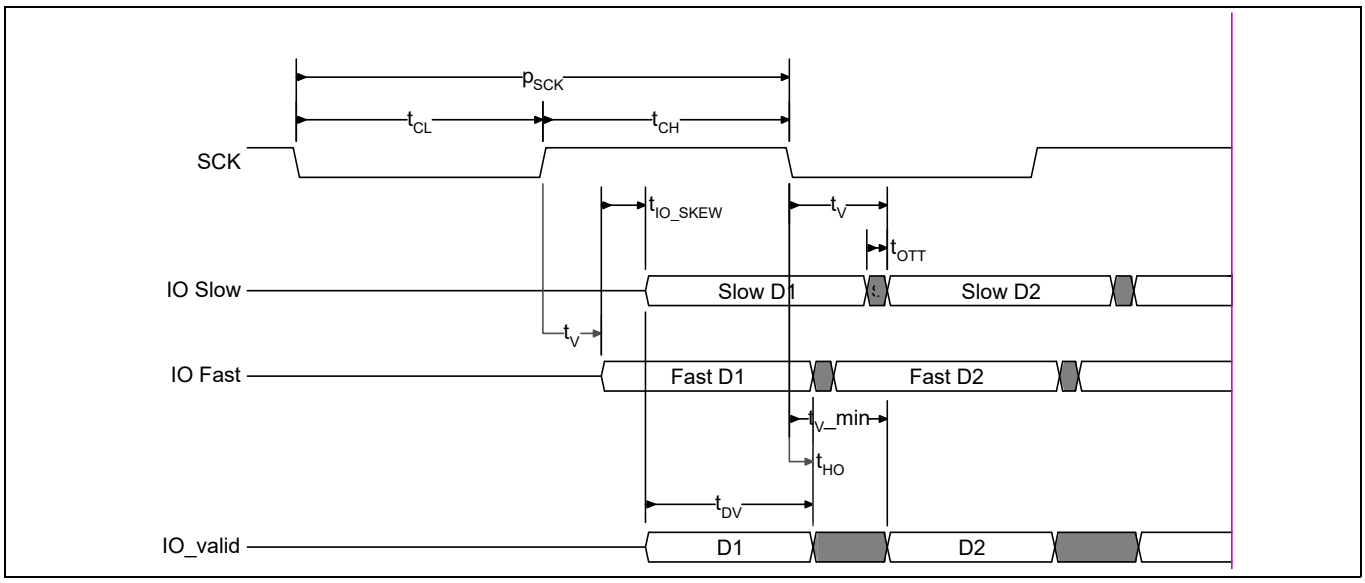


Figure 3 SPI DDR Data Valid Window[2, 3, 4, 5]

Notes

2. t_{CLH} is the shorter duration of t_{CL} or t_{CH}.
3. t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.
4. t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO.
5. t_{OTT} is dependent on system level considerations including:
   a. Memory device output impedance (drive strength).
   b. System level parasitics on the IOs (primarily bus capacitance).
   c. Host memory controller input V_{IH} and V_{IL} levels at which 0 to 1 and 1 to 0 transitions are recognized.
   d. As an example, assuming that the above considerations result in a memory output slew rate of 2 V/ns and a 3V transition (from 1 to 0 or 0 to 1) is required by the host, the t_{OTT} would be: t_{OTT} = 2 V / (2 V/ns) = 1.0 ns.
   e. t_{OTT} is not a specification tested by Infineon, it is system dependent and must be derived by the system designer based on the above considerations.

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DDR AC characteristics

The minimum data valid window (t_{DV}) can be calculated as follows:

As an example, assuming: 102 MHz clock frequency = 9.8 ns clock period with DDR operations are specified to have a duty cycle of 45% or higher.

- t_{CLH} = 0.45 × PSCK = 0.45 × 9.8 ns = 4.41 ns
- t_{IO_SKEW} = 400 ps
- t_{OTT} = 1.0 ns
- $t_{DV} = t_{CLH} - t_{O_SKEW} - t_{OTT}$
  t_{DV} = 4.41 ns – 400 ps – 1.0 ns = 3.01 ns
- $t_{V}_min = t_{HO} + t_{O_SKEW} + t_{OTT}$
  t_{V}_min = 1.0 ns + 400 ps + 1.0 ns = 2.4 ns

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2 Latency code

Table 3 Latency Code (Cycles) Versus Frequency[6, 7]

	Read Command Maximum Frequency (MHz)			
	Fast Read (1-1-1) OTPR (1-1-1) RDAR (1-1-1) RDAR (4-4-4)	**Dual I/O (1-2-2)**	**Quad I/O (1-4-4) QPI (4-4-4)**	**DDR Quad I/O (1-4-4) DDR QPI (4-4-4)**[8]
Latency Cycles	**Mode Cycles = 0**	**Mode Cycles = 4**	**Mode Cycles = 2**	**Mode Cycles = 1**
0	50	80	40	N/A
1	66	92	53	22
2	80	104	66	34
3	92	116	80	45
4	104	129	92	57
5	116	133	104	68
6	129	133	116	80
7	133	133	129	92
8	133	133	133	102
9	133	133	133	102
10	133	133	133	102
11	133	133	133	102
12	133	133	133	102
13	133	133	133	102
14	133	133	133	102
15	133	133	133	102

Notes

6. The Dual I/O, Quad I/O, QPI, DDR Quad I/O, and DDR QPI, command protocols include Continuous Read mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Quad I/O command has 2 Continuous Read mode cycles following the address. Therefore, the legacy Quad I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Quad I/O command can be increased to allow operation up to the maximum supported 133 MHz frequency.
7. Other read commands have fixed latency, e.g., Read always has zero read latency. RSFDP always has eight cycles of latency.
8. DDR QPI is only supported for Latency Cycles 1 through 7 and for clock frequency of up to 92 MHz.

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3 DC characteristics

Table 4 DC characteristics (–40°C to +85°C range)

Symbol	Parameter	Test conditions	Min	Typ[9]	Max	Unit
I_{CC1}	Active power supply current (READ)[10]	Quad DDR at 102 MHz	–	70	100	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	200	µA
I_{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	120	

Table 5 DC characteristics (–40°C to +105°C range)

Symbol	Parameter	Test conditions	Min	Typ[9]	Max	Unit
I_{CC1}	Active power supply current (READ)[10]	Quad DDR at 102 MHz	–	70	100	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	300	µA
I_{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	150	

Table 6 DC characteristics (–40°C to +125°C range)

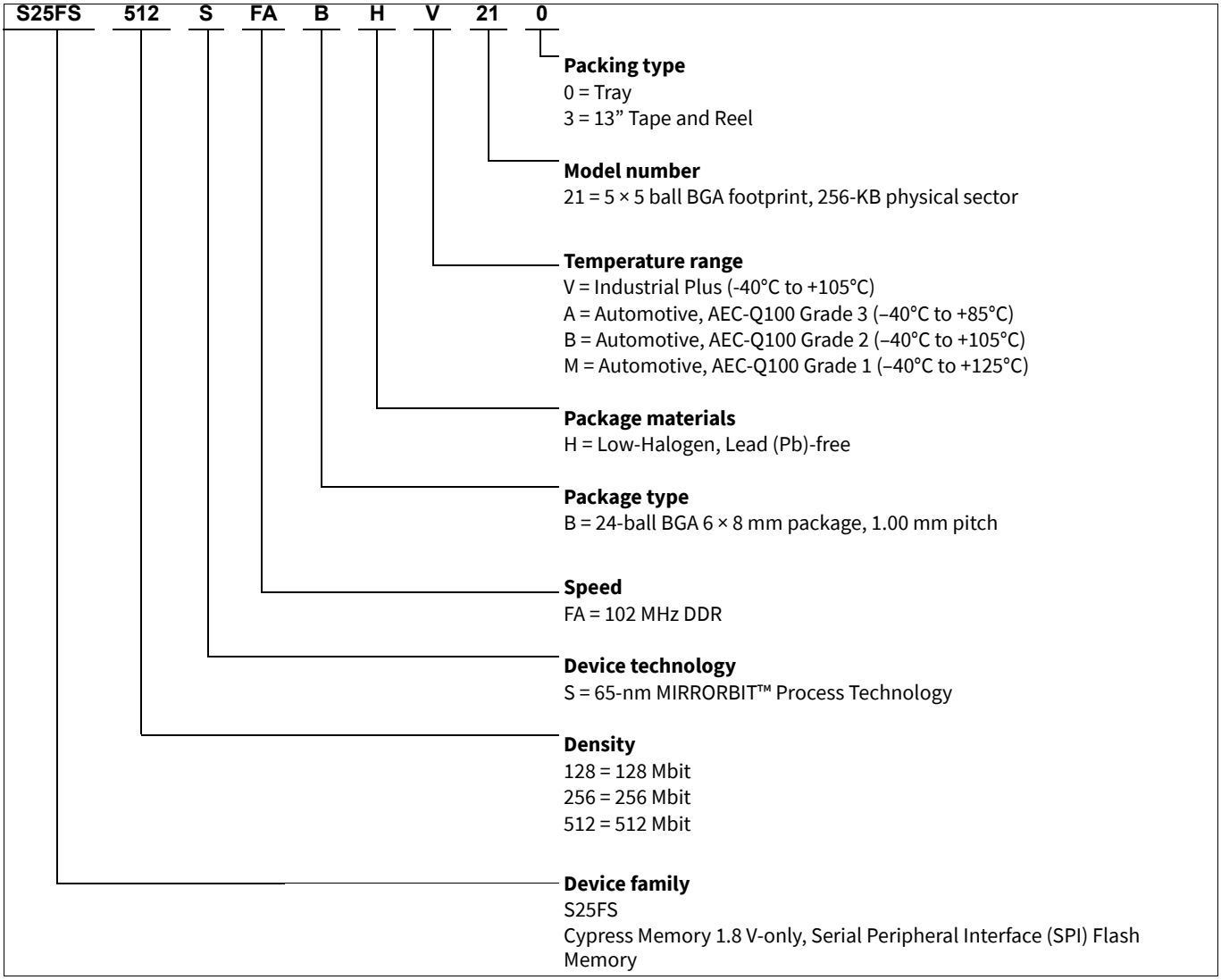
Symbol	Parameter	Test conditions	Min	Typ[9]	Max	Unit
I_{CC1}	Active power supply current (READ)[10]	Quad DDR at 102 MHz	–	70	100	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	450	µA
I_{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	350	

Notes
9. Typical values are at TAI = 25°C and VCC = 1.8 V.
10. Outputs unconnected during read data return. Output switching current is not included.

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4 Ordering part number

The ordering part number is formed by a valid combination of the following:



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4.1 Valid combinations — Standard

Valid combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 7 S25FS128S, S25FS256S, S25FS512S valid combinations: Standard

Base ordering part number	Speed option	Package and temperature	Model number	Packing type	Package marking
S25FS128S	FA	BHV	21	0, 3	FS128SFVH21
S25FS256S	FA	BHV	21	0, 3	FS256SFVH21
S25FS512S	FA	BHV	21	0, 3	FS512SFVH21

4.2 Valid combinations — Automotive Grade / AEC-Q100

Table 8 lists the configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 8 S25FS128S, S25FS256S, S25FS512S valid combinations: Automotive Grade / AEC-Q100

Base ordering part number	Speed option	Package and temperature	Model number	Packing type	Package marking
S25FS128S	FA	BHB	21	0, 3	FS128SFBH21
S25FS256S	FA	BHB	21	0, 3	FS256SFBH21
S25FS512S	FA	BHB	21	0, 3	FS512SFBH21

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Revision history

Document revision	Date	Description of changes
**	2016-03-01	Initial release.
*A	2017-02-07	Added Preliminary status. Replaced “100 MHz DDR” with “102 MHz DDR” in all instances across the document. Changed Max DDR clock rate from 100 MHz to 102 MHz in all instances across the document. Updated **Latency code**: Updated **Table 3**. Updated Note **8**. Updated **Ordering part number**: Added “Automotive, AEC-Q100 Grade 2 (–40°C to +105°C)” under “Temperature range”. Added **Valid combinations — Standard**. Added **Valid combinations — Automotive Grade / AEC-Q100**. Updated to new template.
*B	2017-12-08	Removed Preliminary status. Updated **DDR AC characteristics**: Changed maximum value of t_V parameter from 4.5 ns to 5 ns. Updated **Latency code**: Updated **Table 3**. Updated to new template.
*C	2017-08-10	Updated **Latency code**: Updated **Table 3**.
*D	2021-08-25	Updated **DC characteristics**: Replaced “Industrial Plus” with “DC characteristics” in heading. Added **Table 4**. Added **Table 6**. Updated **Ordering part number**: Updated details under “Temperature range”. Updated **Valid combinations — Automotive Grade / AEC-Q100**: Updated **Table 8** (Added OPNs).
*E	2023-01-04	Added S25FS128S, S25FS256S parts related information in all instances across the document. Added 128 Mb, 256 Mb densities related information in all instances across the document. Updated description under **General description**. Updated table under **Affected documents/Related documents**. Updated **Ordering part number**: Updated details under “Density”. Updated **Valid combinations — Standard**: Updated **Table 7**. Updated **Valid combinations — Automotive Grade / AEC-Q100**: Updated **Table 8**. Migrated to Infineon template.
*F	2025-08-01	Updated **Table 1**.

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